Volume 2, Issue 1, January 2012 ISSN: 2277 128X
International Journal of Advanced Research in Computer Science and Software Engineering
Research Paper
Available online at: www.ijarcsse.com

Advancement in Current Mirror Techniques

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Abstract— **The current mirror is one of the necessary parts in CMOS (Complementary Metal Oxide Semiconductor) analog circuit design. The current mirror can be used as an active element and as a biasing circuit. The circuit structures are supposed to be compatible with low-voltage operating environments to avoid the decrement in system performance caused by the low-voltage low-power designs including reduction of speed and operating current. Therefore, it is required to design the low power analog circuits based on CMOS technology. And for this, the feature size of the CMOS devices has decreased to very small dimensions. The current mirrors have been so modified so that magnitude of incremental output resistance and the accuracy of current-transfer ratio can be improved. Many of the biomedical circuits require large-voltage compliance current sources and current mirrors having high output impedance. Modern Nano-CMOS technologies are bring into being very appropriate to accomplish this objective.**

Keywords— **CMOS (Complementary Metal Oxide Semiconductor), PMOS (Positive Metal Oxide Semiconductor), NMOS (Negative Metal oxide Semiconductor), BDCCM (Bulk Driven Cascade Current Mirror), IC (Integrated Circuit)**

I. INTRODUCTION

The development in computers and communications requires much smaller chip size with low power and wide dynamic range [1]. Hence, low power and low voltage mixed mod circuits and analog are of a great importance. A series of current mirror circuit useful for low voltage analog circuit design are required to reduce channel length modulation and offering much higher accuracy [2]. Some of the principle building blocks to realize wide swing and regulated cascade current mirror, to achieve low input resistance, are discussed.

II. LOW VOLTAGE – LOW POWER CURRENT MIRROR

The High swing current mirror circuit shown in Fig. 1(a, b) consist of a common-source stage followed by a common-gate stage that has to be biased by a reference voltage V_{CP} and V_{CN}. Whereas the biased cascade circuit is operated at bare minimum reference voltage promising that both transistors are saturated for the actual output current [3]. The fixed biased cascade circuit has a fixed reference voltage that is best only for the maximum output current and deviates from optimal at lower currents.

A novel low-voltage low-power PMOS cascade current mirror utilizing the bulk-driven technique is described. The characteristics of the low-voltage bulk-driven cascade current mirror are analyse and validated, including the system dc transmission error, the frequency characteristics, noise performance and input/output resistance [4].

The topology of the low-voltage PMOS BDCCM is shown

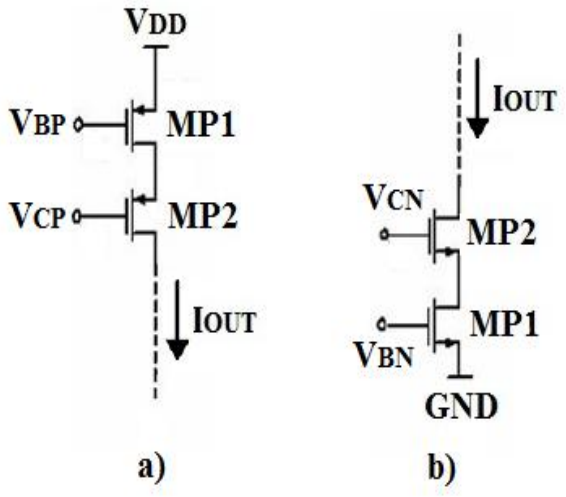

Fig. 1 High swing current mirror, (a) current source, (b) current sink

in Fig.2. The inversion layer is created by connecting the gate terminal to a fixed voltage V_G to form the conduction channel underneath the gate. Input signal is directly introduced to the bulk terminals of M1 and M3, whose source drain currents are put up by controlling weak positive bias between bulk and source of transistors. Low-voltage PMOS BDCCM may eradicate the restriction of threshold voltage on the signal pathway thereby accomplish a low input/output voltage drop.

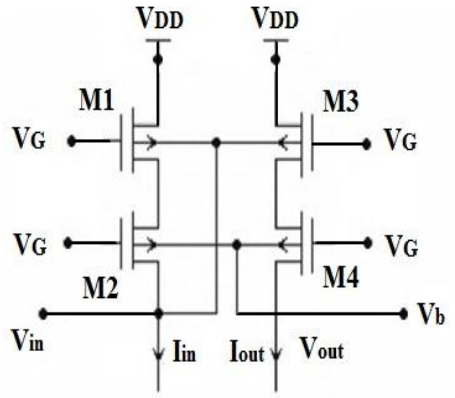

Fig. 2 Low voltage PMOS bulk driven cascade current mirror

III. BULK DRIVEN TECHNIQUE

The bulk-driven technique may efficiently abolish the restriction of the threshold voltage on the signal channel thereby dropping the supply voltage required by CMOS analog IC, and it is a main method to realize low voltage low-power IC design in the standard CMOS process. When it is compared with the normal gate-driven current mirrors, the low-voltage BDCCM decreases the input/output voltage drop and has a good input/output resistance characteristic together with an improved current driving capacity. But for the low self-gain of the bulk-driven transistor, a big equivalent noise and a small characteristic frequency f_T comes into action. So the shortcomings of this technique should be reduced by means of the detailed layout design [5] as far as possible. The low-voltage BDCCM is a novel cascade current mirror configuration with high performance, which is fit for low-frequency low-voltage CMOS analog IC design.

A new simple and high performance current mirror suitable for low voltage applications is presented. This circuit achieves very low input impedance, high output impedance with an accurate current copy. These characteristics are validated with simulations in 0.35µm CMOS TSMC-MOSIS technology [6].

An efficient implementation of a low voltage high performance CMOS current mirror [7], which used a two MOS sub-threshold amplifier, is described in Fig.3.

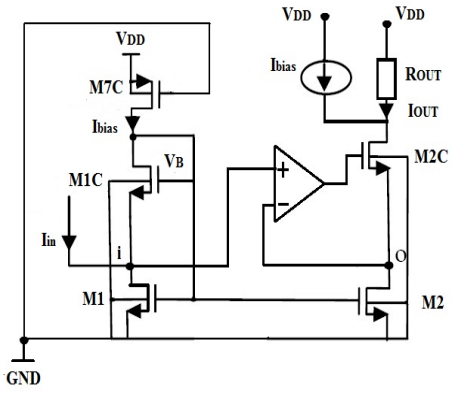

Fig. 3 Low supply voltage High speed CMOS current mirror

This current mirror shows a very high output impedance, low input impedance, low settling time and high bandwidth with only 1.2V of supply voltage. Current mirror can be used as a necessary element in low voltage mixed mode VLSI (Very Large Scale Integration) systems such as for implementation of high gain operational amplifiers and as a current buffer to sense current signals.

Low voltage high output impedance CMOS current mirror proposing enhanced output voltage compliance using bulk-driven technique is described [8]. The intangible schematic of the PMOS high output impedance current mirror is shown in Fig. 4. Circuit consisting of M1, M2, M3, and I_{B2} forms output part of the current mirror. The basic proposal is to use a feedback amplifier to maintain the drain to source voltage across M2 as stable as possible irrelevant of the output voltage. Adding up this amplifier idyllically increases the output impedance by a factor equal to loop gain plus one over that which would occur for low voltage low power BDCCM [4]. The circuit consisting of M4, M5, M6, I_{B1}, and I_{in} functions almost indistinguishable to a diode connected transistor, but is used in its place to assure that all transistor bias voltages are precisely matched to those of the output circuitry. As a result, I_{out} will very precisely match I_{in}.

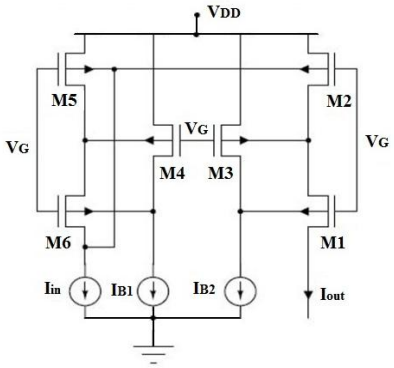

Fig. 4 High output impedance CMOS current mirror

For achieving high output impedance and enhanced input/output voltage compliances under bulk driven technique, low voltage high output impedance BDRCCM (Body Driven Regulated Cascade Current Mirror) is premeditated and simulated using a CMOS process. It would be appropriate for various analog applications of low voltage and low power.

On the basis of bulk driven PMOS transistor, a low voltage CMOS cascade current mirror (BDCCM) is presented [9], then the frequency characteristics and input/output impedance and are discussed.

The low-voltage PMOS BDCCM circuit is shown in Figure.5 It can efficiently unwind the threshold limitation of V_{IN} and V_{OUT}. It shows a fixed voltage V_G is connected to the gate of all the PMOS transistors to form the conduction channel between the source and drain and the n-well behaves as a bias and ascertains a leakage current by a slightly forward-biased

well-source junction. From Figure.5, we can get: $V_{SD2}=V_{SD1}+V_{SB3}-V_{SB4}$, $V_{SG1}=V_{SB2}$, in addition, $V_{SB1}=V_{SD1}$, $V_{SB3}=V_{SD3}$. For $I_{IN} > I_{SDS,\ MP1}$, the well-source junctions are working in the slightly forward-biased mode. For MP3 and MPI transistors matching well ($I_{SD1,MP3}=I_{SDS,MP1}$) and V_{SD1} is a positive value, V_{SD2} will be greater than zero. As a result, MP2 commence to turn on because the sum of V_{SD2} and V_{SB4} is greater than zero. The conditions mentioned above, besides DC feedback, particularly $V_{SDl}+V_{SB3} = V_{SD2}+V_{SB4}$ and the matching of the transistors force $I_{IN} = I_{OUT}$.

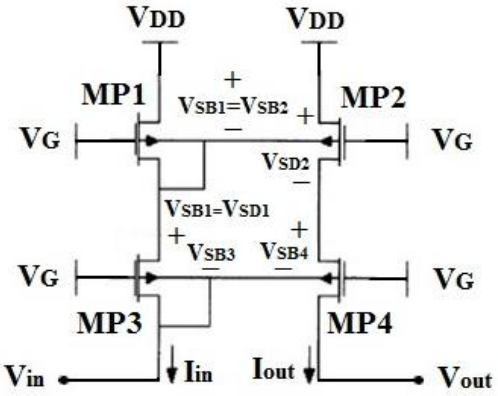

Fig. 5 Bulk-driven PMOS cascade current mirror

Since the bulk-driven PMOS technique can get rid of the threshold limitation on the signal channel and effectively rest the need for low-voltage analog circuits, this technique is an significant move towards to low-voltage analog designs based on the standard CMOS technology [10][11]. BDCCM is a circuit with high performance for low-voltage low-frequency CMOS analog designs.

IV. APPLICATIONS

A current-mirror attaining an incremental output resistance twice that of the Wilson circuit by the novel interconnection of a simple buffered current-mirror and a common-base stage [12] is described. The inspiration following this work is the growth of a new high performance current-conveyor CCII+ to be implemented in BJT complementary technology [13].

In many biomedical applications operating at low voltage necessitate very high output impedance current mirror. A Very high impedance current mirror, with fewer numbers of transistors which can operate at low voltage without any supplementary biasing circuitry is presented [14]. The planned current mirror uses MOS current dividers to sample the output current to attain very high impedance with a large output and voltage range. A feedback action is used to force the input and output currents to be equal. The planned circuit is also not sensitive to the biasing current. This accomplishment capitulates an increase in the output impedance by a factor near about to $g_m r_{out}$ matched up with that of the Super-Wilson current mirror, thus offering a potential solution to diminish the effect of the low output impedance of deep submicron CMOS transistors used in low voltage current mirrors and current sources.

The planned circuit proposes very high impedance due to the existence of the PMOS at both legs since no supplementary biasing circuit is used. It can be used for applications operating with very low current [15]. The planned circuit can be customized to generate very high impedance at the fragile inversion region for ultra deep sub-micron technology.

The design of a very-high output impedance CMOS current mirror with enhanced output voltage compliance is presented [16]. Recently, a regulated cascode CM that offers much higher output impedance than the conventional cascode CM was first presented in [17]. The planned current mirror uses MOS current dividers to sample the output current and a feedback action is used to force it to be equal to the input current; yielding very high impedance with a very large output voltage range. The planned implementation yields an increase of the output impedance by a factor of about $g_m r_o$ compared with that of the super-Wilson current mirror, thus offering a potential solution to diminish the effect of the low output impedance of ultra-deep submicron CMOS transistors used in sub 1-V current mirrors and current sources.

A customized regulated cascode structure having a feature of a push-pull inverting amplifier and having a low output compliance voltage is used in the implementations of low voltage regulated cascode current mirrors [18].

Three LVCM (Low Voltage Current Mirror) configurations with wide output swing ability that can operate with supply voltage below 1V is described. Employing a level shifter at input decreases the input compliance voltage whereas incorporation of adaptive bias and capacitance compensation develops CTR (Current Transfer Range) and BW (Bandwidth) correspondingly [19]. The planned RCCM configuration can find wide ranging applications in low voltage low power systems.

V. CONCLUSIONS

Various types of current mirror circuit and their applications are reviewed in this paper. The well-organized implementation of a low-voltage high performance current mirror allows complementary current mirrors with voltage necessities in the signal path to develop the input and output resistance. The bulk-driven technique may efficiently eradicate the restriction of the threshold voltage on the signal channel, thus dropping the supply voltage requisite by CMOS analog IC. Low supply voltage, high speed CMOS current mirror illustrates a very high bandwidth, high output impedance low input impedance and low settling time with only 1.2V of supply voltage. A low voltage high output impedance BDRCCM is designed and simulated using a CMOS process. BDCCM is a circuit with high performance for low-voltage low-frequency CMOS analog designs. The

very high impedance current mirror suggests very high impedance due to the existence of the PMOS at both legs since no auxiliary biasing circuit is used. It can be used for applications which operate with very low current. Three LVCM configuration having wide output swing ability that can operate with supply voltage beneath 1V are presented.

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