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Modified Vedic Multipliers: A Review

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Abstract: Multiplier is an important basic function in most fast processing systems. Multipliers are the key block used in high speed arithmetic logic units, multiplier and accumulate units, digital signal processing units etc. Multiplication requires substantially more hard-ware resources and processing time than addition and sub-traction. With the increasing constraints on delay, more and more importance is being laid on design of faster multiplications. As switching and critical computations of a multiplier are high, compared to other data path units of a processing architecture, design of low power, high speed multipliers are designed to reduce latency and power dissipation of a processing system. To enhance speed numerous modifications over the standard modified booth algorithm, Wallace tree methods for multiplier design have been made and several new techniques are being worked upon. Amongst these Vedic multipliers based on Vedic mathematics are currently under focus due to these being one of the fastest and low power multiplier. Vedic Mathematics is based on 16-sutras and 16-sub sutras invented in (1884-1960) which can be applied to any branch of mathematics like algebra, geometry, trigonometry etc. Its methods reduce the complex calculations into simpler ones because they are based on methods similar to working of human mind thereby making them simpler. It has been seen that being coherent and symmetrical, they consume lesser power and acquire lower chip area. In Vedic mathematics there are three sutras Nikhilam Navatascaraman Dasatah, Ekadhikena Purvena and Urdhva Tiryakbhyam used for multiplication. In this paper I have discussed comparison between different vedic multiplers based on commonly used Urdhva Tiryakbhyam and Nikhilam Navatascaraman Dasatah algorithms. This paper also discussed the different modifications in vedic multipliers which improves performance of these multipliers. The result of work helps to choose a better option between methods of vedic multiplier infabricating different systems. So by analyzing the working of different multipliers helps to frame a better system.

Keywords: DSP, MAC, FFT, SUM

I. INTRODUCTION

Multiplication is a fundamental function in arithmetic operations. It is used in the design of microprocessors , Accumulate(MAC) unit , RISC processors, in many Digital Signal Processing (DSP) applications such as convolution, Fast Fourier Transform(FFT) and filter circuits .

A system's performance is generally determined by the performance of the multiplier because the multiplier is generally the slowest element in the system so there is a need of high speed multiplier. Furthermore, it is generally the most area consuming .Hence, optimizing the speed and area of the multiplier is a major design issue. However, area and speed are usually conflicting constraints so that improving speed results mostly in larger areas.

Therefore there are two possible ways to speed up the multiplication reduce the number of partial products or accelerate their accumulation. A smaller number of partial products also reduces the complexity, and as a result reduces the time needed to accumulate the partial products.

Over the past few decades, various architectures of multipliers have been designed. But Vedic multiplier is the Easiest and the fastest multiplier (Vucha, 2014).Among 16 sutras of Vedic mathematics; Urdhva Tiryagbhyam is a general formula which is applicable to all cases of multiplication. This Sutra also shows the effectiveness of to reduce the NXN multiplier structure into an efficient 4X4 multiplier structures[6]. Nikhilam Sutra is much more efficient in the multiplication of large numbers as it reduces the multiplication of two large numbers to that of two smaller ones. Multiplier is faster for small inputs and Nikhilam multiplier is better for large inputs. This paper investigates novel architecture

The Vedic multiplication method which is basically array multiplication method permits the use of a highly recursive type multiplier architecture resulting in significant improvement in the speed [10-14]. The layout of Vedic multiplier is highly compact resulting in very small contributions of interconnects to the overall propagation delay as the operand size increases.

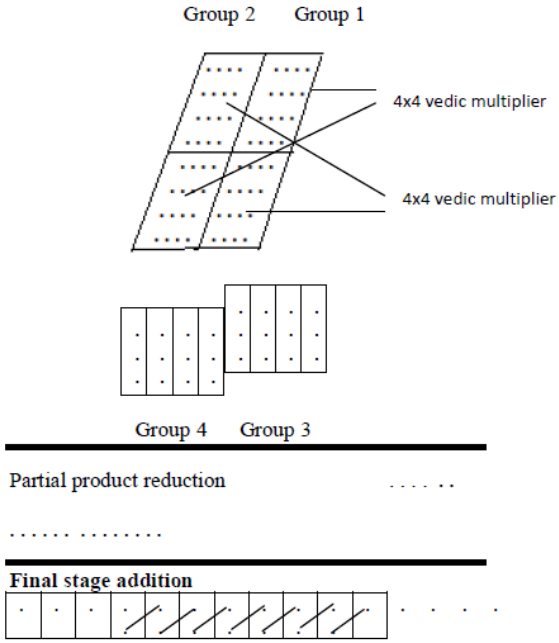
The speed of multiplier depends on type of adder. For high speed multiplication, fast adders are required.

This paper discuss the different types of Vedic multipliers using different types of adders used to improve the performance of multiplier unit. The effective methods for multiplications are studied from all types of Vedic multiplication methods and can be selected for designing better system.

II. EFFECTIVE METHODS FOR PERFORMANCE IMPROVEMENTS.

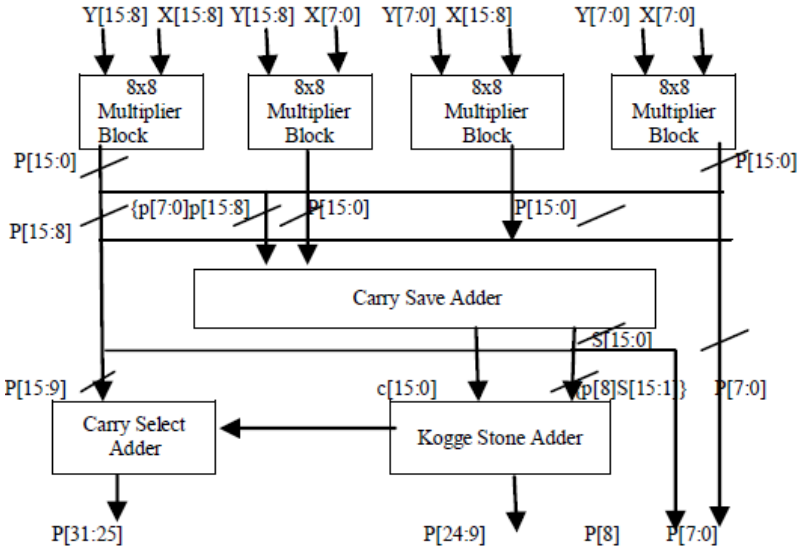
A. Design and Performance Comparison of Adiabatic 8-bit multipliers :

H. V. Ravish Aradhya [1] proposed ECRL based 8-bit multiplier designs and compares them with the CMOS designs. The proposed work designs an 8x8 Vedic-Dadda hybrid multiplier using combination of both Vedic sutra and Dadda compression technique, a new hybrid multiplier named Vedic-Dadda multiplier . In the first stage, partial products are generated and summed up using 4x4 multipliers.The partial products are divided into four parts, group1 to group4 using the decomposition logic. Group1 and group4 use 4x4 Vedic multipliers, while group2 and group3 use 4-bit Dadda multipliers as shown in Fig. 7. The intermediate partial product matrix is reduced to a height of two using eight full adders and in the final stage an 11-bit Kogge-stone adder is used to sum up the partial products and obtain the product bits. ECRL Adiabatic Logic using a 4-phase power clock provides low leakage losses at lower frequencies and has larger bandwidth of optimum performance. The low power dissipation is due to the use of 'Urdhva-Tiryagbhyam' sutra and the increase in speed is due to parallelism in computing partial products and their summation.



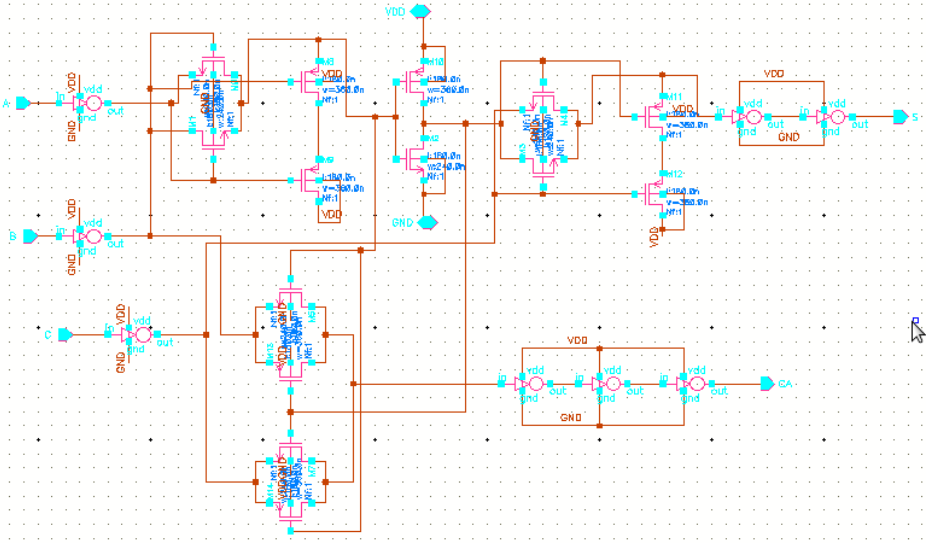
B. Implementation of a High Speed Multiplier desired for High-Performance Applications Using Kogge Stone Adder:

S Nikhil† and Mrs. P. Vijaya Lakshmi [2] proposed Vedic algorithm to design a 8-bit multiplier using fast adders, which can add the partial products with a high speed and reduces the power delayproduct. The design of a 8x8 multiplier block is as shown in Fig. To obtain 8 × 8 multiplier block, the multiplicand and multiplier bits are decomposed equally and partial products are added using Carry save adder which can generates the sum and carry output bits. Then, the sum and carry bits of carry save adder are added by using kogge stone adder along with the partial product bit that generates the final product term and a carry bit Cin. The final stage of addition is done by using carry select adder that contains multiplexers and half adders. The usage of the fast adder in the proposed design improves the performance in terms of delay, and power-delay product.In the proposed multipliers,the summation of partial products of Vedic multiplier was slightly modified using carry save adder, kogge-stone adder,and carry-select adder in order to improve the efficiency of the multipliers.

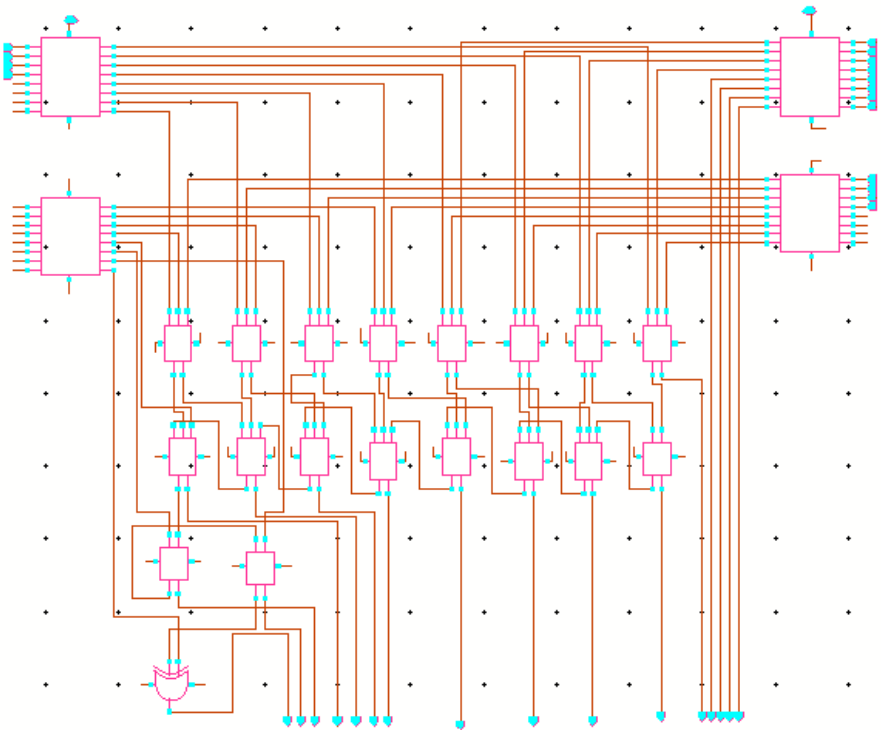


C. Design of High Performance 8-bit Vedic Multiplier:

Yogendri, Anil Kumar Gupta[3] discussed fast and low power multiplier architecture using Urdhva-tiryakbyham sutra. For designing a high speed, low power multiplier, it is required that full adders must consume low power and provide for high speed. In addition for k-bit binary adder low power, high speed full adders with efficient scheme for carry generation and propagation is required. This proposed architecture is regular. It is highly recursive in nature for designing an m-bit multiplier. The recursive nature of Vedic multiplier permits the design of highly compact layout that is silicon area used is minimum. The compact layout also ensures that the interconnect length is minimum which also leads to higher speed. Further, this architecture is such that the bigger multipliers can be easily built just by adding an adder block and using the smaller multipliers as functional blocks. This permits the reuse of smaller multipliers to a great extent.In this work, the 20T FA reported in [15] is used. The SUM (S) output has been generated using two XOR gates. The XOR function is obtained using pass transistors based XNOR gate followed by an inverter to restore the logic levels. For generating the Carry output, transmission gates have been used. The advantage of this FA circuit is that the all the transistors are minimum area transistors i.e. 360n/240n for pMOS and 240n/180n for nMOS. In addition to the above, FA should also have equal delay from input to both the outputs i.e. Sum and are minimum.



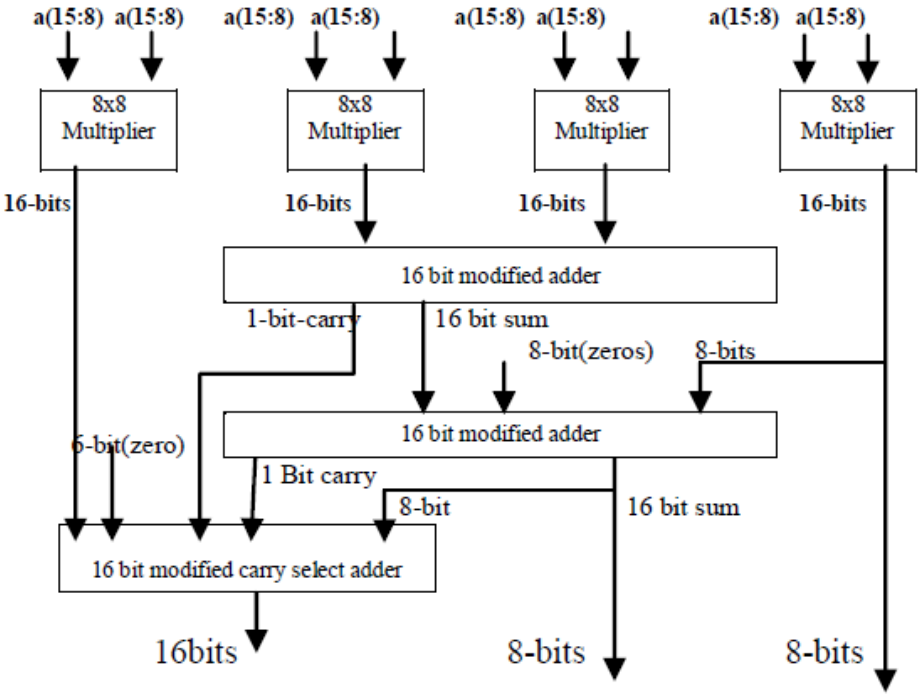
Schematic of 20T Full Adder



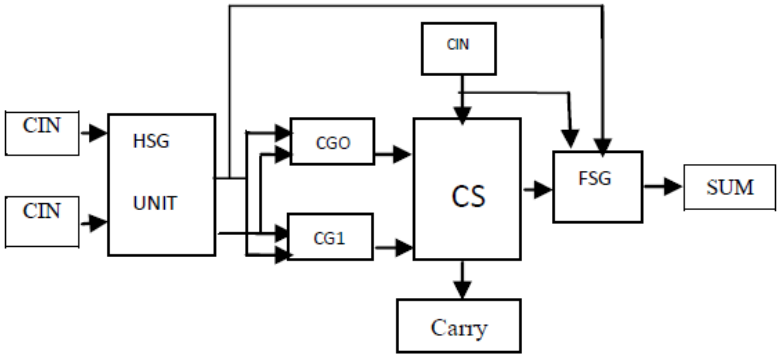
Schematic of 8-bit multiplier

D. Implementation of High Speed Vedic Multiplier using Modified Adder:

M. Akila, C. Gowribala, S. Maflin Shaby[4] This paper proposed new innovative modified carry select adder with performance improvement in delay and area.



16 Bit Multiplier

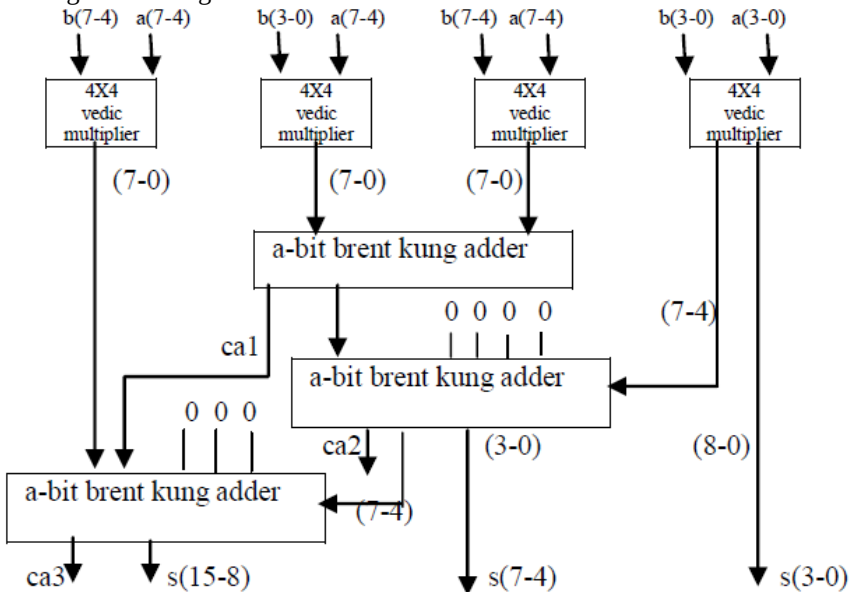


Adder Unit

Half sum generation unit, Full sum generation unit generates sum and carry using modified carry select adder.

E. Performance Evaluation of 8-Bit Vedic Multiplier with Brent Kung Adder:

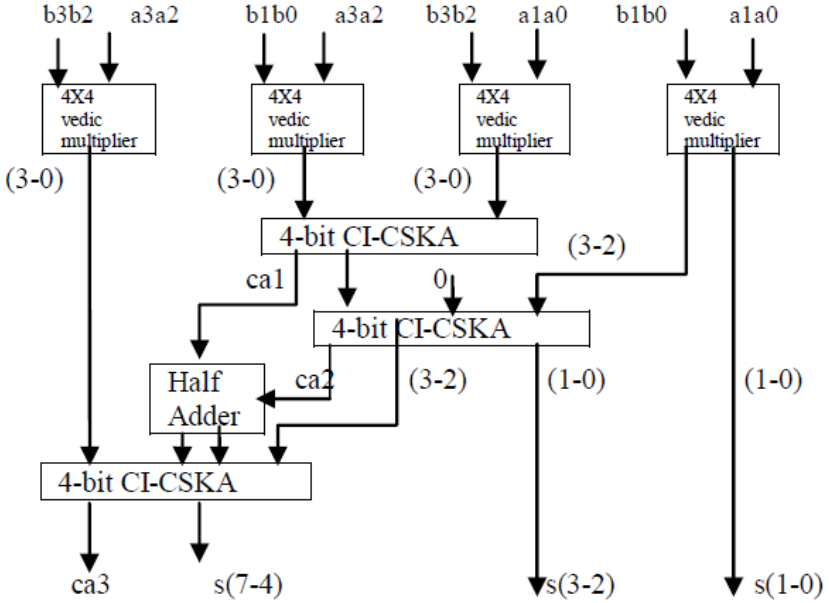
Nidhi Singh and Mohit Singh [5] designed 8x8 multiplier using 4x4 vedic multiplier as a basic block and adding partial products using Brent Kung adders.



Thus Brent Kung adder based Vedic multiplier is found to have reduced delay by 30.6 %. The speed of Brent Kung adder based multiplier is increased but the only limitation is that area is slightly increased.

F. Vedic Multiplier Using High Speed Carry Skip Adder:

P.Pavan Kumar, P.Anjaneya, O.Homa Kesav: To reduce the delay in the Carry Skip Adder (CSKA), high speed Carry Skip Adder structure is proposed. In the proposed structure speed can be improved by applying concatenation and incrementation schemes (CI-CSKA). In addition, the proposed structure replaces the multiplexer logic by the AND-OR-Invert (AOI) and OR-AND-Invert (OAI) compound gates. The Vedic multiplier is designed using CI-CSKA adder results in the speed improvement and reduces the delay compared with the same multiplier designed using CSKA.



Hardware realization of 4x4 Vedic Multiplier designed with CI-CSKA

III. RESULTS

Comparision Table between different Multiplier Architectures

Table I

Paper	Type of Adder	No.of Bits	Dealy (ns)
A	Kogge-Stone parallel adder	8	21.001
B	Kogge Stone Adder	8	15.028
C	20T Adder	8	2.5
D	Modified Carry Select Adder	16	10.73
E	Brent Kung Adder	8	6.176
F	Concatenation and Incrementation Carry Select Adder	8	16.89

IV. CONCLUSION

Vedic Multiplier is seen to be efficient in speed, power and area in digital designs with respect to other multipliers. In existing multipliers, the summation of partial products of Vedic multiplier was slightly modified using carry save adder, Kogge-Stone adder, carry-select adder and Brunt Kung Adder in order to improve the efficiency and performance of the multipliers.Experimental results of the different proposed multiplier with fast adders can achieve significant improvement in delay and power-delay product when compared with the conventional multiplier architectures.

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