



## High Speed and Area Optimize Shift Register Design in Deep Submicron Technology

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**Abstract:** *The work comprises of low power and low area shift register design using the pulse latch design using transmission gate logic. For speed enhancement a combinational shift register is design using CMOS layout design on 50nm technology. The channel length of NMOS and PMOS transistor is 0.05 $\mu$ m and that of width is 0.1 and 0.15 $\mu$ m. Transmission gate base logic pulse latch shift register is faster shift register as compare to shift register design using flip flop circuit. This method solves the timing problem between pulsed latches through the use of multiple non-overlap delayed pulsed clock signals instead of the conventional single pulsed clock signal. The shift register uses a small number of the pulsed clock signals by grouping the latches to several sub shifter registers and using additional temporary storage latches.*

**Keywords:** PMOS, VLSI, AND, NOT

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### I. INTRODUCTION

The shift register are the commonly use circuit in design of memory, digital filters, microprocessors etc and in many applications such as microcontroller base system, image processing, communication receivers etc. In recent VLSI circuits the increase in word length of data requires large length shift registers. Thus with increase in word length of the shifter register, the area and power consumption of the shift register become important design considerations.

The internal structure of shift register composed of N number of series connected D flip flops. The output of one flip flop is directly connected to the input of second flipflop through interconnect. There is no circuit present between this connection, thus area and power consumption is the major design constraint. The area is reduce by reducing the size of transistors, length of interconnect and reducing the number of transistors requires for design. In modern VLSI design, pulsed latches is use, because a pulsed latch is smaller than the conventional flip-flops. But the pulsed latch cannot be used in a shift register due to the timing problem between pulsed latches [1]. This paper presents the area and power optimizes shift register design using transmission gate base pulse latch. This shift register increases the speed of operation using selection input logic instead of the conventional single pulsed clock signal. The latches are design using combination multiplexer logic cell using transmission gates.

### II. RELATED WORK

The work in [1], is base on pulse latch shift register design on 0.18 $\mu$ m technology. This design of speed tradeoffs to solve the timing problem using multiple non-overlap delayed pulsed clock signals instead of the conventional single pulsed clock signal. Their shift register reduces the number of delayed pulsed clock signals significantly, but it increases the number of latches because of the additional temporary storage latches. The work focus on delay degradation due to parasitic capacitance and resistance degraded the rising and falling times of the clock pulse increase due to the wire delay [1]. In [2] a Bistable Cross-coupled Dual Modular Redundancy Adaptive Coupling Flip-Flop on 65nm technology using pass transistor logic. In this work the PMOS use as pass transistor are weak to transmit strong 0 logic. This creates the difficulty to transmit the master flipflop signal to the slave flipflop output. The Adaptive-Coupled (AC) two transistors make it easy to overwrite the master latch. When the next value is same as the current value, the cross-coupled loop keeps the current value. When it is different, the AC makes the holding value weak. After simulation the delay, and power 0.72ns and 0.51 $\mu$ W [2]. In [3] The AC elements composed of a CMOS pass gate are required to overwrite the master latch connected to the input inverters through PMOS pass transistors. They weaken the connection between the cross coupled inverters when the input and overwritten values are different. This work explains how the AC element works when changing the stored value ( Q ) from 0 to 1. When the master latch value is transferred to the slave latch, the AC elements isolate the cross-couple connection in the master latch to make it easier for the master latch to overwrite the slave value [3]. [4] design transmission-gate based master-slave flip-flop using 180nm technology [4]. For the large output load the charging and discharging of output capacitance, thus delay increases. In static CMOS delay depends on R (resistivity) which is inversely proportional to the width of the transistor and c (capacitance) which is proportional to the size of the transistor in the next stage. Hence by increasing the channel width of the transistor, speed will be increased since there is more space for the current to flow and it is called as Transistor sizing. The delay calculates in this work is in the range of 0.571ns to 3.217ns with the power consumption of 1mW to 7mW [4].

### III. D FLIP FLOP BASE SHIFT REGISTER

The construction of a D flip-flop with two D latches and an inverter is shown in Fig. . The first latch is called the master and the second the slave. The circuit samples the D input and changes its output Q only at the negative edge of the synchronizing or controlling clock (designated as Clk ). When the clock is 0, the output of the inverter is 1. The slave latch is enabled, and its output Q is equal to the master output Y . The master latch is disabled because Clk = 0. When the input pulse changes to the logic-1 level, the data from the external D input are transferred to the master. The slave, however, is disabled as long as the clock remains at the 1 level, because its enable input is equal to 0. Any change in the input changes the master output at Y, but cannot affect the slave output. When the clock pulse returns to 0, the master is disabled and is isolated from the D input. At the same time, the slave is enabled and the value of Y is transferred to the output of the flip-flop at Q . Thus, a change in the output of the flip-flop can be triggered only by and during the transition of the clock from 1 to 0.

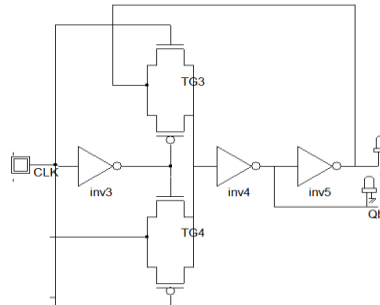


Figure 1: Schematic Diagram of Pulse Latch Circuit

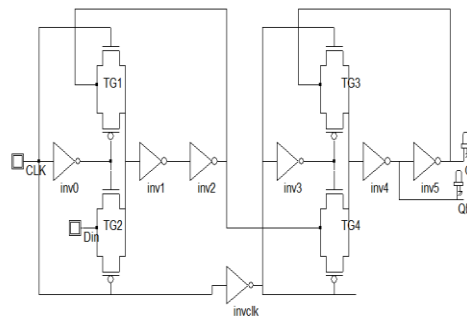


Figure 2: Schematic Diagram Master Slave Flip flop

### IV. PULSE CLOCK GENERATOR

The pulse clock generator generates clock pulses for the level triggering of latch. The pulse clock generator consists of two bit counter and 2X4 decoding circuit. The two bit counters output is connected to the two inputs of decoder circuit. The output of decoder generates a logic high pulse at anyone output at one time. These outputs are connected to the level trigger clock signal of pulse shift register. The schematic design of pulse clock generator is shown in fig 3.

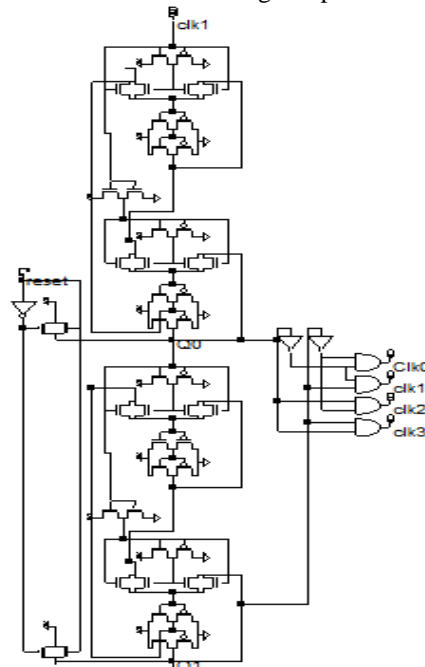


Figure 3: Pulse Clock Generator

The counter is design with flip flops using master slave arrangement of two latches. The decoder circuit is design using four AND logic gates and two NOT logic gates. This design requires 10 transmission gates out of which two transmission gates are connected to the reset signal of counter circuit. The same reset signal is further use to reset the pulse shift register circuit. The schematic design of clock pulse generator consist of 17 NOT logic gates and 4 AND gate requires total 78 MOS transistors.

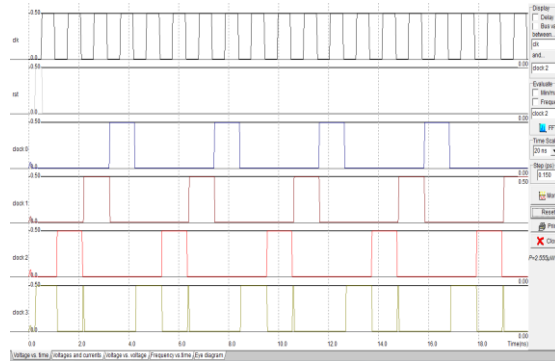


Figure 4: Timing Simulation of clock pulse generator

**V. PULSE LATCH SHIFT REGISTER**

The pulse latch shift register is divided into sub shifter registers to reduce the number of delayed pulsed clock signals. A 4-bit sub shifter register consists of five latches and it performs shift operations with five non-overlap delayed pulsed clock signals (CLK\_pulse(1:4) and CLK\_pulse(T)). In the 4-bit sub shifter register #1, four latches store 4-bit data (Q1-Q4) and the last latch stores 1-bit temporary data (T1) which will be stored in the first latch (Q5) of the 4-bit sub shift register #2. Fig. 5(b) shows the operation waveforms in the proposed shiftregister.

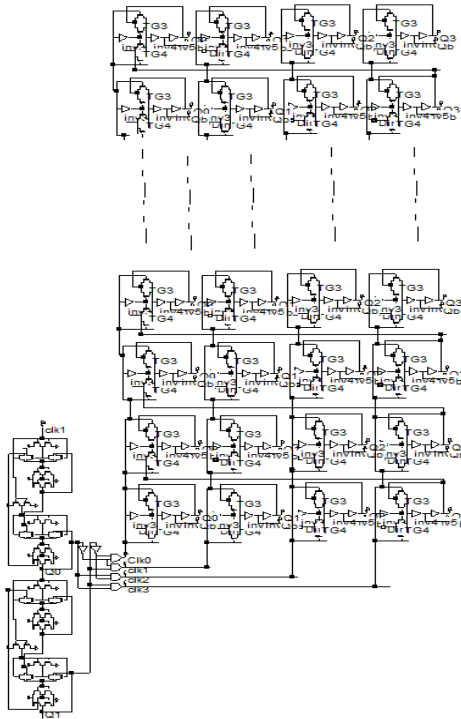


Figure 5: PulseLatch Base Shift Register

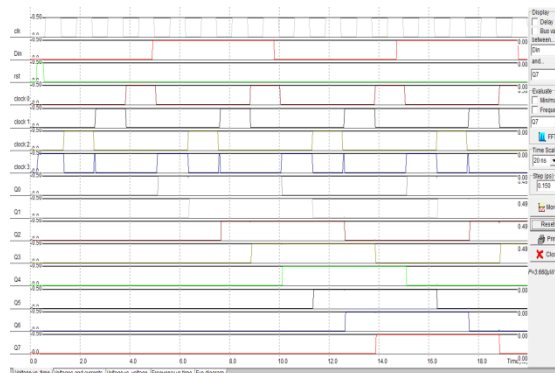


Figure 6: Timing Simulation of Pulse Latch Base Shift Register

Five non-overlap delayed pulsed clock signals are generated by the delayed pulsed clock generator in Fig. 6. The sequence of the pulsed clock signals is in the opposite order of the five latches. Initially, the pulsed clock signal CLK\_pulse (T) updates the latch data T1 from Q4. And then, the pulsed clock signals CLK\_pulse (1:4) update the four latch data from Q4 to Q1 sequentially. The latches Q2–Q4 receive data from their previous latches Q1–Q3 but the first latch Q1 receives data from the input of the shift register (IN). The operations of the other sub shift registers are the same as that of the sub shift register #1 except that the first latch receives data from the temporary storage latch in the previous sub shift register [1].

## VI. CONCLUSION

In this work we have discuss the schematic structure and operation for various flip-flops with its timing simulation. The transmission gate-based flip-flops exhibit the best power-performance trade-off with a total delay (clock-to-output) reduces as compare to conventional flipflops. The use of transmission gate in fliflop design will reduce the number of transistors requirement

## REFERENCES

- [1] Byung-Do Yang "Low-Power and Area-Efficient Shift Register Using Pulsed Latches" IEEE Transactions on Circuits and Systems—I: Regular Papers, Vol. 62, No. 6, June 2015 pp no 1564.
- [2] Masaki Masuda, Kanto Kubota, Ryosuke Yamamoto, Jun Furuta, Kazutoshi Kobayashi, and Hidetoshi Onodera "A 65 nm Low-Power Adaptive-Coupling Redundant Flip-Flop" IEEE Transactions On Nuclear Science, Vol. 60, No. 4, August 2013 pp no 2750.
- [3] K. Kobayashi, K. Kubota, M. Masuda, Y. Manzawa, J. Furuta, S. Kanda, and H. Onodera "A Low-Power and Area-Efficient Radiation-Hard Redundant Flip-Flop, DICE ACFF, in a 65 nm Thin-BOX FD-SOI" IEEE Transactions On Nuclear Science, Vol. 61, No. 4, August 2014 pp no. 1881.
- [4] A.ParvathiKarthica "Power Efficient Synchronous Counter Using Transmission-Gate Based Master-Slave Flip-Flop With Modified Logical Effort Optimization" International Conference on Electronics and Communication Engineering (ECE) 7th April 2013 ppno. 86.
- [5] S. EhsanRazavi, " Shift Register Design Using D-Flip flop with Low Power Consumption and High Speed " International Journal of Science and Advanced Technology (ISSN 2221-8386) Volume 1 No 7 September 2011
- [6] Ch. DayaSagar, T. Krishna Moorthy "Design of a Low Power Flip-Flop Using MTCMOS Technique" International Journal of Computer Applications & Information Technology Vol. 1, No.1, July 2012.