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Design and Implementation of an Efficient 32×32 Bit Vedic Multiplier Using Kogge Stone Adder

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Abstract-- This paper reveals the design of an efficient 32×32 bit Vedic multiplier using the Urdhva Triyakabhyam (UT) sutra of Vedic mathematics. Vedic mathematics is based on 16 formulae constructed by Sri Bharati Krishna Tirthaji. Multiplication operation is the most vital operation in many numeric computations. Since speed is definitely a noteworthy need in the numerical computations, rise in speed can be enhanced by diminishing the quantity of steps during calculation. The UT sutra helps to reduce the carry propagation from LSB to MSB in the calculation of the intermediate products and sums. The proposed Vedic multiplier is designed using modified ripple carry adder and Kogge Stone adder. It is coded in Verilog HDL, synthesized using Xilinx ISE 14.7 and implemented on Spartan-6 FPGA board. The work has proved that the area and delay of the proposed Vedic multiplier are less than the existing Vedic multipliers.

Keywords— Multiplier, Urdhva Triyakabhyam, Kogge Stone Adder, Ripple Carry Adder, Verilog HDL

I. INTRODUCTION

Multiplication operation is the most key operation in several numerical estimations. It discovers its application in multiply and accumulate (MAC) unit, microchips, microcontrollers and computerized signal processing applications such as filtering, Fast Fourier Transform (FFT) and convolution. As multiplication assumes an imperative part in large portions of the applications, we need to select an efficient multiplier in terms of area, power consumption and delay. Since speed is inevitably a major need in the multiplication operation, rise in speed can be improved by reducing the number of steps in the calculation process. The system performance is determined by the speed of the multiplier. The term Vedic mathematics is the general name assigned to a set of 16 mathematical sutras.

These 16 sutras can be used to solve problems ranging from arithmetic to geometry to algebra to conics to calculus and help to reduce the carry propagation from LSB to MSB in the calculation of the partial products and sums. Consequently, incorporating Vedic arithmetic strategies for the multiplier outline would bring about the sparing of computation time, in this way expanding the speed of multiplication operation.

II. VEDIC MULTIPLIER

The proposed Vedic multiplier depends on the Urdhva Triyakabhyam (UT) sutra. Urdhva Triyakabhyam is taken from the Sanskrit. "Urdhva" signifies "Vertically" and "Triyakabhyam" signifies "Crosswise". This UT sutra can be by and large connected to all instances of multiplication, for example, binary, hexadecimal, decimal and octal.

2.1) 4×4 Multiplier [1]

The 4×4 multiplier architecture [1] shown in fig-2.1 consists of a 4-bit adder and seven full adders and two half adders. It avoids the use of four 2×2 multipliers in implementing the existing multipliers thereby reducing the number of components in implementing the 4x4 bit multiplier. It will reduce the delay and area compared to the 4×4 existing multiplier which is designed using the four 2×2 multipliers.

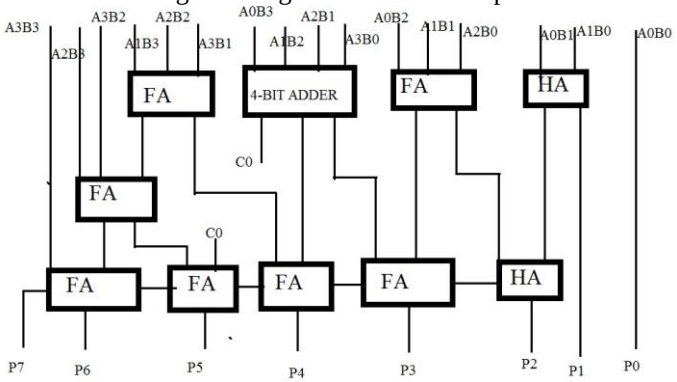

Fig-2.1 Block Diagram of 4×4 Bit Multiplier [1]

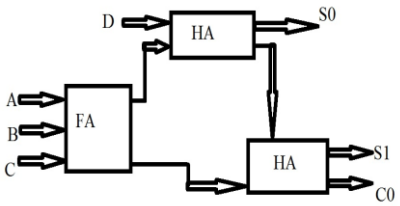

Fig-2.2 The 4-Bit Adder

The 4 bit adder illustrated in fig-2.2 performs the function of 4 bit addition. It produces two bits of sum and one carry as output.

2.2) 8x8 Vedic Multiplier

The 4×4 multiplier shown in fig-2.1 is used to implement the 8×8 Vedic multiplier as shown in fig-2.3. It consists of three ripple carry adders which are modified as per the length of inputs

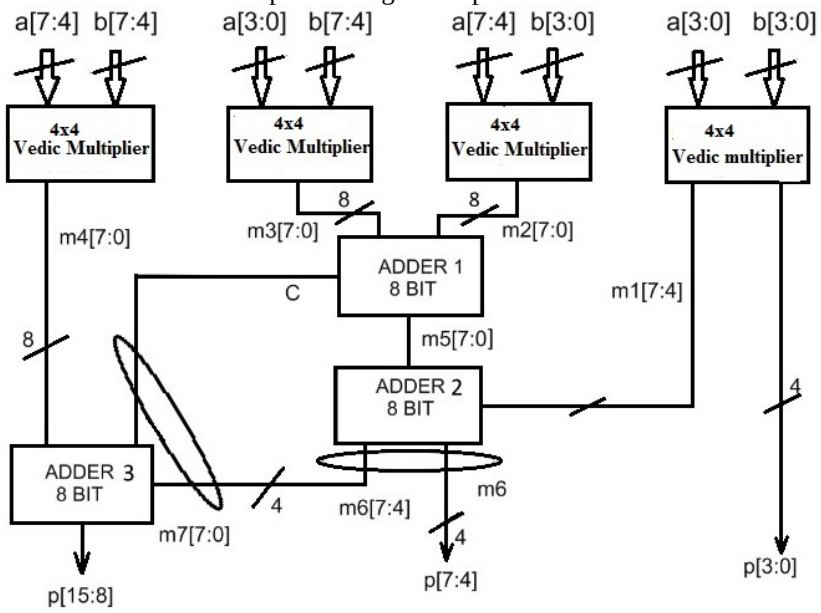

Fig-2.3 Block Diagram of 8×8 Vedic multiplier

The outputs of 2nd and 3rd multiplier blocks are added by the ADDER1. The ADDER-1 consists of one half adder and seven full adders connected in ripple carry adder style as shown in figuere-2.4

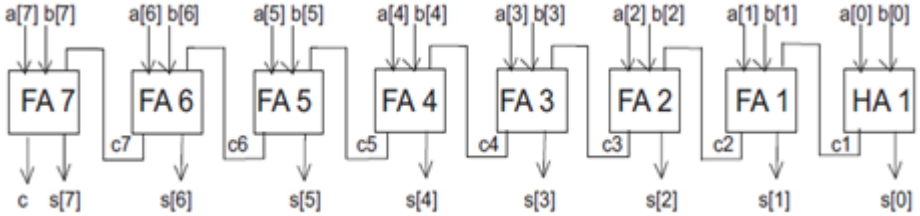

Fig-2. 4 ADDER-1 arhitecture

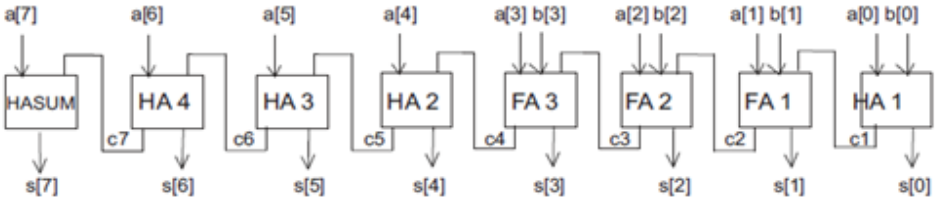

Fig-2.5 ADDER-2 architecture

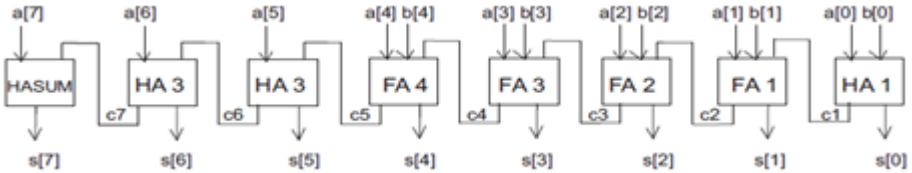

Fig-2.6 ADDER-3 architecture

The ADDER-2 in the fig-2.3 adds the higher nibble of the first multiplier block (m1 [7:4]) with the sum output of ADDER-1 (m5 [7:0]). ADDER-2 uses four half adders, three full adders and an XOR gate as shown in figuere-2.5

The block diagram of ADDER-3 is shown in fig-2.6. It adds 8 bit output of fourth multiplier block and higher nibble of ADDER-2 and the carry from ADDER-1. ADDER-3 consists of 3 half adders, 4 full adders and a XOR gate. The 8 bit output (m7 [7:0]) of ADDER-3 forms the higher byte of the final output (p [15:8]).

Using these modified ripple carry adders we can avoid appending zeros which is to make both the inputs of same length thereby reducing the hardware utilization.

2.3) 16×16 Bit Vedic Multiplier:

Similarly, to design 16×16 bit Vedic multiplier, we use the four 8x8 multipliers of figuere-2.3 and three 16-bit ripple carry adders which are modified as per the length of inputs. Its block diagram is shown in figuere-2.7. The 16 bit adders are designed in the same way in similar to the 8 bit adders as discussed above.

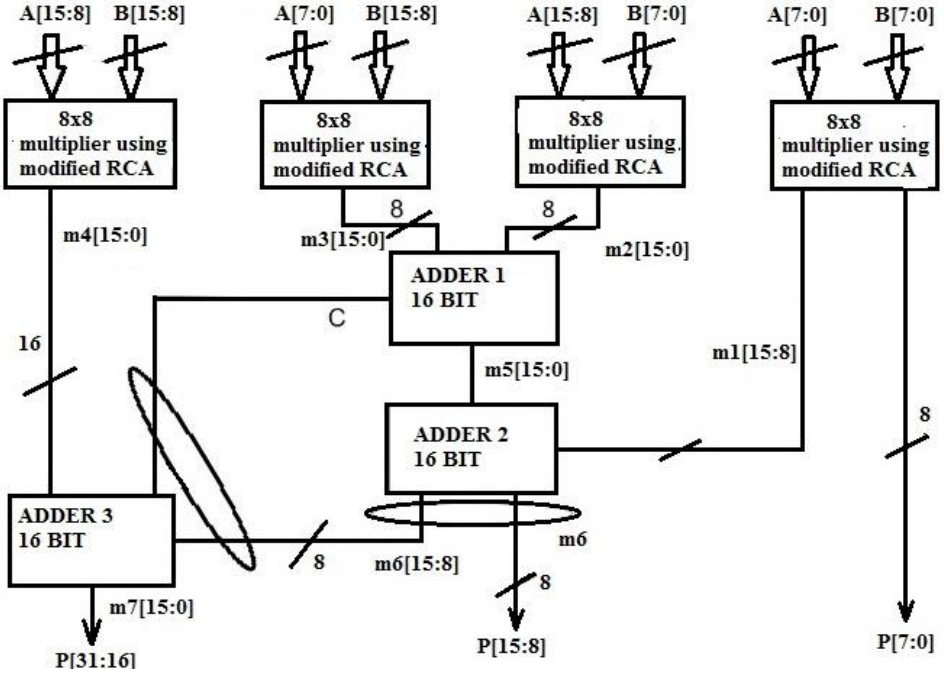

Fig-2.7 16×16 Bit Vedic Multiplier

III. PROPOSED 32×32 BIT VEDIC MULTIPLIER

The 32×32bit Vedic multiplier is designed using the above 16×16 bit multipliers modules and Kogge Stone Adders(KSA) as shown in the below fig-2.8. Since for higher order bit addition, the ripple carry adder consumes more power and more area on the chip and the delay is more, it is better to use here the Kogge Stone Adder (KSA) which is efficient adder for higher order addition. The first kogge stone adder adds the outputs of second and third multipliers with the first two higher bytes of the first multiplier. The second adder performs the addition of the output of fourth multiplier and the higher bytes of the first adder.

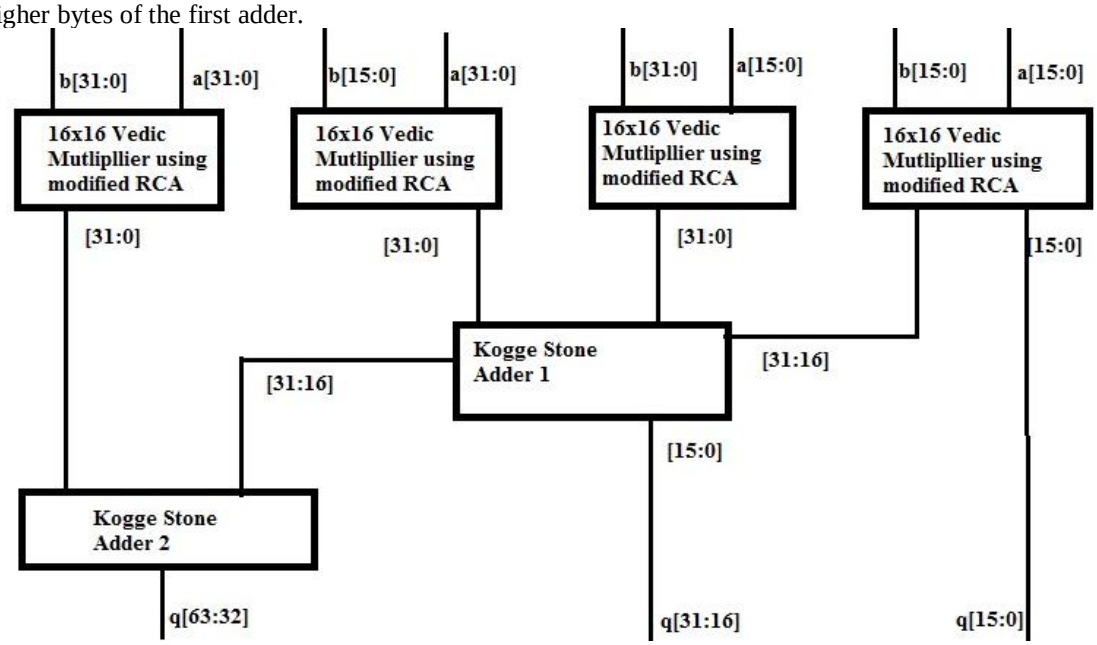

Fig-3.1 Block Diagram of Proposed 32×32 Bit Vedic Multiplier

3.1) Kogge Stone Adder (KSA) [6]

Kogge Stone Adder is one of the fastest parallel prefix adders. It takes more area to implement than other parallel prefix adders like Brent Kung adder, Harl Carlson adder and the Spanning Tree adder, but has lower fan-outs at each stage that increases its performance. It is demonstrated that the Kogge Stone adder is best suited for higher order addition. Fig-3.2 illustrates the block diagram of 4 bit Kogge Stone Adder.

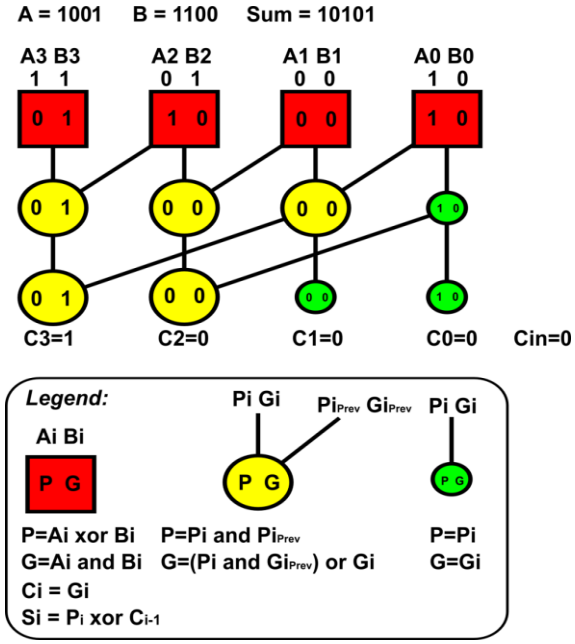

Fig-3.2: Illustration of 4-bit Kogge Stone Adder [6]

The working procedure of KSA can be easily explained as follows.

1. Pre-processing:

In this step, the Generate and Propagate signals for each pair of bits in a and b are computed. Below equations will represent this step.

P=Ai xor Bi.

G=Ai and Bi

Ci=Gi

2. Carry Look Ahead network: This block makes the KSA distinct from the other adders and is the key block behind its high performance. In this step intermediate carries are computed and represented by the following equations.

P= Pi and Pprev.

G= (Pi and Giprev) or Gi.

3. Post-Processing:

In this final step the sum bits are computed as given by the following equation.

Si= $Si = Pi\ xor\ C_{i-1}$

IV. RESULTS

This section reveals the simulation results, delay and area comparison of 16×16 bit Vedic multipliers and proposed 32×32 bit Vedic multiplier.

Fig-4.1 shows the simulation results for 16×16 bit Vedic multipliers. It shows the output for maximum value of inputs i.e. **a** =65535 **b**=65535 and then the output becomes s=4294836225

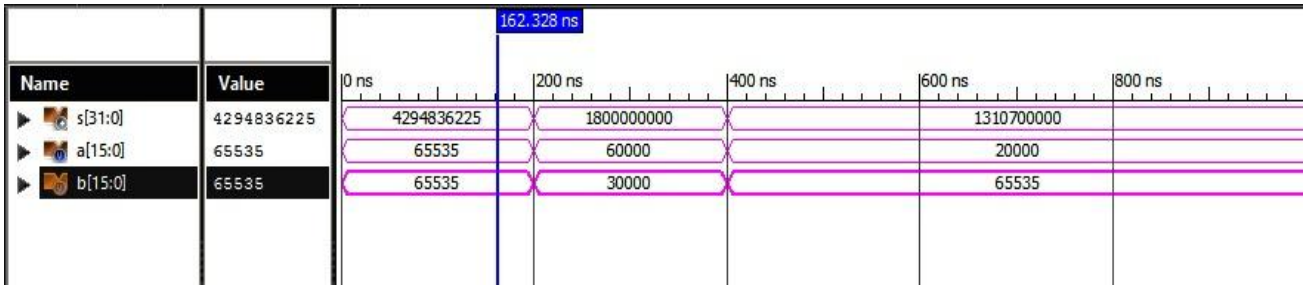

Fig-4.1: Simulation result of 16×16 bit Vedic multipliers

The table-I illustrates the area and delay comparison of 16x16 Vedic multipliers. The delay of the existing Vedic multiplier is 30.193ns and that of modified multiplier using the koggestone adder is 26.562ns. But the modified multiplier designed using modified ripple carry adder produces the delay of 24.561ns. It indicates that there is 18.65% and 7.53% reduction in the delay of modified multiplier using the modified RCA over existing multiplier and the modified multiplier designed using the KSA respectively. Also there is 14.71% and 14.14% reduction in the area over existing and KSA based multiplier respectively. Hence the modified multiplier designed using modified RCA is used to design the 32x32 bit Vedic multiplier.

Table-I: Comparison of 16 x16 Vedic multipliers

Multiplier	Existing multiplier	Modified multiplier using modified RCA	Modified multiplier using KSA
Delay(ns)	30.193	24.561	26.562
No. of LUTs	605	516	601

Fig-4.2 illustrates the simulation results of the proposed 32×32 bit Vedic multiplier. It works for the maximum value of inputs a=4294967295 b=4294967295 and output is s=18446744065119617025.

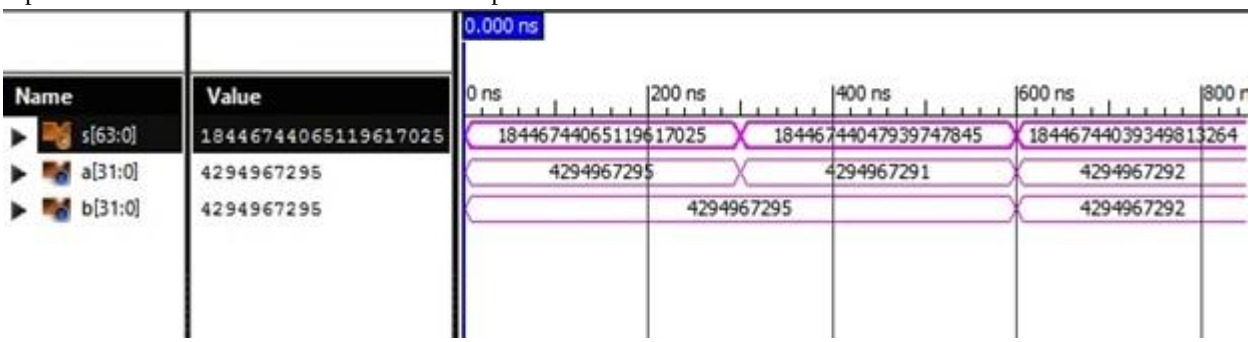

Fig-4.2: Simulation Results of 32x32 bit Vedic Multiplier

The table-II illustrates the area and delay comparison of 32×32 bit multipliers and also the levels of logic in each multiplier. The delay of modified multiplier designed using modified RCA is 40.971ns. If we use the Kogge stone adder instead of ripple carry adder delay will be reduced to 38.63ns. We can find from the table that there is 13.61% reduction in the delay of modified multiplier over the existing multiplier designed using KSA. The modified multiplier designed using Modified RCA requires 2195 slice LUTs where as the modified multiplier designed using the KSA requires 2389 slice LUTs but the levels of logic is less is here.

Table-II: Comparison of 32x32 bit Vedic multipliers

Multiplier	Existing multiplier using 32 bit RCA	Existing multiplier using 32 bit KSA	Modified multiplier using Modified RCA	Proposed Multiplier using KSA
Delay (ns)	50.014	44.719	40.971	38.63
No. of LUTs	2539	2755	2195	2389
Levels of logic	41	39	36	34

V. CONCLUSION AND FUTURE SCOPE

Since multiplication operation is most essential operation in many arithmetic computations, it is required to have a multiplier which is efficient in terms of delay, area and the power consumption. In this project an efficient multiplier is designed to reduce delay and area.

Existing multipliers [1], use the normal ripple carry adders where inputs to the adders are of same length. The problem here is that, if the inputs are of different length, zeros are appended to make them of equal length. The process of appending zeros leads to the increase in the hardware utilization and delay. So to avoid this problem, in this project, ripple carry adders are modified as per the length of inputs. The 8×8 and 16×16 bit multipliers are designed using the modified ripple carry adders. For higher order bit multiplication, ripple carry adders lead to large area and delay even though they are modified. Hence in this project, for 32×32 bit multiplier, Kogge Stone Adder is employed which is the fastest adder for higher order bit addition. In comparison with existing multiplier, results indicate that delay for proposed 32×32 multiplier is reduced from 44.719ns to 38.63ns i.e. 13.61% reduction in delay along with the 13.28% reduction in the area.

Koggestone adders are the fastest adders with more hardware utilization. The delay and area of the multipliers can be further reduced in future if the fastest adders other than Kogge stone adders are designed thereby achieving high speed Vedic multipliers.

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