Volume 6, Issue 6, June 2016 ISSN: 2277 128X
International Journal of Advanced Research in Computer Science and Software Engineering
Research Paper
Available online at: www.ijarcsse.com

A Novel 1V- 0.95ppm/°C Curvature-Compensated CMOS Bandgap Reference

Mehdi Babaei
Master Student of Electrical Engineering,
University of Guilan, Rasht, Iran

Ali Heidari
Department of Electrical Engineering,
University of Guilan, Rasht, Iran

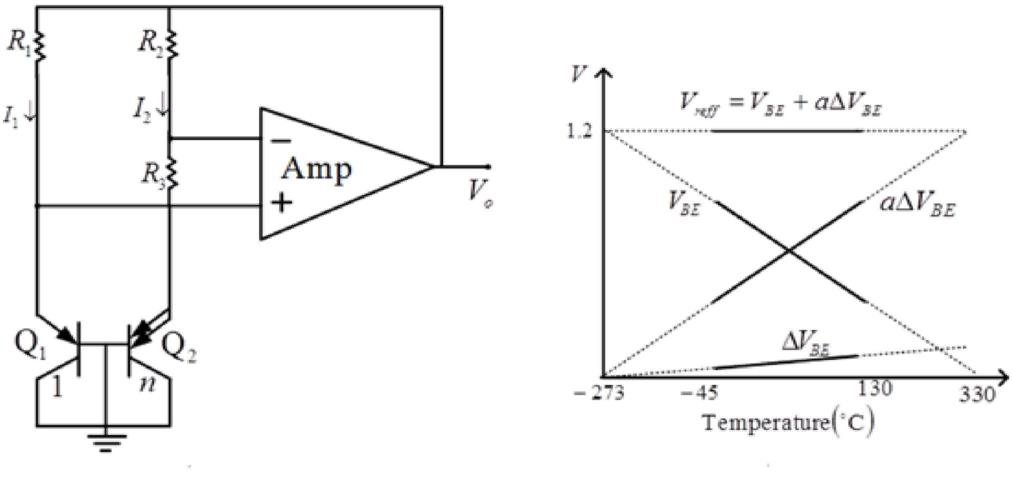
Abstract—This paper proposes a novel CMOS bandgap reference (BGR) with high-order curvature compensation. Basic concept behind this new curvature compensation was to utilize the nonlinear dependence of the base current on temperature to generate a nonlinear voltage and use it to compensate for the higher order term. The mechanism of the proposed curvature-compensation technique is analyzed thoroughly and the corresponding BGR circuit was implemented in standard CMOS 0.18 µm technology. The Simulation results show that the proposed BGR achieves 0.95 ppm/°C over the temperature range of –30°C to 130°C at 1 V supply voltage. It is suitable for low-powerapplications requiring references with high precision.

Keywords—Low voltage bandgap reference, curvature compensation, temperature coefficient.

I. INTRODUCTION

PRECISION bandgap voltage references are criticalbuilding blocks for a variety of analogue and mixedsignal electronic devices such as data converters, PWM controllers,oscillators, operational amplifiers, linear regulators andPLLs [4]. Undoubtedly the reference voltage accuracy plays a significantpart in determining the performance of all subsequentcircuits, which depend on an accurate and stable reference. For example, high precision ADCs, which are widely used ininstrumentation and measurement systems, require a high precisionvoltage reference if the large number of bits in modernprocessing systems are to have any significance. Temperaturedependent drift of the reference voltage is undoubtedly one ofthe key issues in BGR design.In order to achieve high-precision low-voltage CMOS reference,several curvature compensation techniques have beendeveloped [3]–[14].In most bandgap topologies the voltage of a diodeconnectedbipolar transistor is chosen to be the main elementwith well-characterized, temperature-dependentas shown in Fig. 1. In this case, the base-emitter voltage is related characteristics to the bandgap energy and is to be used as part of the compensationmethod [4].

In this paper, the design of a low voltage bandgap reference is discussed. To compensate for the curvature of the output voltage with respect to temperature,Non-linear characteristic h_{FE} in bipolar transistor and base current and resistance added to the base are used.Section II givesa brief description for the low voltage bandgap reference. In Section III, a novellow voltage BGR is proposed and analyzed. In Section IV,the simulation results and in Section V, a comparison between this work andprevious works are presented.At last, Section V is the conclusion.



(a) (b)

Fig.1: An example of Bandgap Reference [1].

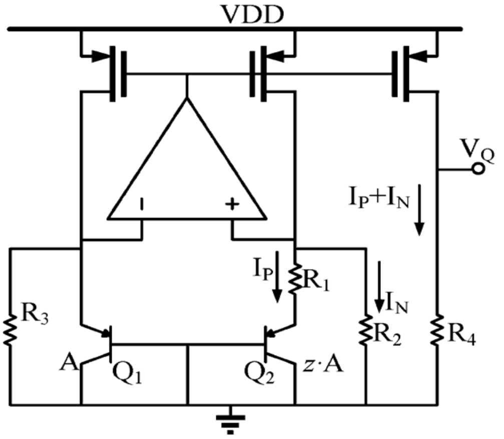


Fig.2: Traditional low-voltage BGR [3].

II. TRADITIONAL LOW-VOLTAGE BANDGAP REFERENCE

Traditional low-voltage BGR is a bipolar transistor (BJT)BGR (Fig. 2) [3], whose positive first-order coefficient is created by the differencein base-emitter voltage,ΔV_{BE} of two BJTs loaded proportionalcurrent density and whose negative first-order coefficientis created byV_{BE}. Most of low-voltage BGRs [3], [4], [11],[12] use BJT BGR as a core element, as shown in Fig. 2. Thetwo voltages,ΔV_{BE}andV_{BE}, are converted to two currents,$I_P$andI_N, by dividing resistors,R_1 and R_2. Thereference voltageV_Q is generated by the sumof$I_P$andI_N, multipliedby the output resistorR_4 .$V_Q$is given by:

$$V_Q = R_4(I_P + I_N) = \frac{R_4}{R_2}V_{EB} + \frac{R_4}{R_1}\frac{kT}{q}\ln z \qquad (1)$$

wherez is the ratio of emitter area ofQ_2 toQ_1, $V_{BE}$is the base-emitter voltage and is given by:

$$V_{BE}(T) = V_{G0}\left(1-\frac{T}{T_r}\right) - cT^2 + \frac{T}{T_r}V_{BE}(T_r) - (\eta - m)\frac{kT}{q}\ln\left(\frac{T}{T_r}\right) \qquad (2)$$

where$T_r$is specified reference temperature, T is absolute temperature,η=4-δ, δ is the order of temperature dependenceof carrier mobility, m is the order of temperature dependence ofcollector current, $V_{G0}$is the bandgap voltage in absolute temperature. Parameter min (2) is equal to 1, sinceI_C is Proportional toAbsolute Temperature (PTAT). resistances of R_1 and R_2 are scaled to eliminate the first order terms [3].The temperature behavior of$V_Q$is shown in Fig. 3.

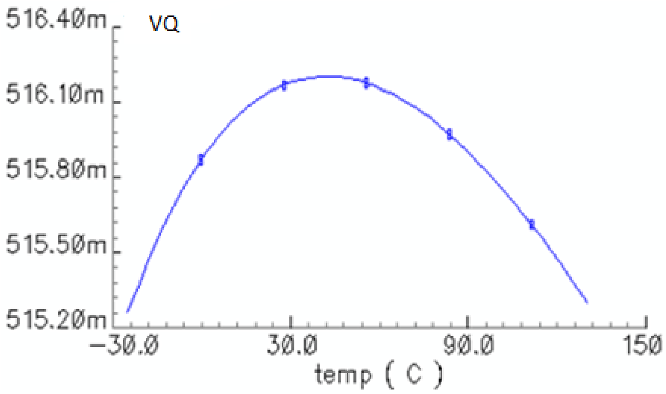


Fig.3: The temperature behavior of $\boldsymbol{V_Q}$

III. PROPOSEDLOW-VOLTAGE BANDGAP REFERENCE

The architecture of the proposed current mode BGR with new curvature compensation technique is illustrated in Fig.4. Basic concept behind this new curvature compensation was to utilize the nonlinear dependence of the base current on temperature to generate a nonlinear voltage and use it to compensate for the higher order term of (2). We can write:

$$I_B(T) = \frac{I_C(T)}{h_{FE}(T)} = \frac{\dfrac{[(\frac{kT}{q})\ln N]}{R_1}}{h_0 + h_1T + h_2T^2 + h_3T^3} \qquad (3)$$

$$I_B(T) = I_{B0} + I_{B1}T + I_{B2}T^2 + I_{B3}T^3 \qquad (4)$$

$$R_{Comp}(T) = R_0[1 + TC_1(T - T_r) + TC_2(T - T)^2] \qquad (5)$$

$$V_B = R_{Comp}(T).I_B(T) \qquad (6)$$

$$V_B = R_{Comp0}(V_{B0} + V_{B1}T + V_{B2}T^2 + V_{B3}T^3) \quad (7)$$

Where $V_{B1} < 0$, $V_{B2} > 0$, $V_{B3} < 0$

$$V_{ref} = R_O\left(\frac{V_{EB1} + V_B}{R_2} + \frac{\frac{kT}{q}\ln N + V_B}{R_1}\right) \quad (8)$$

We find that V_B and V_{BE} have opposite second-order and third-order temperature coefficient from above discussion. It is obvious that by adding (2) , (7) by appropriate weight in (8), the second order temperature coefficient can be eliminated and the third-order temperature coefficient can be partly canceled simultaneously.

TheOP-AMP, is key element. We must ensure that it work in linear amplification state over the whole range of temperature. From Fig. 4, it is obvious that the common-mode input voltage of OP is equal toV_{BE} which varies from about800 mV to 300 mV at temperature–30°C to 130°C.The circuit need to work with the supply voltageas low as 1 V. Ifa folded cascode amp with PMOS differential input is used ,the common-mode input voltage of OP must be lower than$V_{DD} - V_{SG,PMOS} - V_{OD}$and if NMOSinput stage is used, the common-mode input voltage of OP must be higher than $V_{GS,NMOS} + V_{OD}$. Unfortunately, the common-mode input voltage of OP, does not match withV_{BE} at the temperature range of –30°C to 130°C at 1 V supply voltage. For this reason, we have to use Rail to Rail OP-AMP as shown in Fig. 5[1],[9]. For this OP-AMP the common-mode input voltage, is GND to V_{DD}.

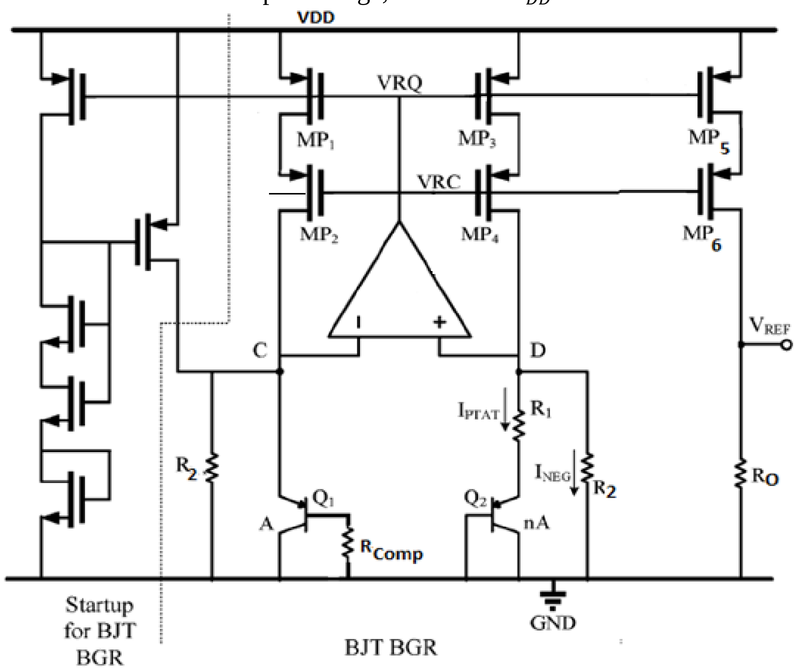


Fig.4: Proposed low voltage BandgapReferene.

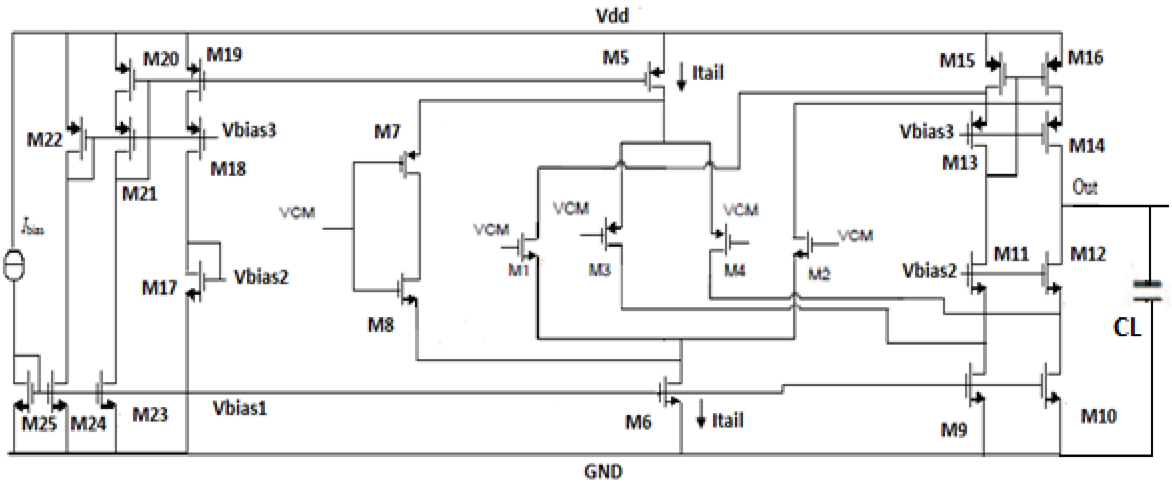


Fig.5: Used Rail to Rail OP-AMP

IV. SIMULATION RESULTS

The simulation result for output voltage in proposed low voltage BandgapReferene, is illustrated in Fig.6. The Simulation results show that the proposed BGR achieves very stable output over the temperature range of –30°C to 130°C at 1 V supply voltage. The total curvature is about 0.07mV which is equivalent to 0.95 ppm/°C. It is suitable for low-power applications requiring references with high precision.Variation of output reference voltage respect tosupply voltage, is illustrated in Fig.7.This result also shows the variation of about 0.03mV over the variation of supply voltage from 1V to 2V.

More details of the designed circuit and comparison with other work is also shown in Table 1.

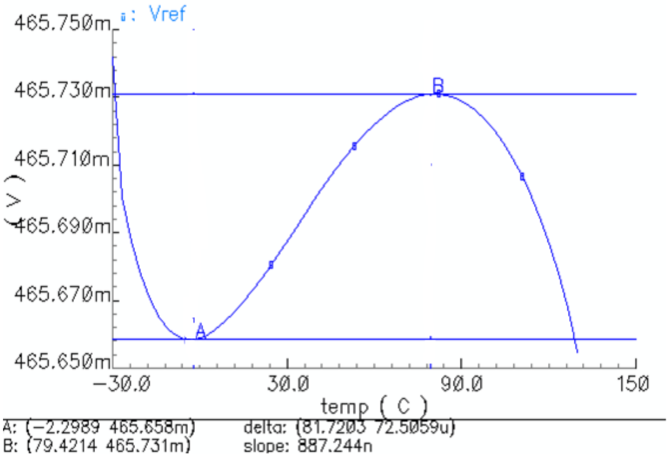


Fig.6: simulation result for output voltage in proposed BGR

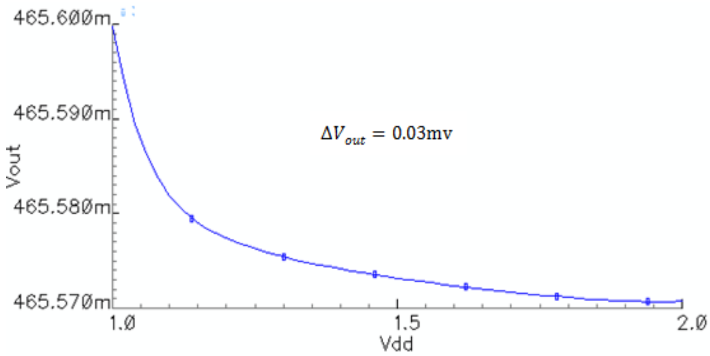


Fig.7:Variation of output reference voltage respect to supply voltage

Table I. Comparison of This Work With Previous Works

References	Technology	Supply voltage (V)	Temp. Coefficient (ppm/°C)	Temperature Range (°C)	Supply Current (µA)	Year Reported
[3]	0.18µm CMOS	1.2	4.9	-40 to 120	36	2014
[4]	0.35µm CMOS	2.5	3.9	-15 to 150	38	2012
[5]	0.18µm CMOS	1.5	2.7	-55 to 125	11.2	2014
[6]	0.18µm CMOS	1.2	2.3	-10 to 110	5	2015
[7]	0.18µm CMOS	1.2	4.2	-40 to 120	-	2015
[8]	0.18µm CMOS	1.3	4.1	-55 to 125	4.3	2015
This Work	0.18µm CMOS	1	0.95	-30 to 130	42	2016

V. COMPARISON WITH PREVIOUS WORKS

A comparison between this work and prior art design isshown in Table I. FromTable I, it is very clear that the proposed circuit has abetter temperature coefficient than all other state of the art bandgapreference over a wide temperature range.In addition to low temperature coefficient, this BGR canprovide a stable output over a range of supplyvoltage from 1 to 2 V.

VI. CONCLUSIONS

A low voltage CMOS bandgap reference withnovel curvature compensation scheme has been presented.The output reference voltage is 465 mV.Higher order temperature compensation is achieved byutilizing the temperature dependence of the base current ina BJT. The temperature coefficient of proposed circuit is only 0.95 ppm/°Cwith temperature ranging from -30°C to 130°C .The variation of the BGR output is less than 0.03mVwhen the supply voltage varies from 1 V to 2V due to its immunityfrom the supply voltage variation, achieved by themodified rail to railOP-AMP.

REFERENCES

[1] BehzadRazavi (2001). Design of Analog CMOS Integrated Circuits, ,McGraw-Hill

[2] Wang, G. (2005). CMOS bandgap references and temperature sensors and their applications, TU Delft, Delft University of Technology.

[3] Ma, B. and F. Yu (2014). "A Novel 1.2–V 4.5-ppm/° C Curvature-Compensated CMOS Bandgap Reference." IEEE Transactions on Circuits and Systems I: Regular Papers, 61(4): 1026-1035.

[4] Andreou, C. M., S. Koudounas, et al. (2012). "A novel wide-temperature-range, 3.9 ppm/C CMOS bandgap reference circuit." IEEE Journal of Solid-State Circuits, 47(2): 574-581.

[5] Ghosh, S. (2014). A Novel Temperature Stable Current Mode Bandgap for Wide Range of Supply Voltage Variation. Electronic System Design (ISED), Fifth International Symposium on, IEEE

[6] Abbasi, M. U., G. Raikos, et al. (2015). A high PSRR, ultra-low power 1.2 V curvature corrected Bandgap reference for wearable EEG application. IEEE 13th International New Circuits and Systems Conference (NEWCAS).

[7] Duan, Q. and J. Roh (2015). "A 1.2-V 4.2-High-Order Curvature-Compensated CMOS Bandgap Reference." IEEE Transactions on Circuits and Systems I: Regular Papers, 62(3): 662-670.

[8] Wang, B., M. K. Law, et al. (2015). "A Precision CMOS Voltage Reference Exploiting Silicon Bandgap Narrowing Effect." IEEE Transactions on Electron Devices, 62(7): 2128-2135.

[9] Lin, Y. (2010). A NEW ARCHITECTURE OF CONSTANT-gm RAIL-TO-RAIL INPUT STAGE FOR LOW VOLTAGE LOW POWER CMOS OP AMP, The Ohio State University.

[10] H. Banba, H. Shiga, A. Umezawa, T. Miyaba, T. Tanzawa, S. Atsumi,and K. Sakui, "A CMOS bandgap reference circuit with sub-1-V operation,"*IEEE J. Solid-State Circuits*, vol. 34, no. 5, pp. 670–674, May 1999

[11] G. De Vita and G. Iannaccone, "A sub-1-V, 10 ppm C, nanopowervoltage reference generator," *IEEE J. Solid-State Circuits*, vol. 42, no. 7, pp. 1536–1542, Jul. 2007.

[12] Ker, M.-D. and J.-S. Chen (2006). "New curvature-compensation technique for CMOS bandgap reference with sub-1-V operation." IEEE Transactions on Circuits and Systems II: Express Briefs, 53(8): 667-671

[13] Leung, K. N., P. K. Mok, et al. (2003). "A 2-V 23-μA 5.3-ppm/° C curvature-compensated CMOS bandgap voltage reference." IEEE Journal of Solid-State Circuits, 38(3): 561-564.

[14]] Li, J.-H., X.-b. Zhang, et al. (2011). "A 1.2-V piecewise curvature-corrected bandgap reference in 0.5 m CMOS process." IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 19(6): 1118-1122.