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Reducing Static Leakage in Soft Error Tolerant SRAM Cell

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Abstract: Soft error is a major issue in modern VLSI circuits. It occurs when a charged particle strikes at a node of the circuit. With technology scaling soft error has become a reliability concern in memory circuits. In this paper we have analyzed and optimized the Quattro 10T cell for high SNM, after which we have propose a technique to reduce power consumption of the cell by minimizing the leakage currents in the cell. The cell is capable of working at voltage supply as low as 0.3v. The proposed cell is designed at 90nm technology node and uses high threshold transistor to control leakage. The design is based on Quattro 10T cell which is soft error robust.

Key words: Soft error, SRAM, SNM, Static Leakage.

I. INTRODUCTION

Radiation tolerance in VLSI circuits is a basic requirement not only in radiation prone environments but even in normal environments also, due to small feature size which has changed the behavior of circuits drastically. Aggressive scaling in sub-micron and deep submicron technologies with reduction in supply voltage critical charge has resulted in significant improvement in power consumption and performance in terms of speed [1]. However reduced feature size and supply voltage has made circuits more sensitive to external radiation. Thus, low energy particles can cause permanent damage or flip in logic value of circuits due to small critical charge at nodes of the circuits. This is making memory cells more sensitive to alpha particles and atmospheric neutrons.

The paper focuses on development of soft error tolerant SRAM cell with low static leakage as static leakage is a considerable part of total power in deep sub micron technology, especially in memory circuits as they remain in steady state in most of the time during operation. The objective has been achieved by conducting study of different soft error hardened cells also including cells customized only for FPGA's. Then a quad node 10T SRAM [2] has been selected and thoroughly analyzed and optimized further in terms of SNM. The optimized cell is then modified to achieve low leakage by adding a base transistor with high $V_{th.}$ The rest of the paper is organized as follows. Section II describes the concepts of soft error, SNM, leakage and hardened cells proposed till now. The SNM optimization and leakage results are shown in section III. In the next section the proposed cell is presented with results and the last section wraps up with the conclusion.

II. CONCEPT AND RELATED WORK

1. *Soft Error*

Soft error is caused when a neutron or alpha particle strikes at the junction of a transistor, it leads to generation of electron hand hole which results in a current flow and development of charge. This is called single event transient (SET), when logic value stored at the node is flipped due to SET it is called single event upset (SEU). It is called soft error because it is not permanent and results in logical fault in the system. It is shown in[4] that if soft error is left uncorrected then it leads in failure rate higher than all other reliability mechanisms combined. It is measured in terms of failure in time (FIT) defined as one failure in million hours estimated by proportionality[3].

$SER \alpha N_{flux} X A_{node} X e^{(-Qcric/Qs)}$

Where N_{flux} is the intensity of neutron flux. A_{node} is the area the node and Q_s is the charge collection efficiency.
Ways to represent SET in terms of current pulse to ease up simulation have been proposed in different papers.

2. *Static Noise Margin (SNM)*

SNM of a SRAM cell is a stability metric of the cell it is required to be more in soft error hardened circuits. The value of SNM for basic 6T cell is obtained by drawing VTC's of each individual inverter and overlapping them. The side of biggest possible square in eye of VTC gives value of SNM. There is no conventional command to calculate SNM of a cell directly in tool so we have used a technique of coordinate rotation discussed in [4] for calculation of SNM of different cells.

3. *Static Leakage*

Leakage is a major consideration in memory circuits as a large part of memory array is left in standby mode and is suppose to retain its stored value. Leakage is divided as follows. First leakage component is sub-threshold leakage and the second component is junction leakage which is further divided into source-body and drain-body leakage. The third

leakage is gate leakage which is divided into gate-body, gate-source and gate-drain leakage. The sub-threshold leakage contributes the most to leakage and other leakage components are negligible in comparison to sub-threshold leakage [5].

The soft error hardened cells proposed till now include asymmetric 6T SRAM cell for FPGA [6], stacked NMOS/PMOS cells, dual interlocked cell (DICE) [7], and Quatro-10T cell [2]. We have selected the last one for further analysis and optimization because unlike others this cell provides differential read/write capability and high tolerance to soft error at 10 transistors and leakage in this cell is lower than DICE.

III. SNM OPTIMIZATION

The optimization is carried out on quad node 10T cell by changing the cell ratio, pull-up ratio and pull-up ratio II of the standard cell shown in fig.1. The cell ratio has been increase to elevate the SNM of the cell.

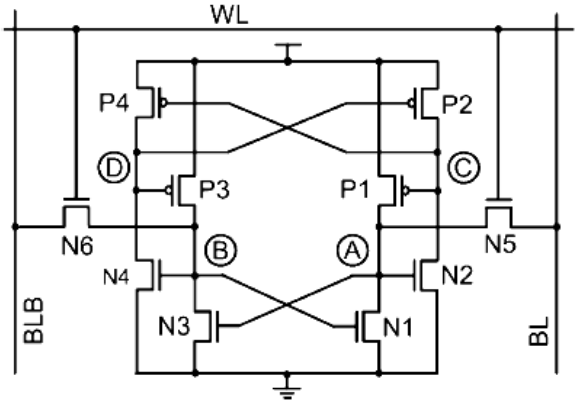

Fig. Quatro-10T cell

The formulas and range of values for different ratios are given in table.1.

Table.1. Ratios involved in cell design

Ratio	Formula	Value
Cell ratio	(W_{N1}/L_{N1}) / (W_{N5}/L_{N5})	1.5-1.7
Pulllup Ratio 1	(W_{P1}/L_{P1}) / (W_{N5}/L_{N5})	1
Pullup Ratio 2	(W_{P4}/L_{P4}) / (W_{N4}/L_{N4})	<0.75

The graph show a comparison of SNM of optimized and privious design at different supply voltages ranging from 0.3V to 1V.

Result of SNM calculation using technique of coordinate rotation [4] is shown in the figure given below. The upper plot shows the difference between the 2 rotated VTC's. Difference gives the value of diagonal of largest square in the eye of VTC, which is futher used to calculate the side of the square.

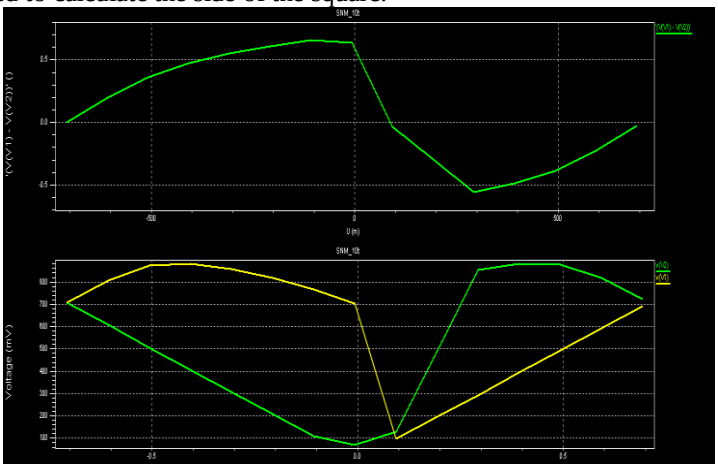

Fig. SNM calculation

The optimized cell shows better SNM results as it has been optimized to get increased static noise margin. But it also increases the static leakage in the cell to a little extent in comparison to the previously proposed design. To reduce leakage we have proposed a new technique which is explained in next section.

IV. LEAKAGE OPTIMIZATION

In order to reduce leakage we have propose a new technique in which a base transistor has been added to the source of driver NMOS transistors of the cell. The base transistor is a high threshold (V_{th}) transistor with a threshold 1.5-2 times higher than threshold of normal transistors. The gate high V_{th} NMOS device is connected to the word line and activates only during read and writes access and it is off during all other times reducing the sub-threshold leakage in the cell.

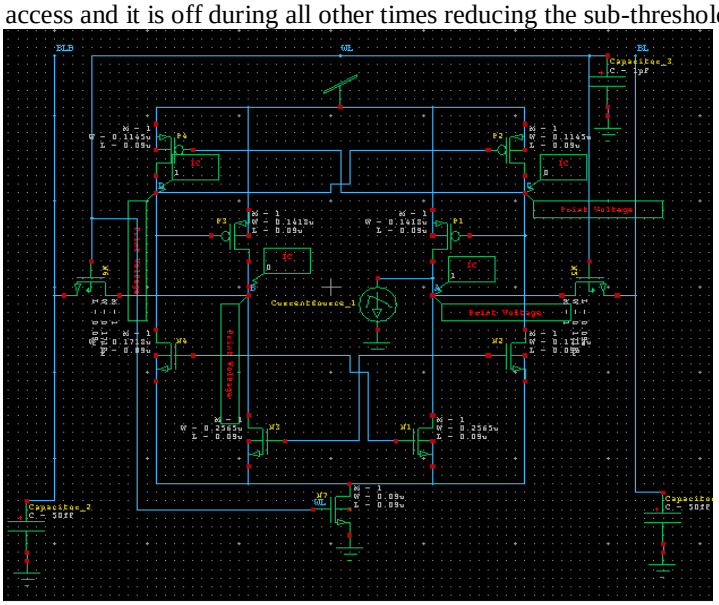

Fig. Proposed cell with setup to simulate single event transient

Figure 4 shows the low leakage cell with a base transistor connected. The cell also shows a current source connected at node A to simulate the SET by providing a pulse of current. The results of simulation of SET are shown in fig.5

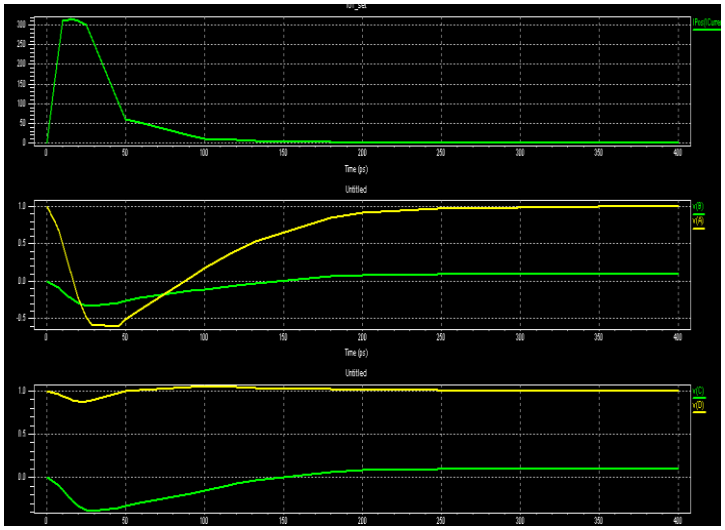

Fig. Recovery from SET

The first plot shows the current pulse applied at node A with peak amplitude of 315µA. The second plot shows voltages of nodes A and B (yellow A, Green B) and third plot shows voltages of nodes C and D (yellow D, green C). As the current pulse is applied the voltage of node A drops first and then recovers due to feedback action of node D. it shows that the leakage optimization hasn't affected the soft error tolerance of the cell.

V. CONCLUSION

The previously proposed quarto-10T cell has been optimized for high SNM with an increase of 0.143V at 1V and the increase in leakage has been compensated by using a base transistor which can be shared by all the cells in a word to increase density. Sharing of base transistor requires proper sizing of the transistor to sink required amount of current.

REFERENCES

[1] Tegze.P.Haraszti "CMOS memory circuits" Kulwer Academic Publishers, Print ISBN 0-792-37950-0

[2] S. Jahinuzzaman, D. Rennie, and M. Sachdev, "A soft error tolerant 10t sram bit-cell with differential read capability," *Nuclear Science, IEEE Transactions on*, vol. 56, no. 6, pp. 3768 –3773, dec. 2009.

[3] Balkaran S. Gill1, Chris Papachristou, and Francis G. Wolff "A New Asymmetric SRAM Cell to Reduce Soft Errors and Leakage Power in FPGA"

[4] Evert Seevinck "Static-Noise Margin Analysis of MOS SRAM Cells" IEEE Journal of solid state circuits, Vol. SC-22, NO. 5, october 1987

[5] A. Islam and M. Hasan, "Leakage Characterization of 10T SRAM Cell" IEEE Transactions on electron devices Vol. 59, NO. 3, march 2012

[6] Balkaran S. Gill1, Chris Papachristou, and Francis G. Wolff "A New Asymmetric SRAM Cell to Reduce Soft Errors and Leakage Power in FPGA"

[7] T. Calin, M. Nicolaidis, and R. Velazco, "Upset hardened memory design for submicron CMOS technology," *IEEE Trans. Nucl. Sci.*, vol. 43, no. 6, pp. 2874–2878, Dec. 1996.

[8] F. Ootsuka *et al.*, "A novel 0.25nm full CMOS SRAM cell using stacked cross couple with enhanced soft error immunity," in *Proc. Int. Electron Devices Meeting*, 1998, pp. 205–208.

[9] Zhang.K "SRAM design on 65-nm CMOS technology with dynamic sleep transistor for leakage reduction" Solid-State Circuits, IEEE Journal of (Volume:40 , Issue: 4), april 2005.

[10] J. M. Rabaey, A. Chandrakasan, and B. Nikolic, *Digital Integrated Circuits: A Design Perspective*. Upper Saddle River, NJ: Prentice-Hall, 2002, pp. 658–661.

[11] S. M. Jahinuzzaman, M. Sharifkhani, and M. Sachdev, "An analytical model for soft error critical charge of nanometric SRAMs," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 17, no. 9, pp. 1187–1195, Sep. 2009

