



Review Paper on Memory less 1-D Discrete Wavelet Transform

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Abstract—Conventional distributed arithmetic (DA) is popular in field programmable gate array (FPGA) design, and it features on-chip ROM to achieve high speed and regularity. In this paper, we describe high speed area efficient 1-D discrete wavelet transform (DWT) using 9/7 filter based new efficient distributed arithmetic (NEDA) Technique. Being area efficient architecture free of ROM, multiplication, and subtraction, NEDA can also expose the redundancy existing in the adder array consisting of entries of 0 and 1. This architecture supports any size of image pixel value and any level of decomposition. The parallel structure has 100% hardware utilization efficiency.

Keywords: - 1-D Discrete Wavelet Transform (DWT), NEDA, Low Pass Filter, High Pass Filter, Xilinx Simulation.

I. INTRODUCTION

The well-known image coding standards, namely, MPEG-4 and JPEG2000 have adopted 1-D DWT as the transform coder due to its remarkable advantages over the other transforms. For lossy and lossless compression, Daubechies 9/7 orthogonal filter is used as the default wavelet filter in JPEG 2000. Efficient implementation of 1-D DWT using 9/7 filters in resource-constrained hand-held devices with capability for real-time processing of the computation-intensive multimedia applications is, therefore, a necessary challenge. Multiplier-less hardware implementation approach provides a kind of solution to this problem due to its scope for lower hardware-complexity and higher throughput of computation.

Several parallel and pipeline systems that meet the computational requirements of the discrete wavelet transform have been proposed. Some of them need multiprocessor to implement it and the system is complex, time consuming, and costly [1]. The Field programmable gate array (FPGA) provides us a new way to digital signal processing [2].

Several designs have been proposed for the multiplier, multiplier-less implementation of 1-D DWT based on the principle of multiplier based design (MBD) distributed arithmetic (DA) canonic signed digit (CSD), [1]–[3]. The structure of distributes the bits of the fixed coefficients instead of the bits of input samples. Consequently, the adder-complexity of the structure of depends on the DA-matrix of the fixed coefficients [2].

Canonic signed digit (CSD) are popular for representing a number with fewest number of non-zero digit. The CSD representation of a number contains the minimum possible number of nonzero bits, thus the name canonic. The CSD representation of a number is unique and CSD numbers cover the range $(-4/3, 4/3)$, out of which the value in the range $\{-1, 1\}$ are of greatest interest.

Martina *et al* [5] have approximated the 9/7 filter coefficients and performance of a hardware implementation of the 9/7 filter bank depends on the accuracy of coefficients representation. By that approach, they have significantly reduced the adder-complexity of the 9/7 DWT. Gourav *et al* [7] have suggested an LUT-less DA-based design for the implementation of 1-D DWT. They have eliminated the ROM cells required by the DA-based structures at the cost of additional adders and multiplexors.

Some of them need Rom to implement it and the system is complex, time consuming, and costly [4] The adder-complexity of this structure is significantly higher than the other multiplier-less structures. In this paper, we have proposed an efficient scheme to derive NEDA-based bit-parallel structures, for low-hardware and high-speed computation DWT using 9/7 filters [4].

The remainder of the paper is organized as follows: New efficient distributed arithmetic based computation of 1-D DWT using 9/7 filter is presented in Section II. The proposed structures are presented in Section III. Hardware and time complexity of the proposed structures are discussed and compared with the existing structures in Section IV. Conclusion is presented in Section V.

II. NEW EFFICIENT DISTRIBUTED ARITHMETRIC (NEDA)

Let us consider the following sum of products [4]:

$$R = \sum_{k=1}^L X_k \times Y_k \quad (1)$$

Where X_k are fixed coefficients and they Y_k are the input data words. Equation (1) can be expressed in the form of a matrix product as:

$$R = [X_1 \quad X_2 \quad \dots \quad X_L] \begin{bmatrix} Y_1 \\ Y_2 \\ \vdots \\ Y_L \end{bmatrix} \quad (2)$$

Both X_k and Y_k are in two's complement format. The two's complement representation of X_k may be expressed as

$$X_k = -X_k^M 2^M + \sum_{i=N}^{M-1} X_k^i 2^i \quad (3)$$

Where $X_k^i = 0$ or 1 , and $i = N, N+1 \dots M$ and X_k^M is the sign bit and X_k^N is the least significant bit (LSB).

Equation (3) can be expressed in matrix form as:

$$X_k = \begin{bmatrix} 2^N & 2^{N+1} & \dots & 2^M \end{bmatrix} \begin{bmatrix} X_k^N \\ X_k^{N+1} \\ \vdots \\ -X_k^M \end{bmatrix} \quad (4)$$

Similarly Y_k can be represented in two's complemented format as:

$$Y_k = -Y_k^X 2^X + \sum_{i=W}^{X-1} Y_k^i 2^i \quad (5)$$

Where $Y_k^i = 0$ or 1 , and $i = W, W+1, \dots, X$ and Y_k^X is the sign bit and Y_k^W is the least significant bit (LSB).

Now on combining equations (1) and (3), we get-

$$R = -(R^M \cdot 2^M) + \sum_{i=N}^{M-1} (R^i \cdot 2^i) \quad (6)$$

Where

$$R^i = \sum_{k=1}^L X_k^i Y_k, \quad i = N, N+1 \dots M$$

III. PROPOSED ARCHITECTURE

In this paper, we have proposed a high speed area efficient multiplier-less 1-D 9/7 wavelet filters based NEDA technique. 9/7 wavelet filters coefficient i.e. 9 low-pass and 7 high-pass wavelet filters coefficient are given in table1. We multiply the filter coefficients by 128 for simplification. The mathematical calculation for 1-D high pass filter output is explained by an example.

Table 1: Show high-pass and low-pass wavelet filters coefficient.

	Wavelet filters coefficients	Multiplied by 128	8 bit binary representation with 2's complement of negative no.
h_0	0.60294901823	77	01001101
h_1	0.26686441184	34	00100010
h_2	-0.07822326652	-10	11110110
h_3	-0.01686411844	-2	11111110
h_4	0.026748757410	3	00000011
g_0	0.55754352622	71	01000111
g_1	-0.29563588155	-38	01011010
g_2	-0.02877176311	-4	11111100
g_3	0.045635881557	6	00000110

Where h_0, h_1, h_2, h_3, h_4 are the Low pass filter coefficients and g_0, g_1, g_2, g_3 are the High pass filter coefficients.

If we take the high pass coefficients g_0, g_1, g_2 and g_3 multiply by r_1, r_2, r_3 and r_4 then we get the High pass output Y_H of the 9/7 filter as [6]:

$$Y_H = \begin{bmatrix} g_0 & g_1 & g_2 & g_3 \end{bmatrix} \begin{bmatrix} r_1 \\ r_2 \\ r_3 \\ r_4 \end{bmatrix} \quad (7)$$

Where

$$r_1 = Y(n) + Y(n-6) \quad r_2 = Y(n-1) + Y(n-5)$$

$$r_3 = Y(n-2) + Y(n-4) \quad r_4 = Y(n-3)$$

Let $r_1=1, r_2=2, r_3=3, r_4=4$ then

$$Y_H = [71 \quad -38 \quad -4 \quad 6] \begin{bmatrix} 1 \\ 2 \\ 3 \\ 4 \end{bmatrix} = 7 \quad (8)$$

Now if we implement this with NEDA then

$$Y_H = [01000111 \quad 11011010 \quad 11111100 \quad 00000110]$$

$$\begin{bmatrix} r_1 \\ r_2 \\ r_3 \\ r_4 \end{bmatrix} \quad (9)$$

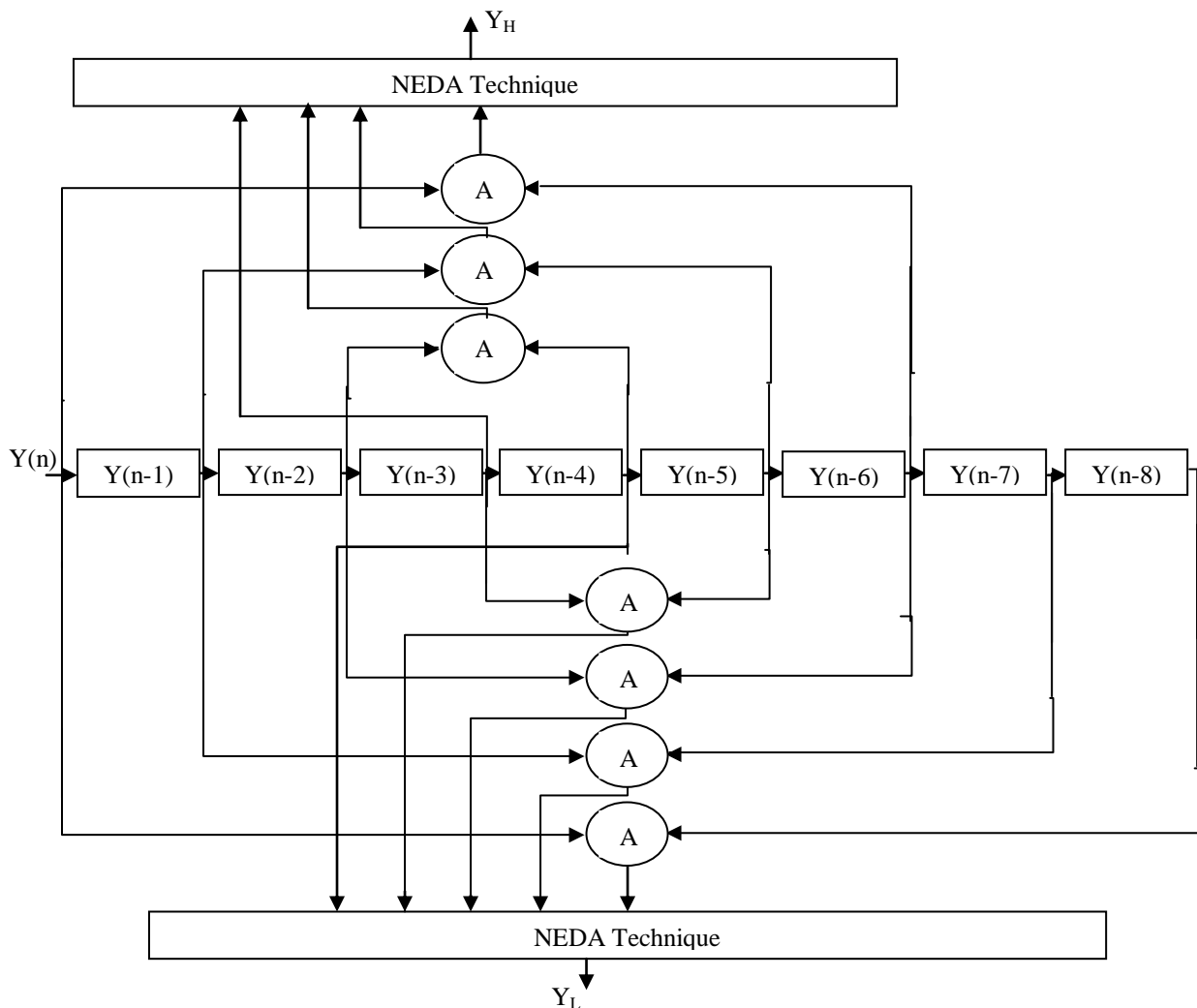


Figure 1: Proposed Multiplier-less 9/7 Wavelet filter using NEDA Technique

Now we can make the DA matrix by the filter coefficients as

$$[B_k] = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 1 & 1 & 0 & 1 \\ 1 & 0 & 1 & 1 \\ 0 & 1 & 1 & 0 \\ 0 & 1 & 1 & 0 \\ 0 & 0 & 1 & 0 \\ 1 & 1 & 1 & 0 \\ 0 & 1 & 1 & 0 \end{bmatrix} \quad (10)$$

$$Y_H = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 1 & 1 & 0 & 1 \\ 1 & 0 & 1 & 1 \\ 0 & 1 & 1 & 0 \\ 0 & 1 & 1 & 0 \\ 0 & 0 & 1 & 0 \\ 1 & 1 & 1 & 0 \\ 0 & 1 & 1 & 0 \end{bmatrix} \begin{bmatrix} r_1 \\ r_2 \\ r_3 \\ r_4 \end{bmatrix} = \begin{bmatrix} r_1 \\ r_1 + r_2 + r_4 \\ r_1 + r_3 + r_4 \\ r_2 + r_3 \\ r_2 + r_3 \\ r_3 \\ r_1 + r_2 + r_3 \\ r_2 + r_3 \end{bmatrix} \quad (11)$$

In Figure 2, apply NEDA techniques step-1 all the input converts' binary number, Step-2 all the binary input applied to sign extension, after than all the sign extension input applied to a adder array so,

$$\begin{aligned} P_1 &= 00001, & P_2 &= 00111 \\ P_3 &= 01000, & P_4 &= 00101 \\ P_5 &= 00101, & P_6 &= 00011 \end{aligned}$$

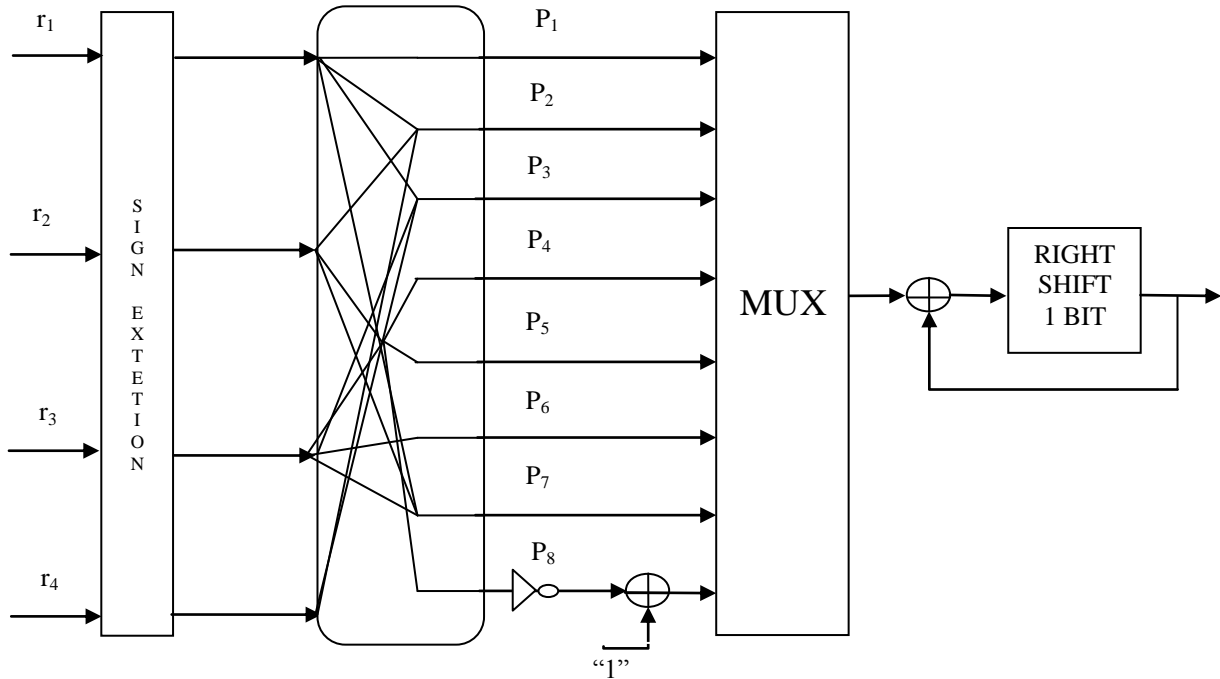


Figure 2: Mathematical calculation of the NEDA Technique of the Low-pass Wavelet Filter Output

$$P_7 = 00110, \quad P_8 = 00101$$

The entire adder array input applied to MUX so, the entire adder array input $m(1)$ right shift 1-bit so

$$\text{MUX}(1) = 0'0111 = Y_p(0)$$

$$\begin{aligned} \text{MUX}(1) \text{ add MUX}(2) &= Y_p(1) \\ &= 0'00001 \\ &= 0 \ 0111 \\ &+ 0 \ 01111 \end{aligned}$$

$$\begin{aligned} \text{Output of the } Y_p(1) \text{ again right shift 1-bit and adds MUX}(3) \text{ so} \\ &= 0'001111 \\ &= 0 \ 1000 \\ &+ 0 \ 101111 \end{aligned}$$

$$Y_p(1) + \text{MUX}(3) = Y_p(2)$$

$$\begin{aligned} \text{Output of the } Y_p(2) \text{ again right shift 1-bit and adds MUX}(4) \text{ so} \\ &= 0'0101111 \\ &= 0 \ 0101 \\ &+ 0 \ 1010111 \end{aligned}$$

$$Y_p(2) + \text{MUX}(4) = Y_p(3)$$

Output of the $Y_p(3)$ again right shift 1-bit and adds MUX(5)

so

$$\begin{aligned}
 &= 0'01010111 \\
 &= 0\ 0101 \\
 &+ 0\ 10100111 \\
 Y_p(3) + \text{MUX}(5) &= Y_p(4) \\
 \text{Output of the } Y_p(4) &\text{ again right shift 1-bit and adds MUX}(6) \\
 \text{so} \\
 &= 0'010100111 \\
 &= 0\ 0011 \\
 &+ 0\ 10000111 \\
 Y_p(4) + \text{MUX}(6) &= Y_p(5) \\
 \text{Output of the } Y_p(5) &\text{ again right shift 1-bit and adds MUX}(7) \\
 \text{so} \\
 &= 0'010000111 \\
 &= 0\ 0110 \\
 &+ 0\ 101000111 \\
 Y_p(5) + \text{MUX}(7) &= Y_p(6) \\
 \text{Output of the } Y_p(6) &\text{ again right shift 1-bit and adds MUX}(8) \\
 \text{so} \\
 &= 0'01010000111 \\
 &= 1\ 1011 \\
 &+ 100000000111 \\
 \text{Total output } Y_p(7) &= 00000000111 = 7 \\
 \text{Carry is rejected.}
 \end{aligned}$$

IV. SIMULATION RESULT

The proposed architecture has very low hardware complexity compared to DA based structures, because DA requires ROM.

In the proposed architecture, calculate the high-pass and low-pass wavelet filter output using NEDA scheme. NEDA does not require ROM. Proposed structure consist only 33 adders, zero mux and 29 registers. In the proposed architecture is better than other architecture in shown the Table 2.

Table 2: Comparison of proposed with existing architectures, Arch.: Architecture, MUL: Multiplier MUX: Multiplex, REG: Register, CP: Cyclic Period

Arch.	MUL	Adder	MUX	Rom	REG	CP
Alam et al. [2]	0	43	9	4	8	12 T _A
Martina et al [5]	0	36	5	4	8	9 T _A
Martina et al. [6]	0	36	4	4	8	6 T _A
Gaurav et al. [7]	0	30	1	4	8	6 T _A
Proposed	0	30	1	0	8	6 T _A

V. CONCLUSION

We propose a novel distributed arithmetic paradigm named NEDA for VLSI implementation of digital signal processing (DSP) algorithms involving inner product of vectors and vector-matrix multiplication. Mathematical proof is given for the validity of the NEDA scheme. We demonstrate that NEDA is a very efficient architecture with adders as the main component and free of ROM (free memory), multiplication, and subtraction. For the adder array, a systematic approach is introduced to remove the potential redundancy so that minimum additions are necessary. NEDA is an accuracy preserving scheme and capable of maintaining a satisfactory performance even at low DA precision.

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