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Vedic Mathematics Applications in DSP: Convolution and De-Convolution

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Abstract— Convolution and Deconvolution is having wide area of application in Digital Signal Processing. As in DSP Convolution and Deconvolution of long sequences is often required in many applications. Convolution helps to estimate the output of a system with arbitrary input, with knowledge of impulse response of the system. Linear systems characteristics are completely specified by the systems impulse response, as governed by the mathematics of convolution. Primary requirement of any application to work fast is that increase the speed of their basic building block. Multiplier and Divider is the heart of convolution and Deconvolution respectively. It is most important but, slowest unit of the system and consumes much time in the system. Many methods are invented to improve the speed of the Multiplier and Divider, amongst all vedic Multiplier and Divider is under focus. Because, of faster working and low power consumption. In this paper the speed of Convolution and Deconvolution module is increased using Vedic multiplier and Divider.

Keywords: Linear Convolution, Deconvolution, Vedic Mathematics, Urdhva Tiryagbhyam sutra, Paravartya sutra, Nikhilam sutra.

I. INTRODUCTION

With the latest advancement of VLSI technology, digital signal processing plays a pivotal role in many areas of electrical engineering. Discrete convolution is central to many applications of Digital Signal Processing and Image Processing. It is used for designing of digital filter and correlation application. However, beginners often struggle with convolution because the concept and computation requires a number of steps that are tedious and slow to perform. The most commonly taught approach is a graphical method because of the visual insight into the convolution mechanism. Graphical convolution is very systematic to compute but is also very tedious and time consuming.

The principal components required for implementation of convolution calculation are adder and multiplier for partial multiplication. Therefore the partial multiplication and addition are bottleneck in deciding the overall speed of the convolution implementation technique. Complexity and excess time consumption are always the major concern of engineers which motivates them to focus on more advance and simpler techniques. Pierre and John have implemented a fast method for computing linear convolution and deconvolution. This method is similar to the multiplication of two decimal numbers and this similarity makes this method easy to learn and quick to compute.

Also to compute deconvolution of two finite length sequences, a novel method is used. This method is similar to computing long-hand division and polynomial division. Since the execution time in most DSP algorithms mainly depends upon the time required for multiplication, so there is a need of high speed multiplier. Now a days, time required in multiplication process is still the dominant factor in determining the instruction cycle time of a DSP chip . Traditionally shift and add algorithm is being used for designing. However this is not suitable for VLSI implementation and also from delay point of view. Some of the important algorithms proposed in literature for VLSI implementable fast multiplication are Booth multiplier, array multiplier and Wallace tree multiplier. Although these multiplication techniques have been effective over conventional ”shift and add” technique but their disadvantage of time consumption has not been completely removed.

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II. VEDIC MATHEMATICS

Vedic mathematics - a gift given to this world by the ancient sages of India. A system which is far simpler and more enjoyable than modern mathematics. The simplicity of Vedic Mathematics means that calculations can be carried out mentally though the methods can also be written down. There are many advantages in using a flexible, mental system. Pupils can invent their own methods; they are not limited to one method. This leads to more creative, interested and intelligent pupils. Vedic Mathematics refers to the technique of Calculations based on a set of 16 Sutras, or aphorisms, as algorithms and their upa-sutras or corollaries derived from these Sutras. Any mathematical problems (algebra, arithmetic, geometry or trigonometry) can be solved mentally with these sutras. Vedic Mathematics is more coherent than modern mathematics.

Vedic Mathematics offers a fresh and highly efficient approach to mathematics covering a wide range - starts with elementary multiplication and concludes with a relatively advanced topic, the solution of non-linear partial differential

equations. But the Vedic scheme is not simply a collection of rapid methods; it is a system, a unified approach. Vedic Mathematics extensively exploits the properties of numbers in every practical application. Vedic mathematics is part of four Vedas (books of wisdom). It is part of Sthapatya- Veda (book on civil engineering and architecture), which is an upa-veda (supplement) of Atharva Veda. It covers explanation of several modern mathematical terms including arithmetic, geometry (plane, co-ordinate), trigonometry, quadratic equations, factorization and even calculus.

His Holiness Jagadguru Shankaracharya Bharati Krishna Teerthaji Maharaja (1884-1960) comprised all this work together and gave its mathematical explanation while discussing it for various applications..Swamiji constructed 16 sutras (formulae) and 16 Upa sutras (sub formulae) after extensive research in Atharva Veda. Obviously these formulae are not to be found in present text of Atharva Veda because these formulae were constructed by Swamiji himself. Vedic mathematics is not only a mathematical wonder but also it is logical. That's why VM has such a degree of eminence which cannot be disapproved. Due these phenomenal characteristic, VM has already crossed the boundaries of India and has become a leading topic of research abroad. VM deals with several basic as well as complex mathematical operations. Especially, methods of basic arithmetic are extremely simple and powerful .

A) Sutras Of Vedic Mathematics

The word Vedic is derived from the word "Veda" which means the store-house of all knowledge. Vedic mathematics is mainly based on 16 Sutras (or aphorisms) dealing with various branches of mathematics like arithmetic, algebra, geometry etc. These Sutras along with their brief meanings are enlisted below alphabetically.

1) (Anurupye) Shunyamanyat – If one is in ratio, the other is zero.
2) Chalana-Kalanabyham – Differences and Similarities.
3) Ekadhikina Parvenu – By one more than the previous One.
4) Ekanyunena Parvenu – By one less than the previous one.
5) Gunakasamuchyah – The factors of the sum is equal to the sum of the factors.
6) Gunitasamuchyah – The product of the sum is equal to the sum of the product.
7) Nikhilam Navatashcaramam Nashotah – All from 9 and last from 10.
8) Paraavartya Yojayet – Transpose and adjust.
9) Puranapuranabyham – By the completion or no completion.
10) Santayana- vyavakalanabhyam – By addition and by subtraction.
11) Shesanyankena Charmin – The remainders by the last digit.
12) Shun yam Saamyasamuccaye – When the sum is the same that sum is zero.
13) Sopaantyadvayamantyam – The ultimate and twice the penultimate.
14) Urdhva-tiryakbhyam – Vertically and crosswise.
15) Vyashtisamanstih – Part and Whole.
16) Yaavadunam – Whatever the extent of its deficiency.

These methods and ideas can be directly applied to trigonometry, plain and spherical geometry, conics, calculus (both differential and integral), and applied mathematics of various kinds. As mentioned earlier, all these Sutras were reconstructed from ancient Vedic texts early in the last century. Many Sub-sutras were also discovered at the same time, which are not discussed here. The beauty of Vedic mathematics lies in the fact that it reduces the otherwise cumbersome-looking calculations in conventional mathematics to a very simple one. This is so because the Vedic formulae are claimed to be based on the natural principles on which the human mind works. This is a very interesting field and presents some effective algorithms which can be applied to various branches of engineering such as computing and digital signal processing.

B) History Of Vedic Mathematics

Ancient Indian sculptures (Vedas) contain Indian system of mathematics which was rediscovered in the early twentieth century. It includes Vedic mathematical formulae which can be applied to various branches of mathematics. The conventional mathematical algorithms are simplified and also optimized by using vedic sutras. Trigonometry, plain and spherical geometry, conics, calculs are one of few areas where these vedic sutras can be applied efficiently. Now-a -days, because of increasing demand of digital signal processing, image processing and other heavy computational applications require faster computation by processor. Higher throughput arithmetic operations are required in these signal processing applications.

Multiplication, division are one of arithmetic operations which require heavy calculations. Traditional methods for doing these operations take a lot of processing time. These traditional methods include array, booth, carry save, Wallace tree, etc. Multiplier architecture based all these methods are not very efficient in terms of speed, area, power. Vedic multiplication involves fewer steps to solve multiplication than traditional multiplication. This helps to achieve optimization at all levels of design of digital systems reducing power consumption. Vedic mathematics based multipliers are efficient in terms of speed, power and area.

III. CONVOLUTION

3.1: 4 bit Vedic Multiplier

The 4x4 Multiplierismadebyusing4, 2x2multiplierblocks. Here, the multiplicands are of bit size (n=4) where as the result is of 8 bit size. The input is broken into smaller chunks of size of n/2 = 2, for both inputs, that is a and b. These

newly formed chunks of 2 bits are given as input to 2x2 multiplier block and the result produced 4 bits, which are the output produced from 2x2 multiplier block are sent for addition to an addition tree.

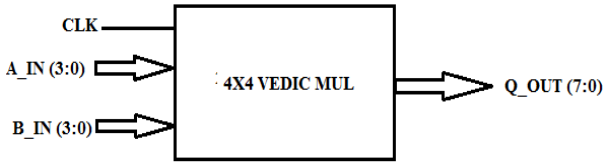


Fig 3.1: 4 bit Vedic Multiplier

For higher no. of bits in input, little modification is required. Divide the no. of bit in the inputs equally in two parts. In this section a novel multiplier architecture based on Urdhva Triyagbhyam Sutra of Ancient Indian Vedic Mathematics is embedded into proposed method of convolution to improve its efficiency in terms of speed and area. This method for discrete convolution using Vedic multiplication algorithm is best introduced by a basic example

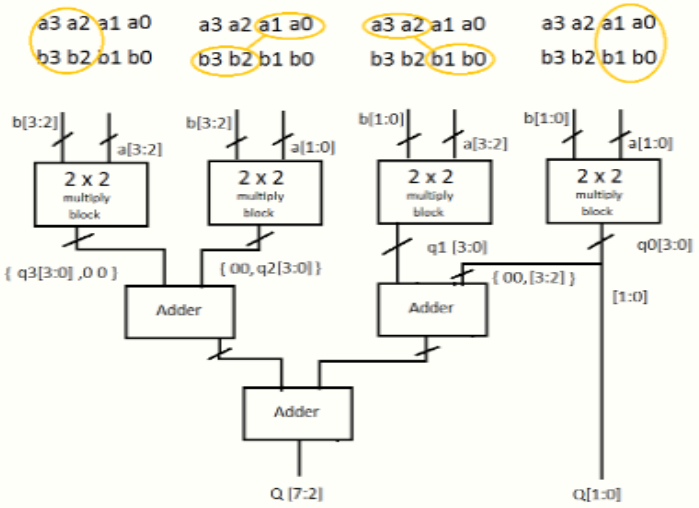


Fig3.2: Block Diagram of 4 bit Vedic Multiplier

In this section a novel multiplier architecture based on Urdhva Triyagbhyam Sutra of Ancient Indian Vedic Mathematics is embedded into proposed method of convolution to improve its efficiency in terms of speed and area. This method for discrete convolution using Vedic multiplication algorithm is best introduced by a basic example.

Among all available multipliers, this paper proposes a systematic design methodology for fast and area efficient digit multiplier based on Vedic Mathematics. In the proposed convolution method the multiplier architecture is based on an algorithm Urdhva Triyagbhyam (Vertical and Crosswise) of Ancient Indian Vedic Mathematics . The use of Vedic Mathematics lies in the fact that it reduces the typical calculations in conventional mathematicsto very simple ones. Urdhva Tiryagbhyam Sutra is a general multiplication formula applicable to all cases of multiplication. Because of parallelism in generation of partial products and their summation obtained, speed is improved. In this algorithm the small block can be wisely utilized for designing bigger NxN multiplier.

Vedic mathematics provides easiest way to perform multiplication. It reduces the typical calculation which is difficult to compute using conventional multiplier. Urdhava Tiryagbhyam is general multiplication formula applicable for all types of multiplication. The parallelism in generation of partial product improves the speed of multiplication. For computing big multiplication of N X N, the number is divided in to small blocks and utilize for design. For higher number of bit some modification is required. Divide the number in to two equal parts. Let's analyse 4x4 multiplication, Say X3X2X1X0 and Y3 Y2 Y1 Y0 . The result of multiplication of these two numbers is given by M7 M6 M5 M4 M3 M2 M1 M0. Let'sdivide the X and Y in to two parts say X3X2and X1X0for X and Y3Y2and Y1Y0for Y. using the Vedic multiplication method consider 2 bit at a time and perform the multiplication on using 2 bit multiplier. The following structure shows the multiplication of 4 x 4 numbers using Vedic multiplier.

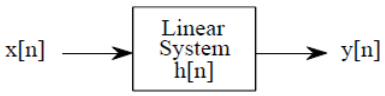
3.2 Convolution using proposed system

Convolution is a mathematical way of combining two signals to form a third signal. It is the single most important technique in Digital Signal Processing. Using the strategy of impulse

decomposition, systems are described by a signal called the impulse response . Convolution is important because it relates the three signals of interest: the input signal, the output signal, and the impulse response. This chapter presents convolution from two different viewpoints, called the input side algorithm and the output side algorithm. Convolution provides the mathematical framework for DSP.

Convolution is a formal mathematical operation, just as multiplication, addition, and integration. Addition takes two numbers and produces a third number , while convolution takes two signals and produces a third signal. Convolution is used in the mathematics of many fields, such as probability and statistics. In linear systems, convolution is used to describe the relationship between three signals of interest: the input signal, the impulse response, and the output signal.

The notation when convolution is used with linear systems. An input signal, x[n] , enters a linear system with an impulse response, h[n], resulting in an output signal, y[n] . In equation form: x[n]*h[n]=y[n] Expressed in words, the input signal convolved with the impulse response is equal to the output signal. Just as addition is represented by the plus, +, and multiplication by the cross, ×, convolution is represented by the star, *. It is unfortunate that most programming languages also use the star to indicate multiplication. A star in a computer program means multiplication, while a star in an equation means convolution.



$$x[n] * h[n] = y[n]$$

Convolution is considered to be heart of the digital signal processing. It is the mathematical way of combining two signals to obtain a third signal. Convolution helps to estimate the output of a system with arbitrary input, with knowledge of impulse response of the system. Linear systems characteristics are completely specified by the systems impulse response, as governed by the mathematics of convolution. Convolution is an operation which takes two functions as input, and produces a single function output (much like addition or multiplication of functions).Consider two finite length sequences f(n) and h(n) on which the convolution operation is to be performed with lengths l and m respectively. The output of convolution operation y(n) contains l+m-1 number of samples.

The linear convolution of f(n) and h(n) is given by :

$$y(n) = x(n) * h(n)$$

$$y[n] = \sum_{k=-\infty}^{\infty} x(k)h(n-k)$$

Convolution Using VEDIC Mathematics:

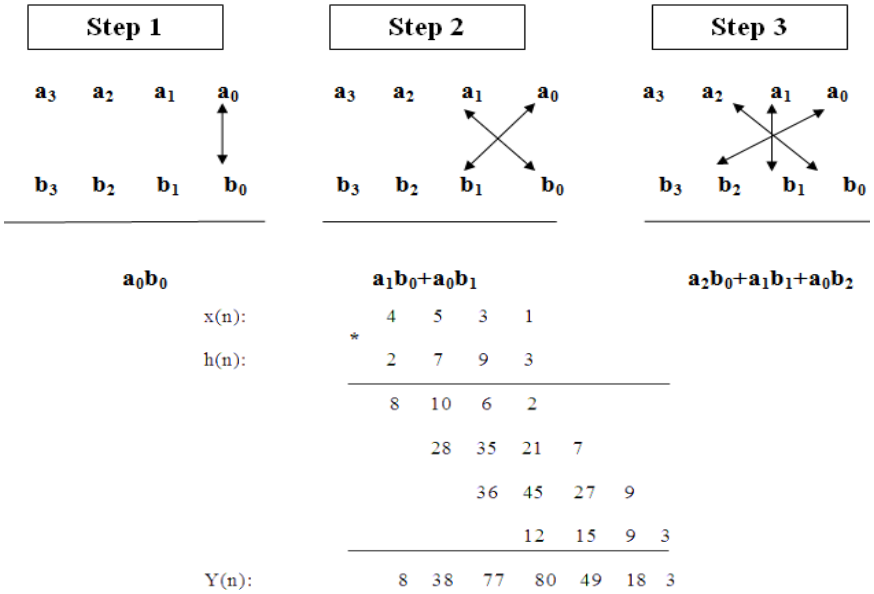


Fig 3.3: Example of Convolution using Proposed Method

IV. DECONVOLUTION

Deconvolution is an operation which takes two functions one input is convolved sequence y(n) where as other input is h(n) , and produces a single function output x(n).For Deconvolution a direct method is presented for performing Deconvolution of two finite length sequences.. The basic recursive Deconvoltion method is used for finding Deconvoltion of finite length sequences. The recursion method works similar to performing long division [10]. To illustrate the method further Consider the example 2, let Y(n) be the convolved sequence equal to (8,38,77,80,49,18,3) and h(n) be the finite length sequence equal to (2,7,9,3). Performing Deconvolution resulting x(n)= (4,5,3,1)

The Deconvolution of finite length sequences Y(n) and h(n) using recursion method as shown below

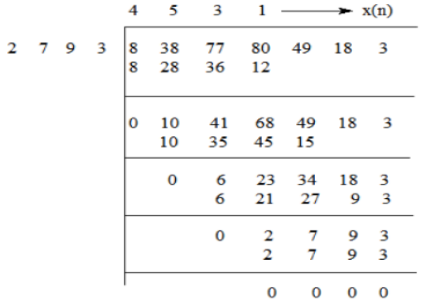


Fig 4.1: Deconvolution using proposed method

By observing figure one can easily predict, for implementing speedy deconvolution by above method, divisor , multiplier and adder(to achieve subtraction inform of addition) used in design must be speedy. High speed division can be carried out by selecting proper division algorithm. Vedic multiplier is used to get speedy multiplication.

Software Required:

The proposed paper requires Xilinx ISE 14.3 and Verilog source code for design implementation.

XILINX design flow

The first step involved in implementation of a design on FPGA involves System Specifications. Specifications refer to kind of inputs and kind of outputs and the range of values that the kit can take in based on these Specifications. After the first step system specifications the next step is the Architecture. Architecture describes the interconnections between all the blocks involved in our design. Each and every block in the Architecture along with their interconnections is modeled in either VHDL or Verilog depending on the ease. All these blocks are then simulated and the outputs are verified for correct functioning.

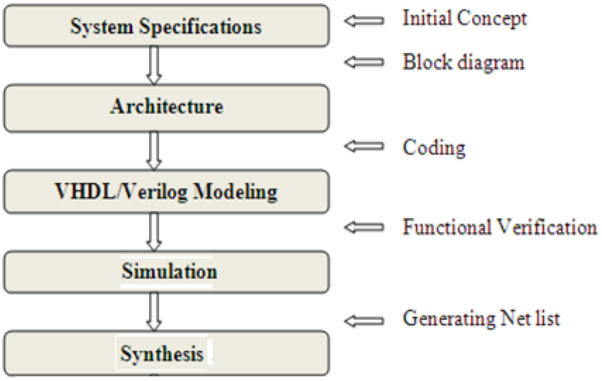


Fig 4.2: Xilinx Implementation Design Flow-Chart

V. EXPERIMENTAL RESULTS

Simulation Results:

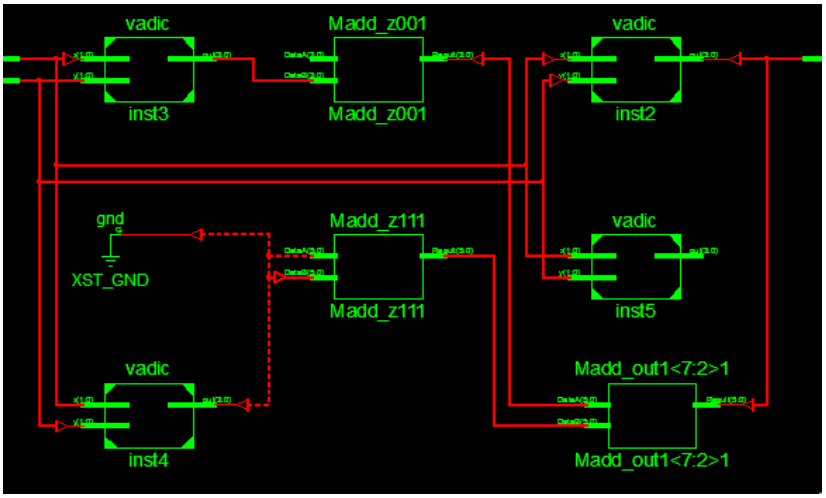


Fig5.1: Internal Schematic of 4 bit Vedic Multiplier

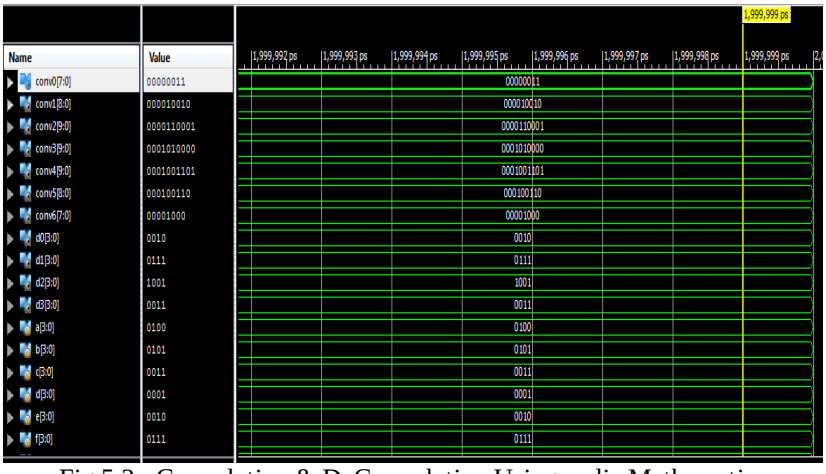


Fig 5.2: Convolution & DeConvolution Using vedic Mathematics

The Convolution module is simulated on Xilinx ISE simulator. . Simulation is the process of forcing the inputs to verify the functionality of the design.

The figure 5.2 shows the simulation waveforms of convolution and deconvolution using vadic mathematics with inputs are a,b,c,d,e,f,g,h the outputs of convolution are conv0,conv1,conv2,conv3,conv4,conv5,conv,conv7 the outputs of deconvolution are d0,d1,d2,d3

Synthesis Results:

The following table shows the difference of synthesis report between the existing and proposed 4x4 multiplier. In this design summary shows the how many slices, used and how many 4 input LUTs are used and also it is show the power consumption and delay of 4 bit array multiplier and 4 bit vedic multiplier.

Table 1: Synthesis report comparison between 4 bit array and Vedic Multiplier

Parameter	4 bit array Multiplier	4 bit Vedic Multiplier
Number of slices	16	14
Number of 4 input LUT's	30	27
Delay	15.554ns	14.675 ns
Power Consumption	0.158	0.158

VI. CONCLUSION

In this paper, a method for calculating the linear convolution, and deconvolution with the help of Vedic mathematics that are easy to learn and perform is introduced. The execution time and area of the proposed Vedic multiplier is compared with array multiplier and we can observe that the vadic multiplier consumes very less area and having very high speed compared with array multiplier. This Project can further be extended to implement circular convolution and deconvolution.

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