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Dual-Band High Efficiency Class-E Power Amplifier

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Abstract— The evolution of new mobile communication standards demand highly efficient multi-band power amplifiers (PAs) both in mobile equipment's and base stations. The design of CMOS power amplifiers (PAs) is still a challenging task. In this paper, a dual-band amplifier for wireless applications in a 0.18 µm CMOS process is presented. The PA uses class-E topology to exploit its soft-switching property for high efficiency. The proposed PA is simulated by Advanced Design System (ADS) in TSMC 0.18 µm CMOS process and simulation results show that the designed PA can deliver 21.407/21.523 dBm output power to 50 Ω standard load at 2.4/5.15 GHz with 55.1/51.07% Power-Added-Efficiency (PAE) and drain efficiency (DE) 55.5/51.4 % from 1.8 V supply voltage.

Keywords—CMOS, Class-E, Power Amplifier, Driver Circuit Dual-Band, Power Added Efficiency (PAE)

I. INTRODUCTION

The implementation of multi-band systems is a very important issue for the next generation wireless communication. While base-band and analog circuits can be integrated within a single chip for multi-band polar transmitters without significant problems [1], [2], the integration of RF circuits, especially power amplifier (PA), needs serious circuit research because of the difficulties in the optimum power matching and harmonic elimination for each band. Wireless connectivity in portable applications demands high-efficiency RF transmitters to save battery life, desirably integrated into the same chip with standard CMOS logic to reduce costs. The Power Amplifier (PA) is a key component of the RF transmitter, consuming the largest portion of DC power, and generating spurious and thermal interference. The design of efficient and reliable CMOS PAs constitutes a topic of intense research [3], [4]. Among all classes of nonlinear power amplifiers, the c1ass-E power amplifier is better choice in terms of circuit simplicity and high efficiency and this class has good performance at higher frequency [5], [6]. This paper is focused on the design of reliable, high efficiency CMOS PAs for high power transmitter applications. A cascode switched mode Class-E topology, very promising for integrated solutions, is investigated to maximize PA efficiency without compromising device reliability. The rest of the study is organized as follows. The rest of this paper is organized as follows. In section II, the basic operation of c1ass-E P A will be described. In section III, a dual-band class-E PA is proposed and some related concepts will be elaborated. A final simulation result is shown in section IV. Finally, the conclusion is provided in section V.

II. BASIC OPERATION OF CLASS-E POWER AMPLIFIER

It is a switched amplifier and the active device works as a switch. It was invented in 1975s by Nathan and Alan Sokal [7]. A typical configuration of class-E PA with its waveforms is shown in Fig. 1. The inductance L can be a RF choke or a finite DC-feed inductance. However, by carefully choosing the value of L to be a finite value, the efficiency of c1ass-E amplifier can be increased. The shunt capacitor is shown by C_p in Fig. 1 which contains the internal capacitance of the transistor and the external capacitor. In the OFF state of the transistor, current flows through the shunt capacitor and in the ON duration current flows through the transistor; where the transistor is in saturation mode. As usual in the class-E analysis, we will assume that the loaded Q-factor of the series L_f-C_f resonator is very high, so that only a sinusoidal current at the carrier frequency is allowed to flow through the load resistance R_{opt}. The S block is a switching transistor that is turned ON and OFF at the carrier frequency. Under soft-switching conditions were introduced by Sokal, the transistor would dissipate zero power because the voltage and current waveforms would never overlap, and thus no power would be dissipated. In this way, ideally the c1ass-E amplifier has an efficiency of 100%. However the finite on-resistance of the switch and the non-ideal ON-OFF transition times decrease the overall efficiency.

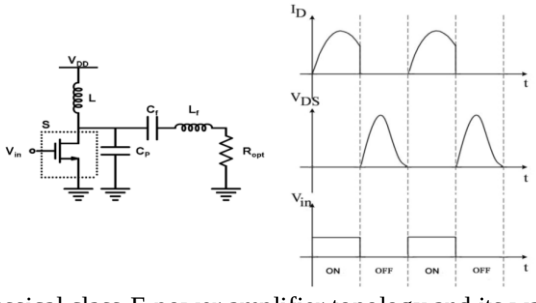

Fig. 1 Classical class-E power amplifier topology and its waveforms

L acts either a RF chock (RFC) or a finite DC-feed inductance. C_P and are design to be a series LC resonator as a band-pass filter. These elements are designed so that the conditions for a class-E power amplifier operation are met.

These conditions are as follows:

i. Voltage across the switch keeps low when the switch turns off.
ii. Voltage across the switch is zero when the switch turns on.
iii. The first derivation of the voltage is zero when the switch turns on.

These conditions ensure no overlapping between the current and voltage wave form over the whole period of time. Those components value can be calculated using the following equations [8], [9].

$$C_f = \frac{P_{OUT}(\pi^2+4)}{8\omega {V_{DD}}^2 Q_L} \quad (1)$$

$$R_{opt} = \frac{8V_{DD}^2}{P_{OUT}(\pi^2+4)} \quad (2)$$

$$L_f = \frac{8{V_{DD}}^2 Q_L}{\omega P_{OUT}(\pi^2+4)} \quad (3)$$

$$C_P = \frac{P_{OUT}}{\pi\omega^2 {V_{DD}}^2} \quad (4)$$

III. CIRCUIT DESIGN

The full schematic of the two-staged Class-E power amplifier is given in Fig. 2. Input and output matching networks are developed for 2.4 and 5.15 GHz fixed carrier frequency. The input power is set to the typical value, 0dBm. As the highest drain voltage of the c1ass-E output stage can be over 3 times of the supply voltage and the CMOS transistors have low breakdown voltage, switch configuration is implemented by NMOS cascode transistors in order to protect the switching transistors. In this case, the device stress is posed on the common gate transistor, which is illustrated in Fig. 3. Furthermore, cascode structure provides high isolation from the input to the output, thus helps to eliminate dependence of input and output matching on one another in single common source transistor. For calculating the transistors sizes, the gate length is in most cases made equal to the minimal gate length of the technology and so the transistors width is the only remaining parameter that needs to be carefully selected. The size of the transistors can only be estimated by their maximum allowable current flow and they have to be traded off to have both a small on-resistance and a small parasitic capacitance; because the on-resistance is reversely proportional to the transistor width and limits the maximum efficiency, and the parasitic capacitance is directly proportional to the width of transistor and limits the maximum operating frequency of the class-E PA [10].

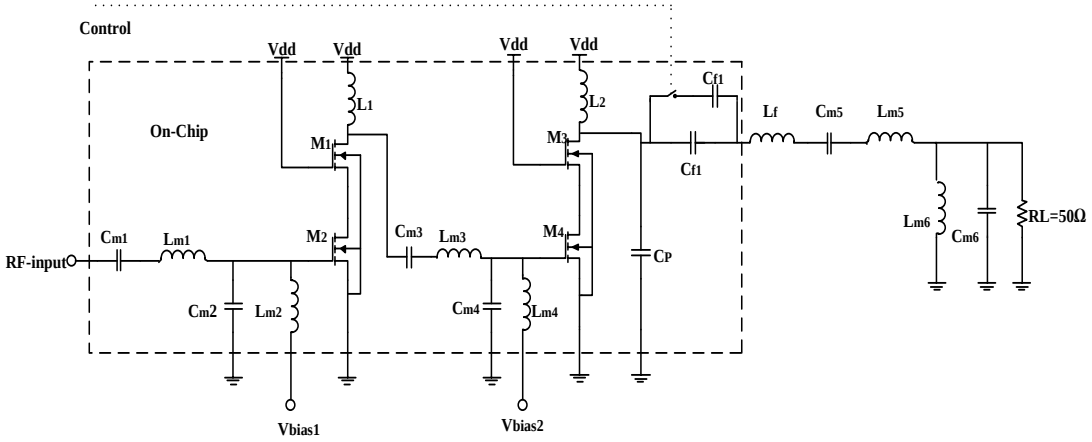

Fig. 2 The proposed class-E power amplifier

Table I. Simulated Performance Values

Control	Frequency	Output Power	DE	PAE
0	5.15 GHz	21.523 dBm	55.4 %	51.07 %
1	2.4 GHz	21.407 dBm	55.5 %	55.1 %

IV. SIMULSTION RESULTS

The proposed power amplifier in Fig. 2 was optimized and simulated by using Advanced Design System (ADS) in TSMC 0.18 µm CMOS technology for 2.4/5.15 GHz and considering output off-chip matching network are replaced by physical lumped element models. Fig. 3 shows the drain voltage and current waveforms at the drain of M3, demonstrating the high current waveform mainly overlaps with the approximately zero voltage waveform and vice versa in the same period. Fig. 4 shows a plot of output power and PAE versus supply voltage. The output power and PAE are 21.407/21.523 dBm and 55.1/51.07 % in 1.8V supply voltage respectively. Fig. 5 shows the simulated drain efficiency (DE) for each band. The drain efficiency is 55.5/51.4 % for the 2.4/5.15 GHz, respectively.

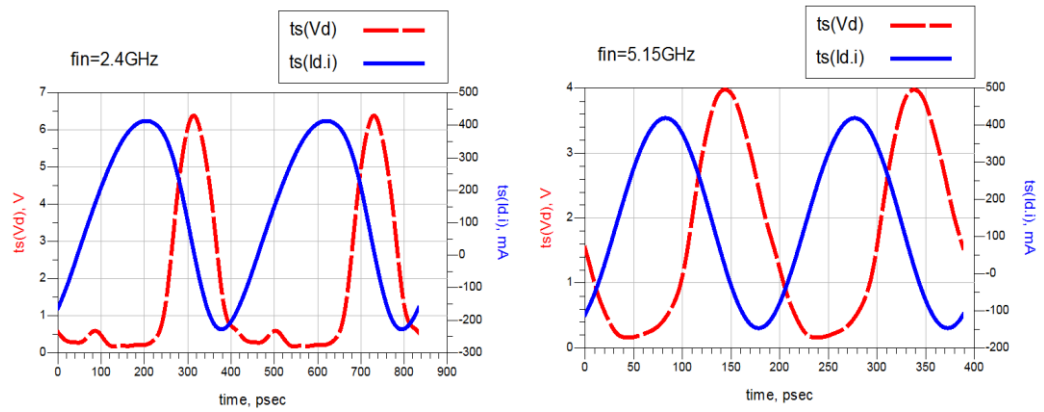

Fig. 3 Drain current and voltage waveforms of M3

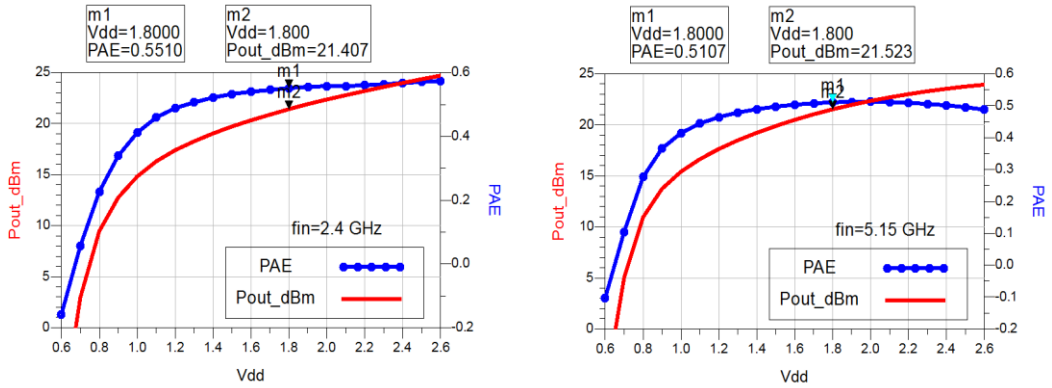

Fig. 4 Output power and PAE versus supply voltage

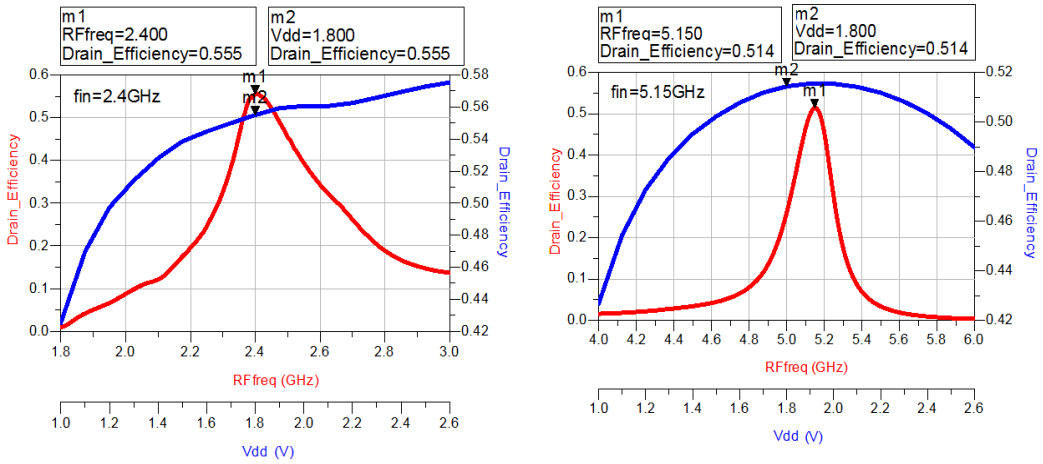

Fig. 5 Simulated drain efficiency

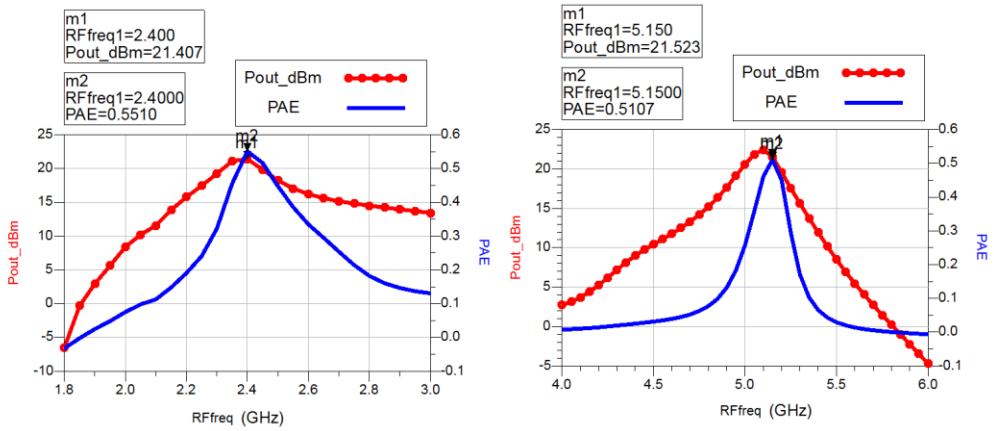

Fig. 6 Output power and PAE as a function of frequency

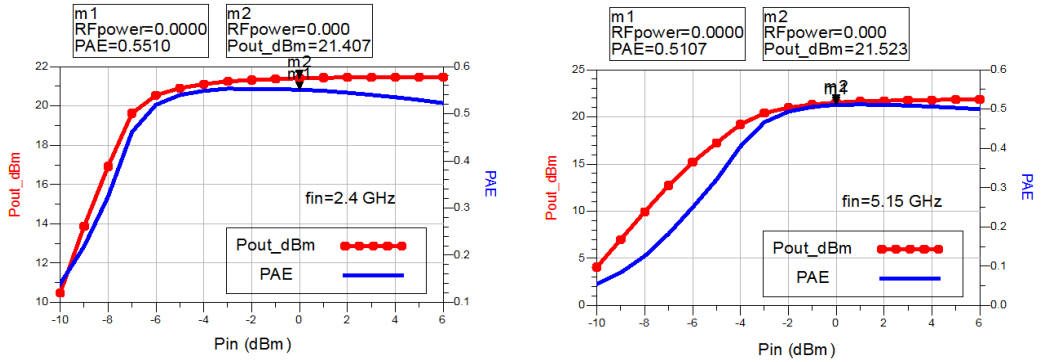

Fig. 7 Pout, PAE and power gain vs. input power

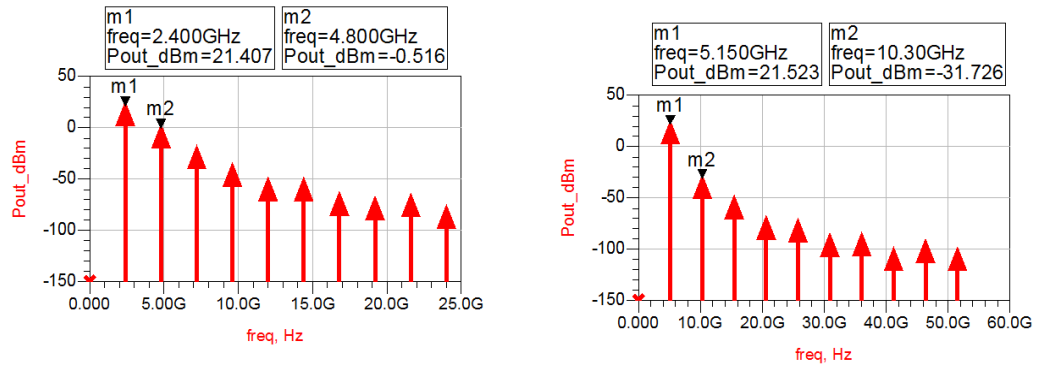

Fig. 8 Output spectrum

Table II. This Work Performances Comparison with Previous Works

References	Technology	Frequency (GHz)	Supply voltage (V)	Output Power (dBm)	DE (%)	PAE (%)
[11]	0.13µm CMOS	2.4/3.5	1.5	18.3/19.0	--	43/43
[12]	0.13µm CMOS	1.7/2.5	3.3	28.0/27.0	63.3/70.3	57.0/61.5
[13]	0.18µm CMOS	1.9/2.3/2.6/ 3.5	1.8	24.2/23.8/23.4/ 20.5	48.2/44.3/ 40.9/35.6	44.5/40.6/3 7.1/32.4
[14]	0.18µm CMOS	2.4	3.3	21.3	55	40
[15]	0.13µm CMOS	1.7	2.5	31	67	58
[16]	0.18µm CMOS	5.7	1.8	25	--	42.6
This Work	0.18µm CMOS	2.4/5.15	1.8	21.407/21.523	55.5/51.4	55.1/51.07

V. CONCLUSIONS

In this paper, the implementation of a dual-band class-E PA in a 0.18 µm CMOS process is presented. The proposed architecture used cascode structure to overcome the low breakdown voltage problem of submicron CMOS transistors and therefore moderate power losses. All circuit components, except the output matching network have been designed on-chip. The designed circuit can satisfy the high-efficiency requirements of modern digital wireless communications.

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