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Design of CMOS Divide by-four Frequency Divider for Wireless Communication Application

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Abstract— In this paper, a circuit topology of a CMOS divide-by-4 injection-locked frequency divider is presented for wireless communication applications. Operated at a supply voltage of 1.4 V the divider core consumes a dc power of 1.4 mW. At an incident power of 0 dBm, the simulated circuit exhibits an input locking range of 0.8 GHz in the vicinity of 10 GHz. The measured output locked phase noise at 1-MHz offset is -153.458 dBc/Hz.

Keywords— Divide by-4, Direct injection, Injection locked frequency divider (ILFD), Low voltage, Locking range.

I. INTRODUCTION

Being a crucial building block in wireless and wireline communication systems, the frequency divider is typically employed to provide a low-frequency replica of the input signal, facilitating the required phase locking in a phase-locked loop (PLL). Recently, with the emerging applications such as wireless personal area network (WPAN), automobile radars, and image sensing, the development of CMOS frequency dividers operating at millimetre-wave frequencies has attracted great attention. Among the existing circuit topologies, dividers based on current-mode logic (CML) flip-flops [1], [2] are widely utilized in conventional circuit designs due to its simplicity and wideband characteristics. The use of digital frequency dividers is constrained at high frequencies by their high power consumption which increases rapidly with frequency [3]. Unfortunately, the maximum operating frequency of such circuits is severely restricted by the cut-off frequency (f_T) of the MOS devices. In order to alleviate the limitation imposed by f_T, the injection-locked frequency dividers (ILFDs) [4], [6] have been proposed. Compared to CML and Miller dividers, the power consumption of an ILFD does not increase significantly with frequency. The advantage of the ILFD is that it has the potential for low power operation because the relatively small perturbation by the input signal does not significantly affect the power consumption of the underlying oscillator [7]. However, the injection-locked dividers inherently suffer from an insufficient locking range, which has become a major concern in practical circuit implementations. In most PLL designs, a high division ratio is typically required for low-frequency input references. Considering the overall power consumption and chip area, it is advantageous to use a divide by-4 ILFD instead of cascading two divide-by-2 stages. In this paper, the ILFD circuit that offers low power consumption for operations at a division ratio of 4 is presented.

II. CIRCUIT DESIGN

An ILFD is an electronic oscillator which produces an output signal whose period (equivalently, zero-crossing rate) is rationally related to that of the input signal [8]. When there is no injected input signal, the oscillator oscillates with a free running frequency f_0. When an injection signal V_i with a frequency f_s, then the output signal V_o oscillates with a frequency f_d . The ratio of f_s/f_d is called the rotation number, denoted by ρ [9]. This locking behaviour is due to the nonlinear phenomenon of synchronization, also known as entrainment or 1 : *m* order injection locking [10], [12]. Analog frequency divider is basically a super-harmonic injection-locked oscillator [4] in which the input signal frequency is approximately equal to an integer multiple (usually less than 10) of its self-oscillating frequency. With a large division ratio, the operating frequency of the ILFD can be increased drastically.

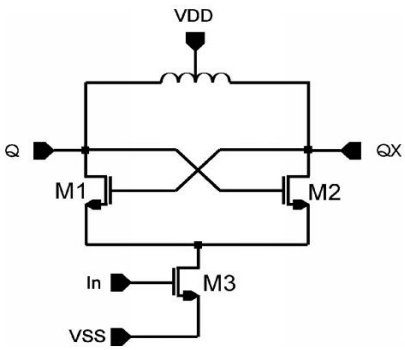

Figure 1: Classical injection-locked oscillator topology

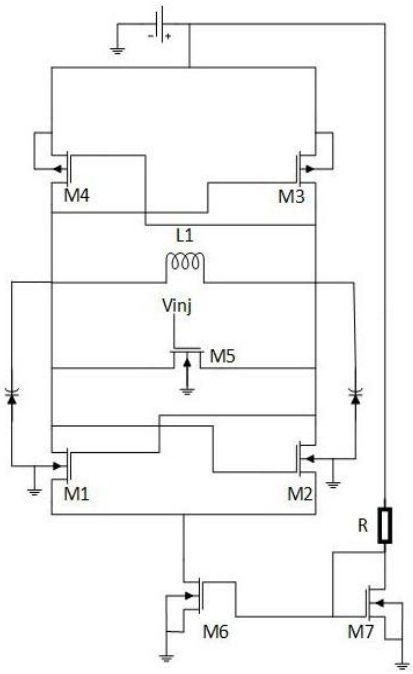

Figure 2: Proposed injection-locked frequency divider

To achieve improved phase-noise performance, a proposed CMOS ILFD design is shown in Fig. 2. It was designed without the top current source, and can achieve low phase noise while also maintaining low power consumption. The cross-coupled NMOS (M_3, M_4) and PMOS (M_1, M_1) transistor pairs generate negative impedance to compensate for the loss of the LC tank, as described in Eq. 1:

$$Z_{in} = \frac{-2}{g_{mn} + g_{mp}} \quad (1)$$

Where:

Z_{in} is the input impedance, g_{mn} is the transconductance of the NMOS device, and g_{mp} is the transconductance of the PMOS device. PMOS technology offers the means of suppressing flicker noise and controlling current consumption.

$$\omega_0{}^2 \approx \frac{1}{L.(C_p + C_{var})} \quad (2)$$

Where:

L = the VCO inductor; C_p = the parasitic capacitance; Cvar = the varactor capacitance

Part of the design challenge is to establish the required g_m values for the NMOS and PMOS devices by appropriate adjustment of the device weight-to-length (W/L) ratios. Oscillator phase noise depends a great deal on the Q of the tank circuit used for a particular oscillator. As a result, improved phase noise requires careful attention to the tank circuit.

The locking range of an ILFD is defined as the input frequency range in which the ILFD is able to divide properly the frequency of the incoming signal by the desired ratio. The locking range of an ILFD is defined as the input frequency range in which the ILFD is able to divide properly the frequency of the incoming signal by the desired ratio. according to [5], the relationship between the locking range ($\Delta\omega$) and quality factor (Q) of the resonant tank is mainly governed by the following expression:

$$\left|\frac{\Delta\omega}{\omega_0}\right| < \left|\frac{H_0 a_2 V_{in}}{2Q}\right| \quad (3)$$

The above equation indicates that the locking range may be improved by using a tank circuit of low Q-factor. However, a small Q value will lead to poor phase-noise performance of the divider circuit. And for oscillation to occur, the cross-coupled pair must be able to provide sufficient gain to compensate for the loss (resistance), thus a higher current consumption may be required. Hence, there is a trade-off between locking range, power consumption and output noise level.

III. SIMULSTION RESULTS

The demonstrated ILFD in Fig.1 was designed using the TSMC 0.18µm technology and simulated by Advance Design System (ADS). The power consumption of the ILFD core is 1.4 mW for a 1.4V supply voltage. Fig 6 depicts the simulation result for phase noise for the proposed ILFD, which is about –149.285 to -153.458 dBc/Hz at 100KHz to 1MHz offset frequency. The measure used for comparing different ILFDs is figure of merit that is defined by [5], [6]:

$$\boldsymbol{FOM = L\{\Delta f\} - 20log\left(\frac{f_0}{\Delta f}\right) + 10log\left(\frac{P_{DC}}{1\ mW}\right)} \quad (4)$$

Where:

L(Δf) = the locked phase noise; Δf = the offset frequency; f_0 = the carrier frequency; and P_{DC} = the DC power consumption of the ILFD.

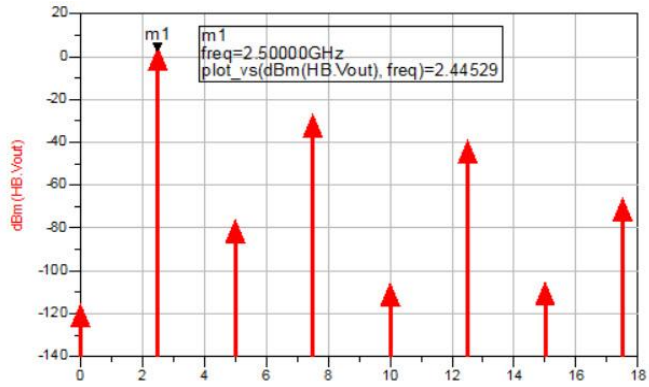

Figure 3: Harmonic balance output spectrum

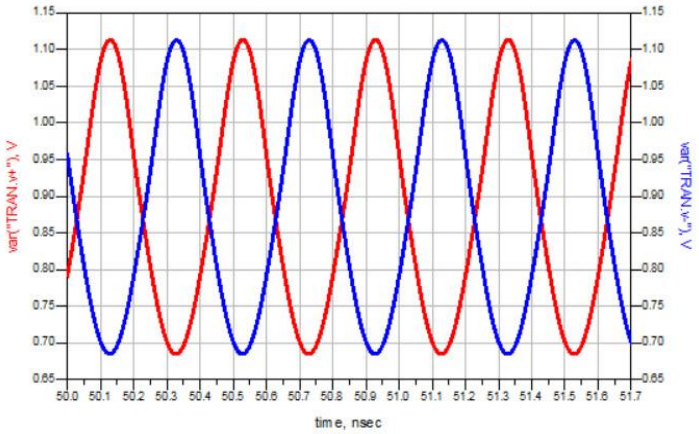

Figure 4: Output waveform V_{out}^{+} and V_{out}^{-}

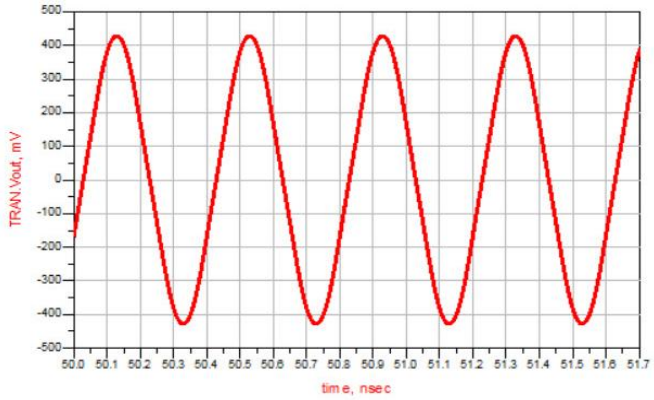

Figure 5: Differential output waveform

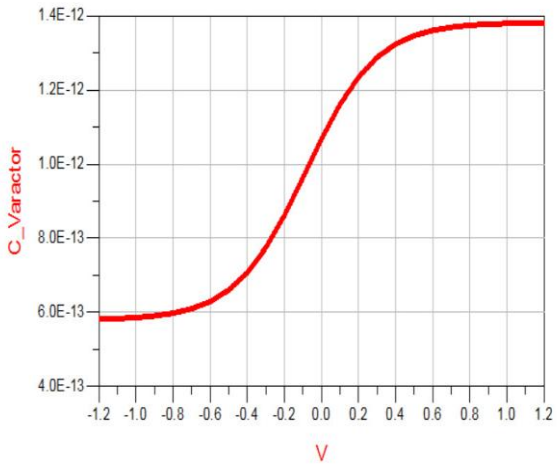

Figure 6: Capacitance variation versus tuning voltage

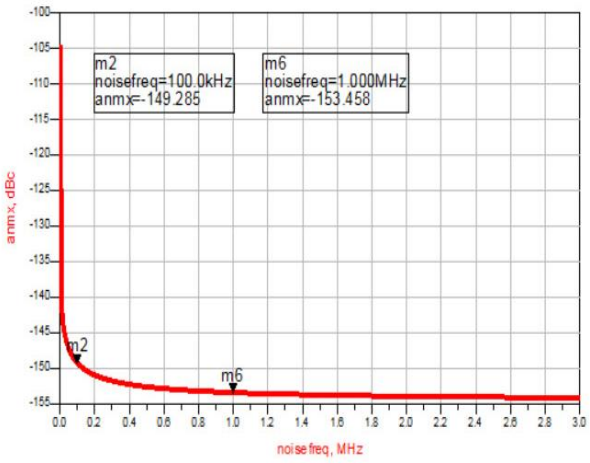

Figure 7: Simulation result for phase noise

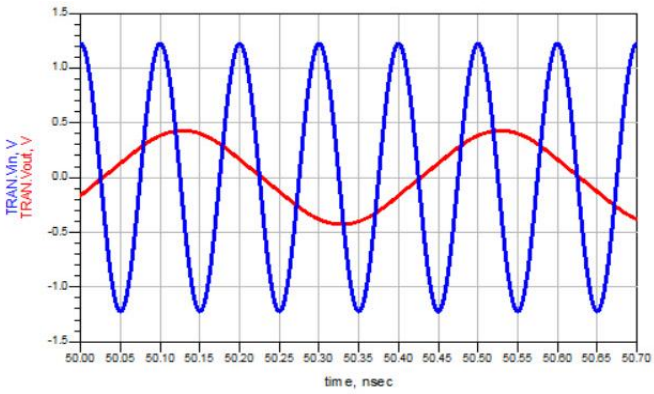

Figure 8: Injection voltage and output waveforms of the ILFD-by-4 with 10 GHz input frequency

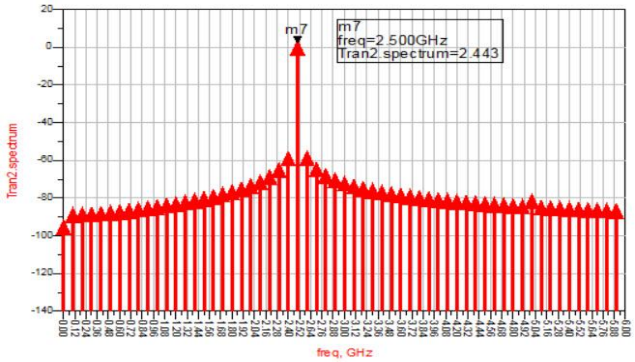

Figure 9: Simulated locked spectrum at 10 GHz injected frequency

IV. CONCLUSIONS

The proposed ILFD is designed in TSMC 0.18 µm CMOS technology. The measured phase noise at 1 MHz offset from the center frequency of 2.5 GHz is -153.458 dBc/Hz The power consumption of the ILFD for a 1.4V supply is 2.8mW. The input frequency input locking range of 0.8 GHz approximately 10 GHz. The studied model's figure of merit is about -172.8 dBc/Hz.

Table I. This Work Performances Comparison With Previous Works

References	Technology	Input Power (dBm)	Supply voltage (V)	Locking Range (GHz)	Power (mW)	Phase Noise@1MHz (dBc/Hz)	FOM@1MHz (dBc/Hz)
[16]	0.18µm CMOS	8	1.8	6.5-11.08	6.6	-137.9	-168.28
[17]	0.18µm CMOS	0	1.8	1.2-7.4	13.8	-130	-138.51
[18]	90nm CMOS	5	1.2	19.5-22	6.4	-126.6	-178.89
[19]	0.18µm CMOS	0	1.8	18.8-23.2	38	-134.8	-180.2
This Work	0.18µm CMOS	0	1.4	9.6-10.4	2.8	-153.458	-172.8

REFERENCES

[1] H. Wang, "A 1.8 V 3 mW 16.8 GHz frequency divider in 0.25 um CMOS," in IEEE Int. Solid-State Circuits Conf. Tech. Dig., pp. 196–197, Feb. 2000.

[2] B. Razavi, "Challenges in portable RF transceiver design" IEEE Circuits Devices Mag., vol. 12, no. 9, pp. 12–25, Sep. 1996.

[3] B. Razavi, K. F. Lee, and R.-H. Yan, "A 13.4-GHz CMOS frequency divider," in IEEE Int. Solid-State Circuits Conf. Tech. Dig., pp. 176–177, Feb. 1994.

[4] H. R. Rategh and T. H. Lee, "Superharmonic injection-locked frequency dividers," IEEE J. Solid-State Circuits, vol. 34, no. 6, pp. 813–821, Jun. 1999.

[5] R. J. Betancourt-Zamora, S. Verma, and T. H. Lee, "1-GHz and 2.8-GHz CMOS injection-locked ring oscillator prescalers," in IEEE VLSI Circuits Symp. Tech. Dig., pp. 47–50, Jun. 2001.

[6] S. Verma, H. R. Rategh, and T. H. Lee, "A unified model for injection locked frequency dividers," IEEE J. Solid-State Circuits, vol. 38, no. 6, pp. 1015–1027, Jun. 2003.

[7] L.-H. Lu and J.-C. Chien, "A wideband CMOS injection-locked ring oscillator," IEEE Microw. Wireless Compon. Lett., vol. 15, no. 10, pp. 676–678, Oct. 2005.

[8] B. Razavi, "A study of injection locking and pulling in oscillators," IEEE J. Solid-State Circuits, vol. 39, no. 9, pp. 1415–1424, Sep. 2004.

[9] M.P. Kennedy, K.R. Krieg, and L.O. Chua. "The devils staircase: the electrical engineers fractal." IEEE Trans. Circuits and Systems, vol. 36, no. 8, pp. 1133–1139, Aug. 1989.

[10] R. Adler, " A study of locking phenomena in oscillators," Proc. IRE Waves Electrons, vol. 34, no. 6, pp. 351–357, Jun. 1946.

[11] A. Pikovsky, " Rosenblum, and J. Kurths, Synchronization. Cambridge," U.K.: Cambridge Univ. Press, 2001.

[12] M. V. Bartuccelli, J. H. B. Deane, and G. Gentile, "Frequency locking in an injection-locked frequency equation," Proc. R. Soc. London A, Math. Phys. Eng Sci., vol. 465, no. 2101, pp. 283–306, Jan. 2009.

[13] M. Tiebout, "A CMOS Direct Injection-Locked Oscillator Topology as High-Frequency Low-Power Frequency Divider,"IEEE. Journal of Solid-State Circuits., vol. 39 No.7, pp. 1170-1174, July 2004.

[14] I-ShingShen, Han-TzungKe, and Christina F. Jou, "A Ultra Low Power 5.4-GHz Current-Reused VCO with Internal LC," Proceedings of Asia-Pacific Microwave Conference, pp.457-459, 2010.

[15] D. Ham, A. Hajimiri, "Concepts and methods in optimization of integrated LC VCOs," IEEE J Solid-State Circuits 36,pp.896–909, June 2001.

[16] J. Yin, N. Li, R. Zheng, W. Li, and G, Ren, "Low-Power wide-locking-range injection locked frequency divider for OFDM UWB systems," journal of Semiconductor, vol. 30, no. 5, pp. 055003-1-5, 2009.

[17] Chuang Y H, Jang S L, Lee S H. A wide band injection locked frequency divider with variable inductor load," IEEE Microw Wireless Components Lett, 17(6): 460, 2007.

[18] Shibasaki T, Tamura H, Kanda K, et al. "20-GHz quadrature injection-locked LC dividers with enhanced locking range," IEEE J Solid-State Circuits, 3(43): 610, 2008.

[19] Lin H Y, Hsu S H, Chan C Y, et al. "A wide locking-range frequency divider for LMDS applications," IEEE Trans Circuits Syst, 9 (54): 750, 2007.

