Volume 6, Issue 3, March 2016 ISSN: 2277 128X
International Journal of Advanced Research in Computer Science and Software Engineering
Research Paper
Available online at: www.ijarcsse.com

Design of Ultra Low Power 1 Bit Full Adder Cell Using Advance GDI 6T Logic Style

Ruchi Gupta*, Atul Kumar Pathak, Gunakesh Sharma
ECE Department & RGPV University,
M.P., India

Abstract— in this paper, we introduce a simple analytical model of full adder logic cell for estimating speed, area and switching power dissipation in deep sub micron CMOS digital circuit. The main design objectives for these Advance 6T Full adder cell modules over the basic GDI full adder cell with 12 transistors are providing Low-Power dissipation, high speed, less area with full-voltage swing without using extra elementary growth on design. In this design, we employed with 6 transistors. The utilizes dynamic change in the width Length ratio with in order to get specified results with process variation new 6T full adders with new methodology. This design is based on a different new approach which eliminate of the need of extra gates for designing full adder cell; it provides high speed and Ultra Low-Power, as well as a full voltage swing without any extra component required. Many of the previously reported adders in literature suffered from the problems of extra elements required to full-fill the circuit recruitment like voltage-swing and speed when operated at low supply voltages. This new designs successfully operate at ultra low voltages. The studied circuits are optimized at 45nm and 90 nm PTM (Tanner). The comparison between these two novel circuits in terms of Power, Delay

Keywords— Propagation delay, Power consumption, Power-Delay-Product, Advance 6T Full Adder design, GDI design style.

I. INTRODUCTION

The increasing demand for low power very large scale integration (VLSI) at different design level, such as architectural, circuit, layout and the process technology At the circuit design level, considerable potential for power saving by means of proper choice of a logic style for implementing digital circuit. Most of the operations based on addition. With these operations we need to minimize the power consumption and increasing speed of the system without further growth on the chip area, the low power requirement of VLSI system design have challenged the area of research towards technology, architectural design and methodology solution to allow reduce power dissipation on CMOS Circuits. Power dissipation influenced parameters are switching capacitance, transition activity and short circuit current in the chosen logic style. Since the full adder cell is performing regularity in the CMOS functional units, improving the performance of the 1-bit full adder is a major goal and has attracted much attention. A variety of full adders using different architectural designs and technologies have been reported in literature [1] and they commonly aim to tradeoff between power consumption and propagation delay. Adder performance affects the arithmetic system and functional units such as multiplier ALU etc. An optimized design is required to prevent any reduction in the output signal, consume less power, have less delay in critical path and be reliable even at low supply voltage as we scale towards nano-meter, layout regularity, and interconnect complexity are also primary concern. By scaling down the feature size of devices in nanometer, the supply voltage should be scaled down to avoid effects of hot carrier in CMOS circuitry. As a result, transistor size and static power playing main role in nano-scale circuits for efficient power control [2].

II. LITERATURE REVIEW

In this section we are using GDI-MUX approach with new methodology by eliminating the need of complex XOR-XNOR gates. Implementation of this Ultra Low- Power circuit using GDI technique [9] is discussed. The basic GDI cell is shown in Fig. 2 while the Truth-Table is shown in Table 1. The GDI cell contains three inputs: G (common gate input of NMOS and PMOS), P (input to the source/drain of PMOS) and N (input to the source/ drain of NMOS). Both NMOS and PMOS are linked to Nor P, so it can arbitrarily be biased at contrast to a CMOS inverter. These features give the GDI cell two extra input pins to use, which makes the GDI design more flexible than usual CMOS design. By considering the full adder's Truth-Table, it can be seen that Cout is equal to (A AND B) when Cin = '0', and Cout is equal to (A OR B) when Cin = '1'. Thus, a multiplexer can be used to obtain the Cout output. Following the same criteria, the SUM output is equal to (A OR B OR Cin) when Cout = '0', and SUM is (A AND B AND Cin) when Cout = '1'. Again, Cout can be used to select the respective value for the required condition, driving a multiplexer. Hence, an alternative logic scheme to design a full adder cell can be formed by AND, OR and MUX logic blocks In order to have an implementation of this alternative logic scheme used.

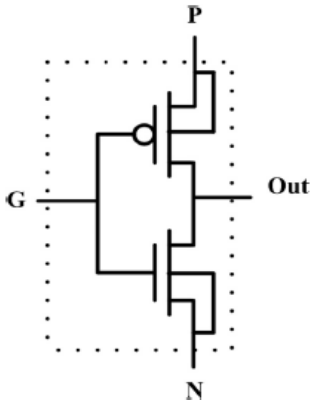

Fig. 1 Basic Gate-Diffusion Input (GDI) cell

GDI is suitable for designing fast, ultra Low-Power circuits, using less number of transistors while improving logic level swing and energy dissipation. By providing small cell library it's easy to improve W/L for transistor to transistor. The proposed GDI-MUX full adder is shown in Fig. 2. To implement (A OR B), N input is connected to V_{dd}, P is connected to B and G is connected to A, hence as shown in Fig. 4, Module.1is GDI implementation of (A OR B). In the next step (A AND B) is designed by connecting G, N and P to A, B and GND respectively. Module.2 in Fig. 2, illustrates the implementation of (A AND B). For producing C_{out}, C_{in} is connected to G input of GDI as enable and N is connected to (A OR B) and P is connected to (A AND B). Fig. 2 shows the implementation of multiplexer (module.3). Following the same criteria, (A OR B OR Cin) is implemented in Module. 4 by connecting G input to (A OR B), P to Cin and N to Vdd. Module.5 show (A AND B AND Cin) by connecting G input to (A AND B), P to GND and N to Cin. Finally in order to produce the SUM, GDI is used as a multiplexer with its G input connected to C_{out} and finally its P and N inputs are linked to (A OR B OR Cin) and (A AND B AND Cin) respectively.

This novel design takes advantage of using GDI technique which is proved [9] as one of the effective structures in designing Low-Power circuits. As stated in [9], this new approach minimizes both static and dynamic power consumption. This design eliminates the leakage current and also providing good driving capability which is necessary in a cascaded situation. This design also uses 12 transistors and has low dynamic power dissipation due to its low switching capacitance.

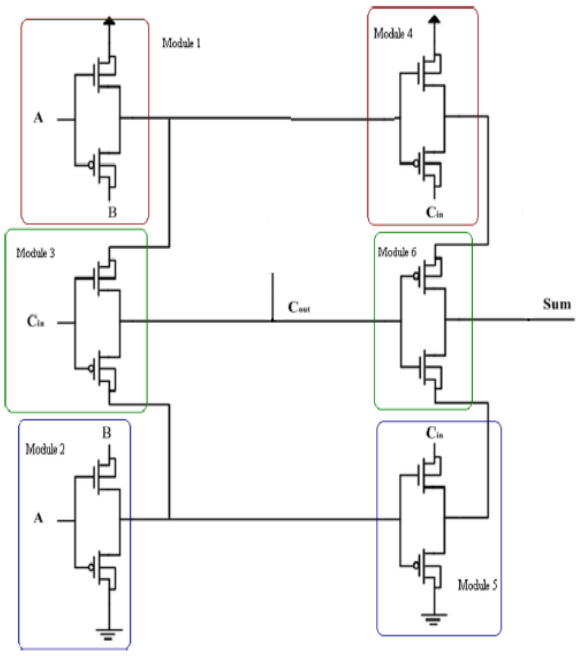

Fig. 2 GDI-MUX Full Adder

Table: 1 Truth Table of Basic GDI cell

N	P	G	OUT	FUNCTION
0	B	A	$\overline{A}B$	F1
B	1	A	$\overline{A+B}$	F2
1	B	A	A+B	OR
B	0	A	AB	AND
C	B	A	$\overline{A B + A C}$	MUX
0	1	A	$\overline{A}$	NOT

This design uses 12 transistors with dynamic W/L of transistor. We are eliminating UPLD circuit from the design and utilize the basic property of the CMOS transistor in this proposed methodology has low energy dissipation and speed without extra circuitry use.

III. PROPOSED DESIGN

In this work, advance 6T full adder is modified to absolute the extra circuit from previous GDI design. Here we use advance GDI cell without using multiplexer circuitry. We derive this design using three GDI basic cells with required

modification. The whole design depicted in fig. 3 in this figure we mansion three different cells that called modules. First module give us the XOR function between A and input B as per normal GDI cell both P and N inputs are different but we use same input with compliment of first input so that when ever input goes to '0' the output of cell goes to A and when input B goes to '1' than our output goes to compliment of A that all input output condition give the output same as output of XOR digital gate.

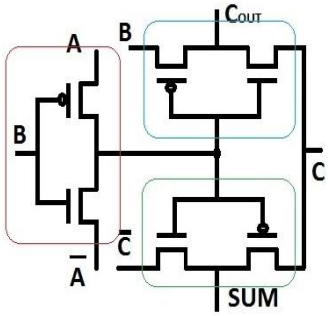

Fig. 3 PROSOSE-6T Full Adder

Table: 2 Truth Table of Advance GDI cell

N	P	G	OUT	FUNCTION
$\overline{A}$	A	B	$A \setminus B$	XOR
C	B	$A \oplus B$	$\overline{(A \setminus B)}B+(A \oplus B)C$	MUX

Now we are able to see in table 2 who show the Advance GDI implementation in this implementation we design the XOR digital output through basic GDI cell in second module we generate another XOR implementation with third input C when output of first module goes to '0' than output of module two goes to C and when output of module 1 goes to '1' it is the input of module 2 than output of module 2 goes to complement of C the total output of module 2 are replicate the SUM output of full adder cell that are the XOR of all three inputs (A XOR B XOR C).

The third module give the result of carry out of the full adder cell by using MUX function of GDI cell here our gate input are XOR of A and B when ever this input goes to '0' the output f the module goes to B and when the input of this GDI cell goes to '1' than output of the cell goes to C. the Boolean equation f the output of carry are

$$Cout = \overline{(A \oplus B)}\ B + (A \oplus B)\ C$$

That is exactly equal to the conventional carry output of full adder cell. After this Advance GDI 6T Full Adder design we are immerge the methodology of process variation with dynamic width length ration to improve the proper charging and discharging of drain current, as we same maintains the threshold voltage to get appropriate result with full voltage swing and minimum power dissipation with maximum speed of signal. Here we mainly improve the silica area of design approximately 50% that is biggest achievement of any design.

IV. SIMULATION RESULTS AND ANALYSIS

In this section, the proposed 6T full adder cells shown in Fig. 3 is evaluated and compared to the ones chosen from the literature is shown in fig. 2 both the circuits are implemented using Tanner EDA and extracted using 90nm and 45 nm PTM CMOS technology. Here we compare the results of both structural design methodologies with different parameters like area, power and speed.

According to Simulation results we are able to measure power delay product (PDP) through Delay and Power multiplication for GDI-MUX Full adder and ADVANCE-6T Full Adder. ADVANCE-6T provide better PDP, Voltage Swing Compare to GDI-MUX Full Adder but the same time ADVANCE-6T not lacking on the Basis of Propagation

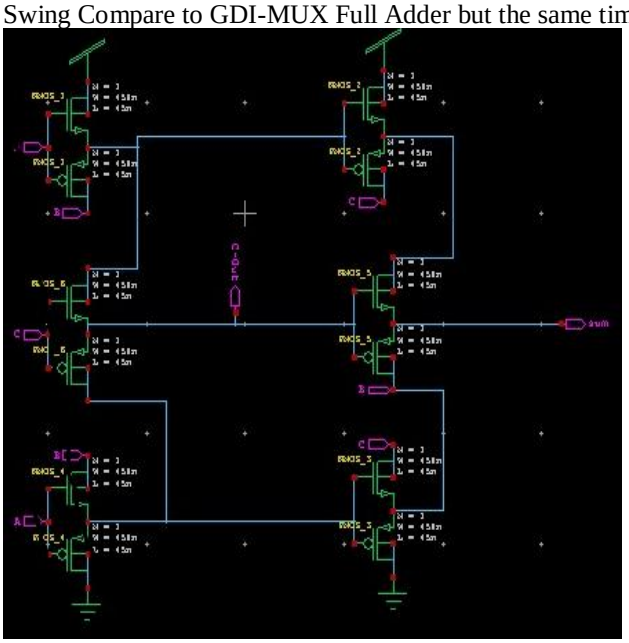

Fig. 4 Schematic Design of GDI-MUX Full Adder

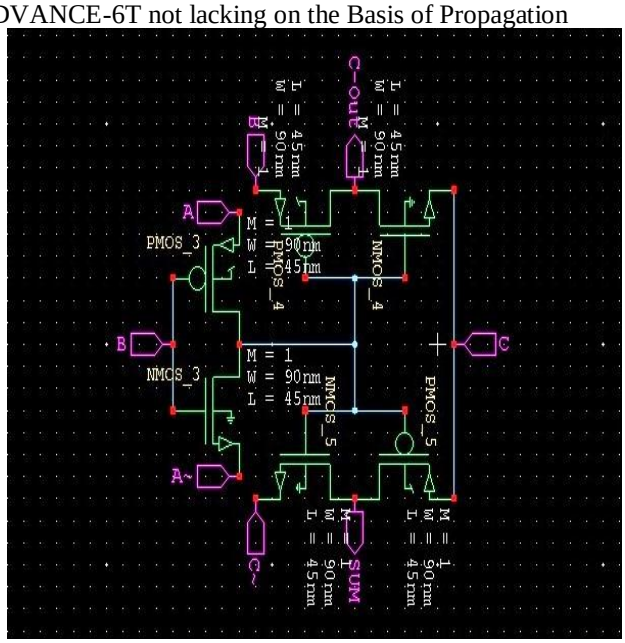

Fig. 7 Schematic Design of Advance 6T Full Adder

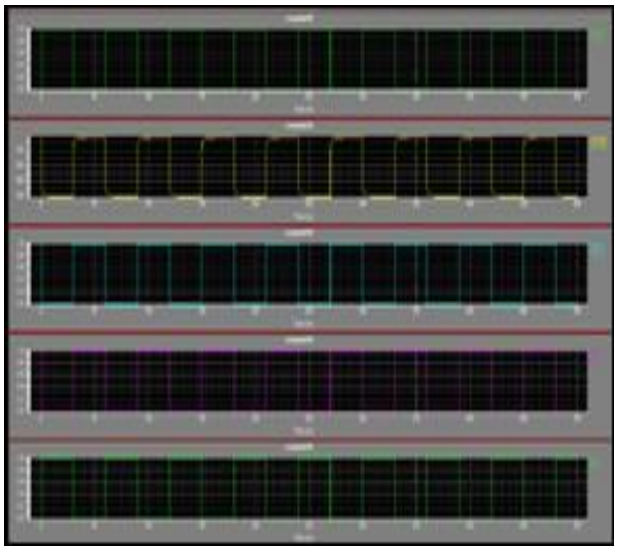

Fig. 5 Simulation Wave form of GDI-MUX Full Adder at 90nm

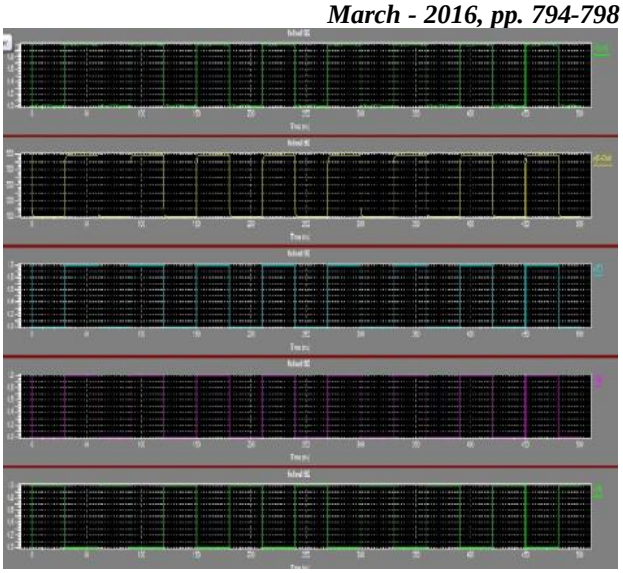

Fig. 8 Simulation Wave form of Advance 6T Full Adder at 90nm

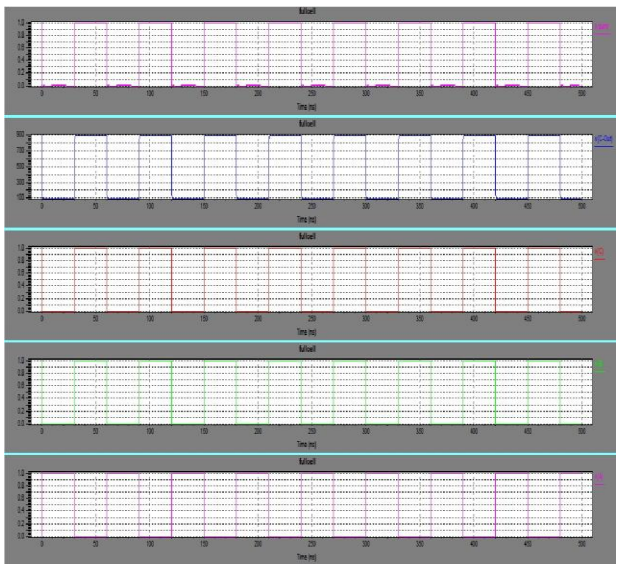

Fig. 6 Simulation Wave form of GDI-MUX Full Adder at 45nm

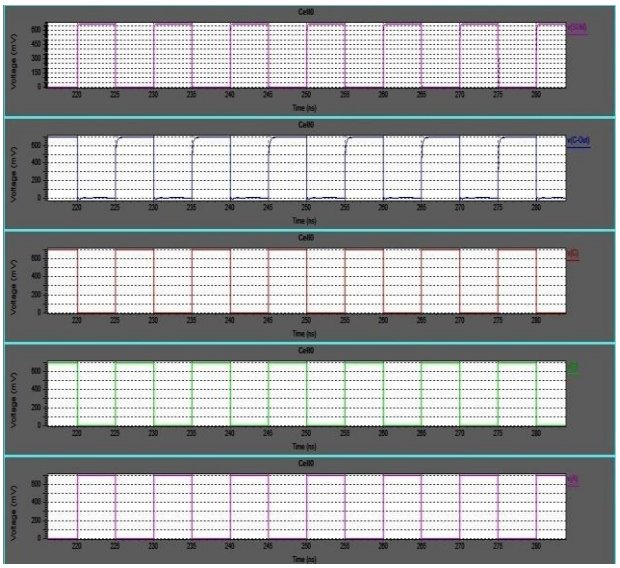

Fig. 9 Simulation Wave form of Advance 6T Full Adder at 45nm

Table: 3 GDI-MUX and ADVANCE-6TResults at 90nm

DESIGN	DELAY ($X10^{-11}S$)	POWER ($X10^{06}W$)	PDP ($X10^{-17}J$)	VDD V
GDI-MUX	2.080	0.386	0.802	0.7
ADVANCE -6T	1.815	0.192	0.348	0.7

Table: 4 GDI_MUX and ADVANCE-6T Results at 45nm

DESIGN	DELAY ($X10^{-11}S$)	POWER ($X10^{06}W$)	PDP ($X10^{-17}J$)	VDD V
GDI-MUX	1.787	0.360	0.643	0.7
ADVANCE-6T	1.012	0.141	0.142	0.7

DELAY

Delay by the GDI-MUX full Adder technique. For each transition, the delay is measured from 50% of the input voltage swing to 50% of the output voltage swing. It is apparent that among the existing full adders, the proposed full adder cell has the smallest delay because of just having six transistors in the critical path for driving the output. The ADVANCE-6T full adder follows the GDI-MUX adder in outperforming the other four full adder cells in delay. Propose full adder in shows the least delay because of removing a extra elementary design to produce internal signals, which is based on Gate Diffusion Input transistor logic.

POWER

The proposed 6T full adder shows the best performance among the above mentioned full adders under varying supply voltages. The ADVANCE-6T full adder utilizes ADVANCE-6T structure as its main cell which is proved in to be one of the lowest power consumer cells that not only is suitable for designing fast, Low- Power circuits but also improves

logic level swing and static power characteristics. GDI-MUX full adder cell follows ADVANCE-6T full adder in outperforming the other full adder cells in power consumption. The GDI full adder cell consume slow static power due to removal of any direct path between Vdd and the ground by employing NMOSs and PMOSs in a complementary manner. The ADVANCE-6T full adder shows minimum power consumption at all supply voltages when compared to the GDI-6T full adder.

POWER-DELAY-PRODUCT (PDP)

The PDP is a quantitative measure of the efficiency and a compromise between power dissipation and speed. PDP is particularly important when low power operation is needed. The Power-Delay- Product for GDI-MUX full adder in two full adder cells is evaluated under different supply voltages (0.8–1.4V) in 90nm and (0.6–1.2V in 45nm. Illustrate the values of PDP of the 1-bit adder based on each full adder cells. Tables 3 and 4 illustrate the values at 0.7V for 90 nm and 0.7 for 45nm. As shown the ADVANCE-6T full adder has the best PDP in comparison with its counterpart.

V. CONCLUSION

In this paper two novel full adder cells using ADVANCE-6T structure and GDI-MUX CMOS logic style for Low-Power application are proposed. These new design successfully operate at low voltages with tremendous signal integrity and driving capability. The circuits being studied are optimized for energy efficiency at 90nm and 45nm PD SOI CMOS process technology. Simulations have been performed on PTM to evaluate the new designs. GDI-6T full adder in and. A broad comparison to the state of the art designs cited in the VLSI literature illustrates a significant improvement in terms of power dissipation and Power- Delay product (PDP) parameter. The number of transistors used is significantly reduced resulting in a great reduction in switching activity and area. This considerable reduction in power by minimizing static and dynamic power dissipation as well as some techniques to enhance the speed of the design leads to the best PDP.

ACKNOWLEDGMENT

The heading of the Acknowledgment section and the References section must not be numbered.Causal Productions wishes to acknowledge Michael Shell and other contributors for developing and maintaining the IEEE LaTeX style files which have been used in the preparation of this template. To see the list of contributors, please refer to the top of file IEEETran.cls in the IEEE LaTeX distribution.

REFERENCES

[1] R. Shalem, E.John, L.K.John, A novel low-power energy recovery full adder cell, in: Proceedings of the Great Lakes Symposium on VLSI, February 1999, pp. 380–383.

[2] R.X. Gu, M.-I.Elmasry, Power dissipation analysis and optimization of deep submicron CMOS digital circuits, IEEE Journal of Solid-State Circuits 31(5) (1996)707–713.

[3] V. Dessard, SOI Specific Analog Techniques for Low-noise ,High-temperature or Ultra-low Power Circuits, Ph.D. Thesis, UCL, Louvain, Belgium,2001.

[4] D. Hassoune, I.O Flandre, Connor, J.D.Legat, ULPFA: a new efficient design of a power-aware full adder, IEEE Transactions on Circuits and Systems—I: Regular Papers 57 (8) (2010).

[5] V. Kilchytska, D.Levacq, L.Vancaillie, D.Flandre, On the great potential of non- doped MOSFETs for analog applications in partially-depleted SOI CMOS process, Solid State Electronics 49 (5) (2005) 708–715.

[6] J.-M. Wang, S.-C.Fang, W.-S.Feng, New efficient designs for XOR and XNOR functions on the transistor level, IEEE Journal of Solid-State Circuits 29 (7) (1994) 780–786.

[7] Arkadiy Morgenshtein, A.Fish, Israel A.Wagner, Gate-diffusion input (PROPOSE-8T): a power-efficient method for digital combinatorial circuits, IEEE Transactions on VLSI Systems (2002) 566–581.

[8] Vahid Foroutan, Mohammad Reza Taheri, KeivanNavi, Arash Azizi Mazreah, Design of two Low-Power full adder cells using PROPOSE-8T structure and hybrid CMOS logic style, INTEGRATION, the VLSI journal 47(2014)48–61.

