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High Speed Area Efficient Linear Convolution using Signed Baugh Multiplier

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Abstract— In this Technical era the high speed and low area of VLSI chip are very- very essential factors. Day by day number of transistors and other active and passive elements are drastically growing on VLSI chip. All the processors of the devices adders and multipliers are played an important role. Adder is a striking element for the designing of fast multiplier. Ultimately here need a fast adder for high bit addition. In this paper, the implemented of linear convolution are based on common Boolean logic and baugh multiplier. Proposing common Boolean logic (CBL) adder provides less components, less path delay and better speed compare to other existing CBL adder and other adders. Here we are comparing the linear convolution of different-different word size from other adders. The design and experiment can be done by the aid of Xilinx 6.2i Spartan device family.

Keywords: - Common Boolean Logic (CBL), Ripple Carry Adder Linear Convolution, Xilinx

I. INTRODUCTION

The processors speed mostly depends on adder design techniques. Adder is the device by which two or more than two bit information can be added. For the high speed processing of the data transfer area must be less of the passive and active element. Adder has two outputs specially sum and carry. For making fast adder carry can be reduced and replaced in different ways. The propagation delay or gate delay of a gate is basically the time interval between the application of the input pulse and the occurrence of the resulting output pulse. The propagation delay is a very important characteristic of logic circuits because it limits the speed at which they can operate. The shorter the propagation delay, the higher the speed of the circuit and vice-versa. Propagation delay should be minimizing as possible as, for high efficient addition. For instance 4 bit addition generally propagation delay is occurred highly. When we add one high bit to another high bit carry is occurred due to normally addition operation. This carry propagates to next bit and now bit addition is performed by 3 bit adder. So carry will propagate to the next bit over and over, this cause propagation delay will be occurred. As we have concerned (see in figure 1) (A_3, A_2, A_1, A_0) bits are added with (B_3, B_2, B_1, B_0) then carry propagation delay bits are occurred notations as(C_2, C_1, C_0). On the other hand propagation delay can be reduced by the aid of suitable structural designing process. For instance full adder can be designed with one XOR gate, three AND gate and one OR gate. That type of designing will provide 8.326 ns propagation delay. On the other hand full adder can be design by using two half adder and one OR gate. This type of designing will provide only 8.036 ns propagation delay. Carry propagation delay can be reduced by using ripple carry adder, fast adder that is also called look a-head carry generator, parallel adder, and specially carry select adder.

	C2 C1 C0	[Carry bits]
	A3 A2 A1 A0	[Augends bits]
+	B3 B2 B1 B0	[Addend bits]
	S3 S2 S1 S0	[Summation bits]

Fig 1: A Propagation delay for four bit binary addition

Now a days, time required in multiplication process is still the dominant factor in determining the instruction cycle time of a DSP chip [3]. Traditionally shift and add algorithm is being used for designing. However this is not suitable for VLSI implementation and also from delay point of view. Some of the important algorithms proposed in literature for VLSI implementable fast multiplication are Booth multiplier, array multiplier and Wallace tree multiplier [4]. Although these multiplication techniques have been effective over conventional "shift and add" technique but their disadvantage of time consumption has not been completely removed. Vedic Mathematics provides unique solution for this problem.
The Baugh-Wooley multiplication is one of the efficient methods to handle the sign bots. This approach has been developed in order to design regular multipliers, suited for 2's complement numbers [2]. Let two n-bit numbers, multiplier (A) and multiplicand (B), to be multiplied.

II. LITERATURE REVIEW

Rashmi K. Lomte et al., (2011, [1]), Convolution and Deconvolution has many applications in digital signal processing. Multipliers and dividers are basic blocks in convolution and deconvolution implementation. They consumes much of time. With advances in technology, many researchers have tried and are trying to design multipliers and dividers which offer either of the following- high speed, low power consumption, regularity of layout and hence less area or even combination of them in multiplier and divider. In this paper, direct method is used to find convolution and deconvolution. Discrete linear convolution of two finite length sequences using Urdhva Triyagbhyam algorithm is presented here. Same algorithm is also used for deconvolution to improve speed. This design approach efficiently and accurately speeds up computation without compromising with area.

Prof J M Rudagi et al., (2011, [2]), Multiplication is an important fundamental function in arithmetic operations. Multiplication-based operations such as Multiply and Accumulate(MAC) and inner product are among some of the frequently used computation Intensive Arithmetic Functions(CIAF) currently implemented in many Digital Signal Processing (DSP) applications such as convolution, Fast Fourier Transform(FFT), filtering and in microprocessors in its arithmetic and logic unit . Since multiplication dominates the execution time of most DSP algorithms, so there is a need of high speed multiplier. Currently, multiplication time is still the dominant factor in determining the instruction cycle time of a DSP chip.

Akhalesh K. Itawadiya et al. (2013, [3]), Digital Signal Processing (DSP) operations are very important part of engineering as well as medical discipline. Designing of DSP operations have many approaches. For the designing of DSP operations, multiplication is play important role to perform signal processing operations such as Convolution and Correlation. The new approach of this implementation is mentally and easy to calculate of DSP operations for small length of sequences. In this paper a fast method for DSP operations based on ancient Vedic mathematics is contemplated.

Surabhi Jain et al. (2014, [4]), In Digital Signal Processing, the convolution and deconvolution with a very long sequence is ubiquitous in many application areas. The basic blocks in convolution and deconvolution implementation are multiplier and divider. They consume much of time. This paper presents a direct method of computing the discrete linear convolution, circular convolution and deconvolution. The approach is easy to learn because of the similarities to computing the multiplication of two numbers. The most significant aspect of the proposed method is the development of a multiplier and divider architecture based on Ancient Indian Vedic Mathematics sutras Urdhvatriyagbhyam and Nikhilam algorithm. The results show that the implementation of linear convolution and circular convolution using vedic mathematics is efficient in terms of area and speed compared to their implementation using conventional multiplier & divider architectures. The coding is done in VHDL. Simulation and Synthesis are performed using Xilinx ISE design suit 14.2.

III. DIFFERENT TYPES OF ADDER

Ripple carry is a combinational circuit for adding more than two bit information. It is also called parallel adder. Ripple carry adder can be designed by using full adder in cascading form. Carry output of first full adder is connected with input of the next full adder, so carry is rippled from one adder to another adder. That is by it is called ripple-carry adder. Let us take example, for designing n bit RCA inputs are $(A_n \dots A_3, A_2, A_1, A_0)$ and $(B_n \dots B_3, B_2, B_1, B_0)$ then carry bits $(C_n \dots C_3, C_2, C_1)$ and summation bits are$(C_{out} \dots S_3, S_2, S_1, S_0)$.

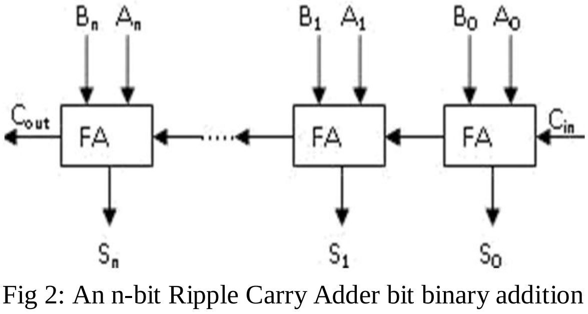

Fig 2: An n-bit Ripple Carry Adder bit binary addition

In this figure all the full adders are connected in cascading form. Carry input C_{in} is an extra input which has fixed value0. First full adder gives the carry output C_1 and summation outputS_0. Carry output of the first full adder is connected with second cascading full adder which will be considered as an input bit.

$$S_0 = (A_0 \oplus B_0) \oplus C_{in} \quad (1)$$

$$S_1 = (A_1 \oplus B_1) \oplus C_1 \quad (2)$$

$$C_{out} = (A_n . B_n) + (C_n . B_n) + (A_n . C_n) \quad (3)$$

- **KOGGE STONE ADDER**

Kogge Stone Adder was proposed by Peter M. Kogge and Harold S. Stone. Kogge Stone Adder is an advanced technology of Look a- head Carry Adder. That is also called parallel prefix adder. It has more area than to Brent Kung Adder but less Fan-out. This adder provides the carry signal time $(O_{logn})$and become fastest adder for industrial level.

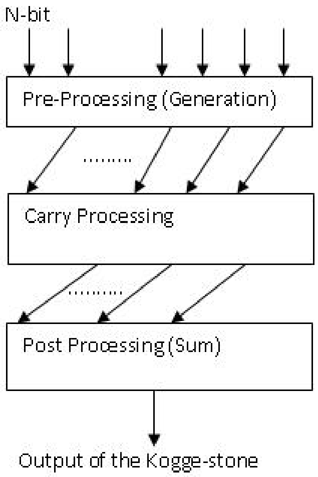

Fig 3: A Block Structure of Kogge Stone Adder **bit** binary addition

First block of KSA is Pre- Processing that will generate and propagate the carry. Processing of carry will be done over the carry processing area and all the carry signal go through the post processing block. In the pre preprocessing stage we find the, generate and propagate signals from each inputs.

$$P_n = A_n \oplus B_n \quad (4)$$

$$G_n = A_n . B_n \quad (5)$$

Carry processing stage provides the carries corresponding to each bit. Execution of these bit operation is carried out from parallel. After finding the carries in parallel they are segmented in to smaller pieces.

$$CP_{n-1} = P_{n-1} \oplus P_n \quad (6)$$

$$CG_{n-1} = (P_n \oplus G_{n-1}) + G_n \quad (7)$$

Bottom block is summation block which provides the summation bits. That blocks are comprised with XOR gate. If one input is different from another then output will be high. And if inputs are same then outputs will be low. Kogge Stone provides the less area than to other parallel adder like carry select adder, carry save adder and look ahead adder.

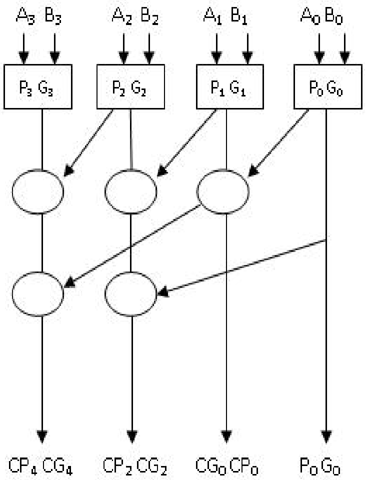

Fig 4: A Functional Diagram of Kogge Stone Adder Stone Adder bit binary addition

Above diagram is a functional diagram of Kogge Stone adder for 4 bit addition. Here elliptically symbol defined as a carry processing stage. The output of the preprocessing stage is fed to next carry stage and post processing as well.

- **MODIFIED COMMON BOOLEAN LOGIC ADDER**

Area and power efficient high speed data logic path are the most significant areas of research. With the help of simple modification in gate level we can achieve the improvement in the results. Speed of the adder depends on the time required to propagate the carry through the adder. These adder works in series format, that is the sum of the elementary position bit is calculated when the previous bits are summed and the carry is propagated to that next stage.

Carry select adder (CSLA) is one of the advanced adders used in data processing processors to perform fast arithmetic function. It focuses on the problem of carry propagation delay by generating the carry independently at each stage and the select the efficient one with the help of multiplexer to perform the sum. The conventional CLSA is RCA (Ripple carry adder) which generate the partial sum and carry by using the input carry condition Cin=0 and Cin=1, select one out of each pair to form final sum and final carry output.

RCA is not area efficient as large number of gates circuitry is used to form the partial products and then the final sum and carry is selected.

Another form of CLSA adder uses binary to excess-1 convertor replacing ripple carry adder with Cin=1. This adder is known as CLSA along with BEC. The number of gates used has been reduced when we have to design large bit adder. This adders is more conventional as compare to RCA when deal with silicon area used but this is having marginally higher delay time.

The proposed Common Boolean Logic (CBL) adder is area-power-delay efficient. It work on the logic to remove the redundant adders and use Common Boolean Logic as compare to conventional carry select adder.

The CBL block is comprised of two parts sum generation block and carry generation block. In sum generation block the output sum is achieved using the multiplex. This multiplex is used to select the output value depeding on the value of Cin(previous bit).

If Cin=0, then output is xor of the two input bits. If Cin=1, then output get inverted. In carry generation block, multiplexer is used to select the carry of next stage depending upon the previous carry input. If Cin=0, cout is OR of two input and if Cin=1 the output carry is AND of the input bit.

$$
\begin{aligned}
&If\ C_{in} = 0 \\
&Sum = A\ XOR\ B \\
&Carry\ A\ OR\ B \\
&else \\
&Sum = NOT\ \ (A\ XOR\ B) \\
&Carry = A\ AND\ B
\end{aligned}
$$

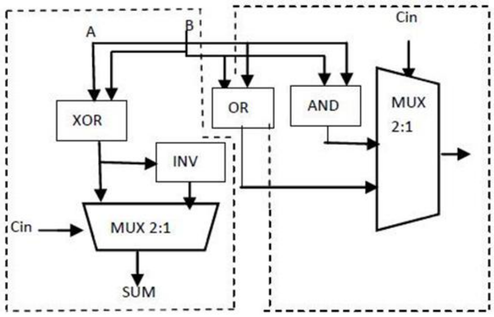

Figure 5: Block Diagram of CBL

This same process is used for the n number of bits and thus we get the final sum and carry as output.

IV. LINEAR CONVOLUTION

Complex logical designing can be reduced by the array mathematics calculation which is consisting with 16 sutras. Number of fan in, fan out pin and input output buffers can be minimized by using these array mathematics sutras. For the high speed convolution, multiplier and adder must be high efficient and low area as possible as. For instance ($A3$, $A2$, $A1$, $A0$) and ($B3$, $B2$, $B1$, $B0$) are the finite length sequence.

For the appropriate output we can use the 4 bit array multiplier, 8 and 9 bit ripple carry adder. Multiplication of convolution input sequence is different from ordinary binary multiplication.

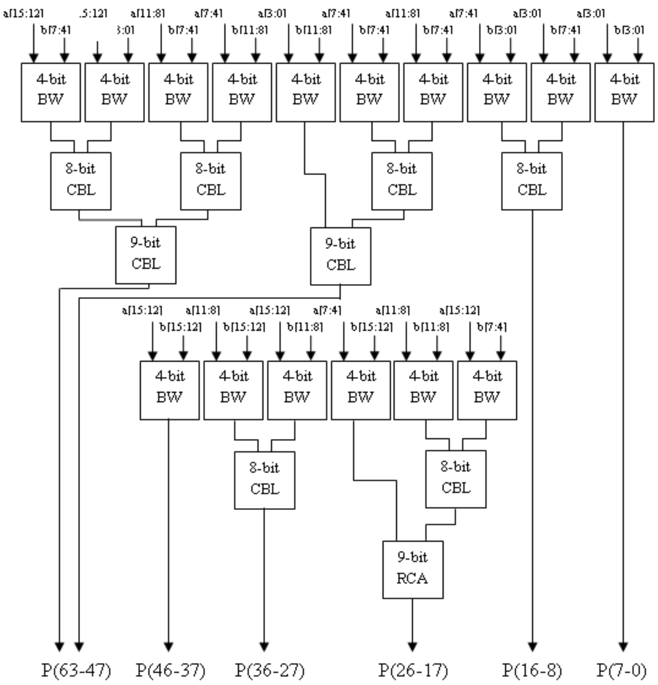

Figure 6: Linear Convolution based on baugh multiplier and CBL adder

V. SIMULATION ANALYSIS

Simulation of these experiments can be done by using Xilinx 14.2I VHDL tool. In this paper we are focusing on propagation delay. Propagation delay must be less for better performance of digital circuit. Xilinx is an analysis is and simulation tools which has many application in research filed. In this tool simulation is divided in to three categories, model, behavioral and structural. Xilinx 14.2i is an updated version which has many merits than other version.

VI. CONCLUSION

Conclusion of this paper is that, designed a low power and less area or minimum propagation delays CBL Adder. According above table (see Table 1) ripple carry adder and other parallel adder has more number of slices than to CBL. Proposing high efficient CBL adder can be used for baugh multiplication to design high speed linear convolution. Apart from that it can be used in high speed convolution methods all the experiment has done in Spartan, Xilinx 6.2I VHDL package.

Table 1: Device Utilizations Summary of 4-input sequence high Speed Linear Convolution

Architecture (4-input Sequence)	Number of Slice	4-input LUTs	Number of IOBs	MCPD (ns)
Surabhi jain et al. [1] (Unsigned)	358	623	96	-
Unsigned Convolution	232	404	76	23.121
Sign Convolution (Parallel Adder + Baugh Wooley Multiplier)	401	704	95	41.039
Sign Convolution (CBL+ Baugh Wooley Multiplier)	255	450	76	24.674

VII. FUTURE SCOPE

Now a day's all the devices need a design with compact and high speed portable components. CBL adder can used to design a fast multiplier and multiplier is an important device for high speed processor. These devices can be used in high efficient convolution and de-convolution, FIR filter, ALU etc.

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