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Analysis Parameter of Area Efficient Vedic Multiplier using Barrel Shifter

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Abstract*—For arithmetic multiplication various Vedic multiplication techniques like Urdhva tiryakbhyam, Nikhilam and Anurupye has been thoroughly discussed. It has been found that Urdhva tiryakbhyam Sutra is most efficient Sutra (Algorithm), giving minimum delay for multiplication of all types of numbers, either small or large. Multiplication requires substantially more hard-ware resources and processing time than addition and sub-traction. Digital signal processors (DSPs) are the technology that is omnipresent in engineering Discipline. Fast multiplication is very important in DSPs for digital filter, convolution, Fourier transforms etc. In this proposed research work an attempt will make for making a novel multiplier using Nikhilam Sutra using Barrel Shifter. Further, the VHDL coding of Urdhva tiryakbhyam Sutra for 8x8 bits multiplication and their FPGA implementation by Xilinx Synthesis Tool on Vertex-7 device family

Keywords: - Digital Signal Processing (DSP), FPGA, BSM Module

I. INTRODUCTION

Multiplication is an important fundamental function in arithmetic operations. Multiplication-based operations such as Multiply and Accumulate(MAC) and inner product are among some of the frequently used Computation- Intensive Arithmetic Functions(CIAF) currently implemented in many Digital Signal Processing (DSP) applications such as convolution, Fast Fourier Transform(FFT), filtering and in microprocessors in its arithmetic and logic unit [1]. Since multiplication dominates the execution time of most DSP algorithms, so there is a need of high speed multiplier. Currently, multiplication time is still the dominant factor in determining the instruction cycle time of a DSP chip. The demand for high speed processing has been increasing as a result of expanding computer and signal processing applications. Higher throughput arithmetic operations are important to achieve the desired performance in many real-time signal and image processing applications [2]. One of the key arithmetic operations in such applications is multiplication and the development of fast multiplier circuit has been a subject of interest over decades. Reducing the time delay and power consumption are very essential requirements for many applications [2, 3]. This work presents different multiplier architectures. Multiplier based on Vedic Mathematics is one of the fast and low power multiplier. Minimizing power consumption for digital systems involves optimization at all levels of the design. This optimization includes the technology used to implement the digital circuits, the circuit style and topology, the architecture for implementing the circuits and at the highest level the algorithms that are being implemented. Digital multipliers are the most commonly used components in any digital circuit design. They are fast, reliable and efficient components that are utilized to implement any operation. Depending upon the arrangement of the components, there are different types of multipliers available. Particular multiplier architecture is chosen based on the application. In many DSP algorithms, the multiplier lies in the critical delay path and ultimately determines the performance of algorithm. The speed of multiplication operation is of great importance in DSP as well as in general processor. In the past multiplication was implemented generally with a sequence of addition, subtraction and shift operations. There have been many algorithms proposals in literature to perform multiplication, each offering different advantages and having tradeoff in terms of speed, circuit complexity, area and power consumption.

The multiplier is a fairly large block of a computing system. The amount of circuitry involved is directly proportional to the square of its resolution i.e. A multiplier of size n bits has n2 gates. For multiplication algorithms performed in DSP applications latency and throughput are the two major concerns from delay perspective. Latency is the real delay of computing a function, a measure of how long the inputs to a device are stable is the final result available on outputs. Throughput is the measure of how many multiplications can be performed in a given period of time; multiplier is not only a high delay block but also a major source of power dissipation. That's why if one also aims to minimize power consumption, it is of great interest to reduce the delay by using various delay optimizations.

The rest of the paper is sorted out as takes after: Literature survey of Vedic multiplier utilizing barrel shifter is introduced as a part of Section II. Brief portrayals of Vedic multiplier are displayed in Section III. Outline of Vedic multiplier utilizing barrel shifter structural planning as a part of Section IV. Confirmed the outcome in area V. Conclusion is introduced in Section VI.

II. SYSTEM DESCRIPTION

Assume that the multiplier is 'X' and multiplicand is 'Y'. Though the designation of the numbers is different but the architecture implemented is same to some extent for evaluating both the numbers. The mathematical expression for modified nikhilam sutra is given below.

$$P = A \times B$$

$$P = 2^{k2}(A \pm C2 \times 2^{(k1-k2)}) \pm C1 \times C2$$

Where k1, k2 are the maximum power index of input numbers A and B respectively. C1 and C2 are the residues in the numbers A and B respectively. The hardware deployment of the above expression is partitioned into three blocks.

- Base Selection Module
- Power index Determinant Module
- Multiplier.

The base selection module (BSM) is used to select the maximum base with respect to the input numbers. The second sub-module power index determinant (PID) is used to extract the power index of k1 and k2. The multiplier comprises of base selection module (BSM), power index determinant (PID), subtractor, barrel shifter, adder/subtractor as sub-modules in the architecture.

III. VEDIC MULTIPLIER

As specified prior, Vedic Mathematics can be isolated into 16 unique sutras to perform scientific counts. Among these the Urdhwa Tiryakbhyam Sutra is one of the most exceedingly favored calculations for performing increase. The calculation is sufficiently able to be employed for the duplication of whole numbers and also binary numbers. The expression "Urdhwa Tiryakbhyam" started from 2Sanskrit words Urdhwa and Tiryakbhyam which mean" vertically" and "transversely" respectively. It depends on a novel idea through which the era of every single fractional item should be possible with the simultaneous expansion of these halfway items. The calculation can be summed up for n x n bit number. Since the incomplete items and their totals are figured in parallel, the multiplier is free of the clock recurrence of the processor. In this way the multiplier will require the same measure of time to figure the item and henceforth is free of the clock recurrence.

The net advantage is that it reduces the need of microprocessors to operate at increasingly high clock frequencies. While a higher clock frequency generally results in increased processing power, its disadvantage is that it also increases power dissipation which results in higher device operating temperatures. The processing power of multiplier can easily be increased by increasing the input and output data bus widths since it has a quite a regular structure. Due to its regular structure, it can be easily layout in a silicon chip. The Multiplier has the advantage that as the number of bits increases, gate delay and area increases very slowly as compared to other multipliers. Therefore it is time, space and power efficient. To illustrate this multiplication scheme, let us consider the multiplication of two decimal numbers (24×16).

Example- 14×12

- The right hand most digit of the multiplicand, the first number (24) i.e., 4 is multiplied by the right hand most digit of the multiplier, the second number (16) i.e., 2. The product 4 X 6 = 24 forms the right hand most part of the answer.

```
 2   4
 1   6
-----
     4
```

- Now, diagonally multiply the first digit of the multiplicand (24) i.e., 4 and second digit of the multiplier (16) i.e., 1 (answer 4 X 1=4); then multiply the second digit of the multiplicand i.e., 1 and first digit of the multiplier i.e., 2 (answer 6 X 2 = 12); add these two i.e., 12 + 4 = 16. It gives the next, i.e., second digit of the answer. Hence second digit of the answer is 6.

```
 2 ↘↙ 4
 1    6
-----
 8    4
```

- Now, multiply the second digit of the multiplicand i.e., 1 and second digit of the multiplier i.e., 1 vertically, i.e., 1 X 1 = 1. It gives the left hand most part of the answer. Thus the answer is 384.

```
 1 ▼  4
 1    2
-----
 3  6  8
```

- Thus the answer is 384.

IV. BARREL SHIFTER ARCHITECTURE

The base selection module and the power index determinant form integral part of multiplier architecture. The architecture computes the mathematical expression in equation1.Barrel shifter used in this architecture. Barrel shifter takes parallel data input and give shifted output either in left or right direction by a specific shift amount. When shift_by input is "000" it will place input data at the output without shifting.

Table 1: Device Summary of Barrel Shifter

Number of slice LUTs	24 out of 218800
Number used as logic	24 out of 218800
Minimum input required time	0.571 nsec
Maximum output required time	1.327 nsec

For specifying shifting direction shift_lt_rt pin is used. When it is '0' the block will perform left shift operation and when it is '1', it will perform right operation.

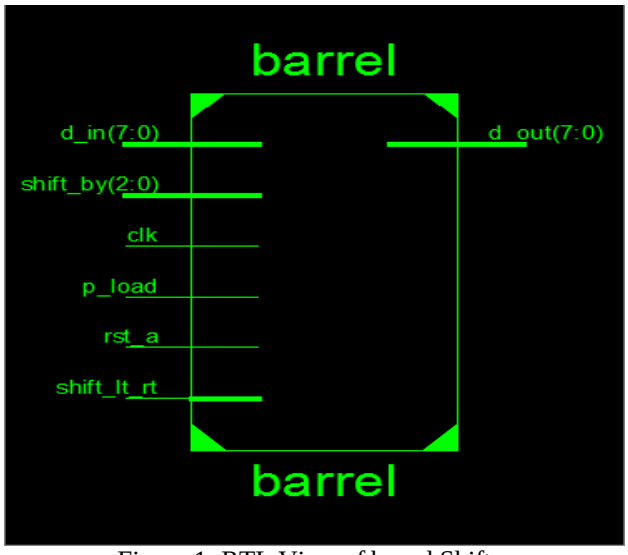


Figure 1: RTL View of barrel Shifter

V. VEDIC MULTIPLIER USING BARREL SHIFTER

The base selection module and the power index determinant form integral part of multiplier architecture. The architecture computes the mathematical expression in equation1.Barrel shifter used in this architecture.

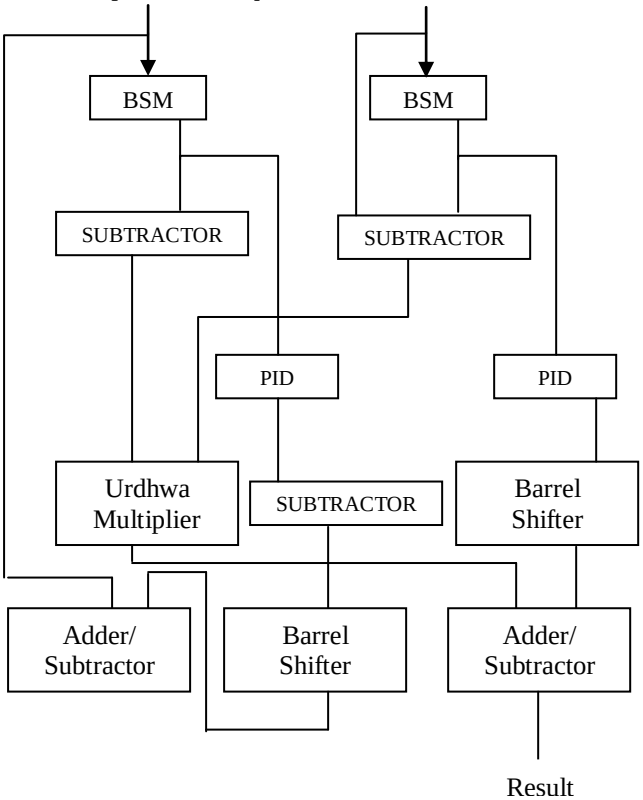


Figure 2: Urdhwa Multiplier using Barrel Shifter

The two input numbers are fed to the base selection module from which the base is obtained. The outputs of base selection module (BSM) and the input numbers 'X' and 'Y' are fed to the subtractors. The subtractor blocks are required to extract the residual parts z1 and z2. The inputs to the power index determinant are from base selection module of respective input numbers.

VI. SIMULATION RESULT

All the designing and experiment regarding algorithm that we have mentioned in this paper is being developed on Xilinx 14.1i updated version. Xilinx 9.2i has couple of the striking features such as low memory requirement, fast debugging, and low cost. The latest release of ISE™ (Integrated Software Environment) design tool provides the low memory requirement approximate 27 percentage low. ISE 14.1i that provides advanced tools like smart compile technology with better usage of their computing hardware provides faster timing closure and higher quality of results for a better time to designing solution. ISE 14.1i Xilinx tools permits greater flexibility for designs which leverage embedded processors.

Table II: Device Summary

Structure	Number of Slice LUTs	MCPD (maximum combinational path delay)
Array Multiplier	879	43.42
Vedic Multiplier	749	27.00
Paven et al. [1]	521	16.753
Proposed multiplier	408	8.547

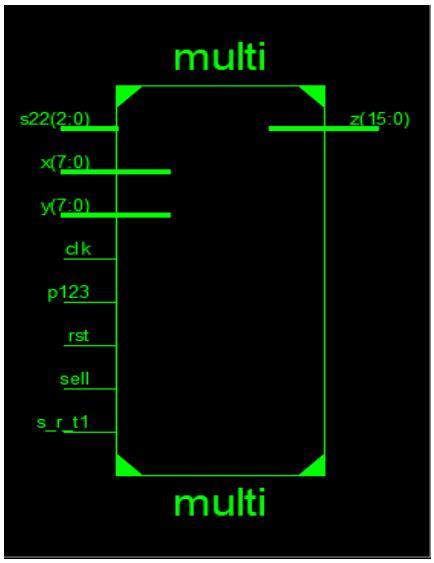


Figure 3: RTL View of Urdhwa Multiplier using Barrel Shifter

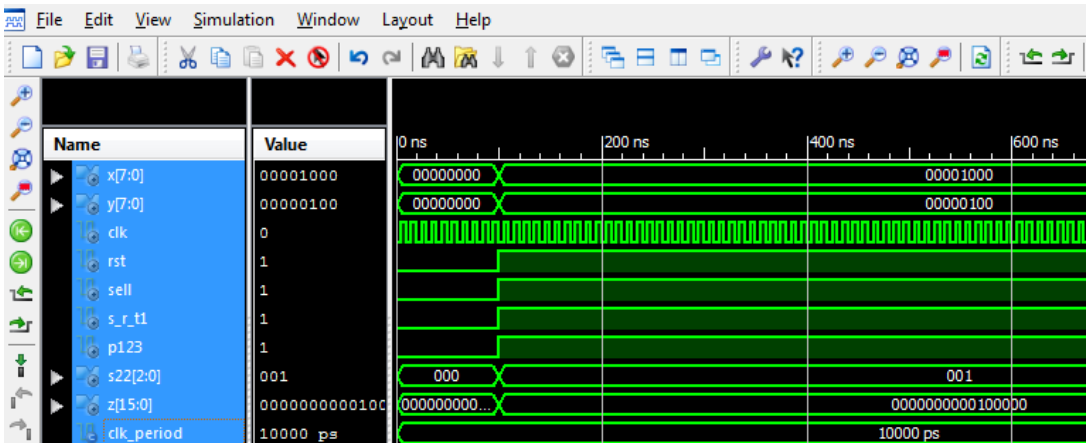
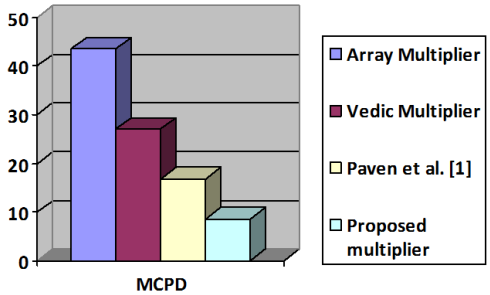


Figure 4: Waveform of Urdhwa Multiplier



VII. CONCLUSION

The high speed implementation of such a multiplier has wide range of applications in image processing, arithmetic logic unit and VLSI signal processing. In our design, efforts have been made to reduce the propagation delay and achieved an improvement in the reduction of maximum combinational path delay with 51% when compared to array multiplier, booth multiplier and conventional Vedic multiplier implementation on FPGA [4].

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