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High Speed and Area Efficient Narrow Band Filter based on Compressor

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Abstract— In this paper, we present the design optimization of high speed area efficient narrow band filter (NBF) sing compressor based multiplier. With the advent of new technology in the fields of VLSI and communication, there is also an ever growing demand for high speed processing and low area design. It is also a well-known fact that the multiplier unit forms an integral part of processor design. Due to this regard, high speed multiplier architectures become the need of the day. In this paper, we introduce a novel architecture to perform high speed multiplication using ancient Vedic math's techniques. Also we design a NBF using compressor based multiplier. This all design and experiments were carried out on a Xilinx Spartan 3e series of FPGA and the timing and area of the design, on the same have been calculated.

Keywords— Narrow Band Filter (FFT), 4:2 Compressor, Xilinx.

I. INTRODUCTION

The performance of digital signal processing and communication systems is generally limited by the precision of the digital input signal which is achieved at the interface between analog and digital information. Sigma-Delta modulation based analog-to digital (A/D) conversion technology is a cost effective alternative for high resolution converters which can be ultimately integrated on digital signal processor ICs. The sigma-delta modulator was first introduced in 1962; but it gained the importance in recent times after the development in digital VLSI technologies. The sigma delta A/D converters are based on digital filtering techniques; almost 90% of the die is implemented in digital circuitry which enhances the prospect of compatibility [1-3].

Conventional converters are often difficult to implement in fine line very large scale integration (VLSI) technology. By keeping these things in mind the people are going for over sampling converters, these converters make extensive use of digital signal processing. The main advantages of the sigma delta A/D converters are mentioned below.

- Higher reliability.
- Increased functionality.
- Reduced chip cost.

Those characteristics are commonly required in the digital signal processing environment of today. Consequently, the development of digital signal processing technology in general has been an important force in the development of high precision A/D converters which can be integrated on the same die as the digital signal processor itself. Conventional high-resolution A/D converters, such as successive approximation and flash type inverters, operating at the Nyquist rate (sampling frequency approximately equal to twice the maximum frequency in the input signal); often do not make use of exceptionally high speeds achieved with a scaled VLSI technology. These Nyquist samplers require a complicated analog low pass filter (often called an anti-aliasing filter) to limit the maximum frequency input to the A/D, and sample-and hold circuitry. The high resolution can be achieved by the decimation process. Moreover, since precise component matching or laser trimming is not needed for the high-resolution sigma delta A/D converters, they are very attractive for the implementation of complex monolithic Systems that must incorporate both digital and analog functions [4].

Azadeh Safari *et al.* (2012, [1]), this paper presents 4-tap orthogonal DWT based on the residue number system. Hardware complexity reduction and design improvement are achieved by employing RNS for arithmetic operations and LUT sharing between low pass and high pass filters. The RNS based DWT is simulated and implemented on the Xilinx FPGA to verify the functionality and efficiency of the design.

Huang C *et al.* (2009, [2]), the present research paper depicts a technique estimating the Field Programmable Gate Array (FPGA) resources utilization for implementation of digital filters with different orders. Its outstanding facility generating Hardware Description Languages (HDLs) for a digital filter object was deployed. Different Very High Speed Integrated Circuit HDL (VHDL) source codes were generated and implemented in Xilinx FPGA device Spartan-3E by increasing filter-order, until the device utilization exceeds the available resources. In this way, a maximum 18th order filter was implementable in FPGA.

Jagannathan *et al.* (208, [3]), in this project an digital signal processing module will be implemented in VHDL on FPGA platform. The digital filtering will be carried out with low pass FIR architecture. Filters shall filter the 50 Hz coupled noise and other high frequency noises. A recorded ECG signal will be used as test input to test the modules implemented on FPGA. The Modelsim Xilinx Edition and Xilinx Integrated Software Environment will be used simulation and synthesis respectively. The Xilinx Chipscope tool will be used to test the results, while the logic running on FPGA. The Xilinx Spartan 3 Family FPGA development board will be used this project.

Ramirez J *et al.* (2000, [4]), heart rate variability (HRV) is defined as oscillation in the interval between consecutive heartbeats as well as the oscillations between consecutive instantaneous heart rates. In a continuous Electrocardiogram (ECG) record, each QRS complex is detected, and the normal-to-normal (NN) intervals (that is, all intervals between adjacent QRS complexes resulting from sinus node depolarization) or the instantaneous heart rate is determined. In this project we will implement four digital filters, namely, low pass filter, high pass filter, notch filter and narrow band filters and demonstrate their use in HRV analysis.

Liu. Y. *et al.* (2004, [5]), WSN is composed of a large number of sensor nodes with multi-hop networking capability that are widely deployed for a wide variety of applications such as health monitoring systems, environment monitoring, interactive user interfaces, etc. One of the most widely used operations in this is finite-impulse response (FIR) filtering. Multiplication is at the core of FIR filter and saving power at the multiplication level can significantly impact the lifetime of a sensor node. In this, we propose design of low power FIR filter and implementations of the same on FPGA. MATLAB is used for an Equiripple or Remez Exchange (Parks-McClellan) technique of FIR filter design. The minimum power achieved is 0.073w in FIR filter based on DA to 626 taps, 8 bits inputs and 9 bits coefficients. The proposed FIR filter has been designed using VHDL, simulated, synthesized and implemented using Xilinx ISE Artix-7 series FPGA and power is analyzed using Xilinx Power analyzer.

II. COMPRESSOR BASED MULTIPLIER

Vedic mathematics is an ancient fast calculation mathematics technique which is taken from historical ancient book of wisdom. Vedic mathematics is an ancient Vedic mathematics which provides the unique technique of mental calculation with the help of simple rules and principles. Swami Bharati Krishna Tirtha (1884-1960), former Jagadguru Sankaracharya of Puri culled set of 16 Sutras (aphorisms) and 13 Sub - Sutras (corollaries) from the Atharva Veda. He developed methods and techniques for amplifying the principles contained in the formulas and their sub-formulas, and called it Vedic Mathematics. According to him, there has been considerable literature on Mathematics in the Veda-sakhas.

Vedic mathematics is part of four Vedas (books of wisdom). It is part of Sthapatya- Veda (book on civil engineering and architecture), which is an upa-veda (supplement) of Atharva Veda. It covers explanation of several modern mathematical terms including arithmetic, geometry (plane, co-ordinate), trigonometry, quadratic equations, factorization and even calculu

- **4:2 Compressor**

To add binary numbers with minimal carry propagation we use compressor adder instead of other adder. Compressor is a digital modern circuit which is used for high speed with minimum gates requires designing technique. This compressor becomes the essential tool for fast multiplication adding technique by keeping an eye on fast processor and lesser area.

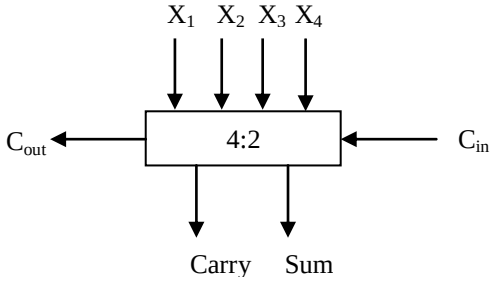


Figure 1: Block Diagram of 4:2 Compressors

III. COMPLEXITY ANALYSIS OF THE NARROW BAND FILTER

It depends on the filter coefficients required to achieve the desired frequency response of the filter. The narrowband filter may be implemented directly or using the multi-rate method. Here we have estimated the required filter coefficients for both these methods to find the complexity of the narrow band filter.

- Specification of the narrowband filter:

Sampling frequency, $F_s = 250Hz$

Pass band ripple, $\delta_p = 0.08dB$

Stop band ripple, $\delta_s = 42dB$

Pass band frequency, $f_p = .825Hz$

Stop band frequency, $f_s = 4.15Hz$

- Direct Approach

Block diagram for implementation of narrow band filter is shown in Figure 2.

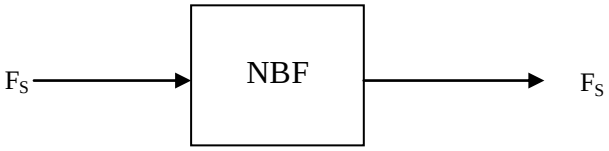


Figure 2: General diagram of narrow band filter

Transition width,

$$\Delta f\,(normalized)\,freq. = {f_s - f_p}/{F_S} \qquad (1)$$

Filter order N Filter order by Kaiser Formulation

$$N = -20\log\sqrt{\frac{\delta_s\delta_p - 13}{14.6\Delta f}} \qquad (2)$$

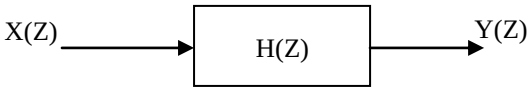
Filter order

$$N = 150 \qquad (3)$$

IV. MULTIRATE APROACH

The process of converting a signal from a given rate to a different rate is called sampling rate conversion. The systems which employ multiple sampling rates in the processing of digital signal are called multi-rate signal processing [5].

Decimation is the processes of lowering the word rate of a digitally encoded signal, which is sampled at high frequencies much above the nyquist rate. It is usually carried out to increase the resolution of an oversampled signal and to remove the out-of-band noise. In a sigma-delta ADC, oversampling the analog input signal by the modulator alone does not lower the quantization noise; the ADC should employ an averaging filter, which works as a decimator to remove the noise and to achieve higher resolutions. A basic block diagrammatic representation of the decimator is shown in Figure 1.The decimator is a combination of a low pass filter and a down sampler. In Figure 1 the transfer function, H(z) is representative of performing both the operations. The output word rate of the decimator is down sampled by the factor M, where M is the oversampling ratio [6]. The function of low pass filtering and down sampling can be carried out using an averaging circuit. The transfer function of the averaging circuit is given by equation (1.1). It establishes a relation between the input and output functions (1.1)



Sampling Frequency f_s

After Decimator Sampling Frequency f_s/M

Figure 3: Block Diagram of Decimator

$$H(Z) = \frac{X(Z)}{Y(Z)} = \frac{1}{M}\sum_{x=0}^{M-1} Z^{-x} \qquad (4)$$

"Up sampling" is the process of inserting zero-valued samples between original samples to increase the sampling rate. (This is called "zero-stuffing".) Up sampling adds to the original signal undesired spectral images which are centered on multiples [7] of the original sampling rate.

"Interpolation", in the DSP sense, is the process of up-sampling followed by filtering. (The filtering removes the undesired spectral images.) As a linear process, the DSP sense of interpolation is somewhat different from the "math" sense of interpolation, but the result is conceptually similar: to create "in-between" samples from the original samples.

The result is as if you had just originally sampled your signal at the higher rate. Increasing the sampling frequency use interpolator

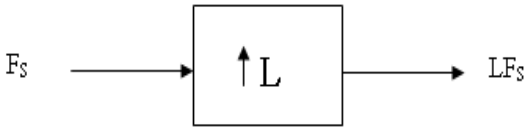


Figure 4: Interpolation with factor L

Since interpolation relies on zero-stuffing you can only interpolate by *integer* factors; you cannot interpolate by fractional factors. (However, you *can* combine interpolation and decimation to achieve an overall rational factor, for example, 4/5

Up-sampling adds undesired spectral images to the signal at multiples of the original sampling rate, so unless you remove those by filtering, the up-sampled signal [7] is not the same as the original: it's distorted.

Some applications may be able to tolerate that; for example, if the images get removed later by an analog filter, but in most applications you will have to remove the undesired images via digital filtering. Therefore, interpolation is far more common [8] that up-sampling alone.

V. SIMULATION RESULT

All the designing and experiment regarding algorithm that we have mentioned in this paper is being developed on Xilinx 14.1i updated version. Xilinx 14.1i has couple of the striking features such as low memory requirement, fast debugging, and low cost. The latest release of ISE^{TM} (Integrated Software Environment) design tool provides the low memory requirement approximate 27 percentage low. By the aid of that software we debug the program easily. Also included is the newest release of the chip scope Pro Serial IO Tool kit, providing simplified debugging of high-speed serial IO designs for Spratan-3 FPGAs.

With the help of this tool we can develop in the area of communication as well as in the area of signal processing and VLSI low power designing. We functionally verified each unit presented in this paper including all three 4:2 Compressor, 7:2 Compressor, Compressor based Multiplier and narrow band filter using compressor based multiplier.

Comparisons Result for different types of proposed design and different types of device family

Design	No. of slices	No. of 4 input LUTs	MCPD (ns)
Sushma R et al.	1179	954	236.847
NBF using Modified Compressor based Multiplier	1124	842	227.719
NBF using Proposed Compressor based Multiplier	1057	754	204.254

VI. CONCLUSION

The narrowband filter is realized in FIR filter. Based on the direct approach, the filter requires 150 filter coefficients to meet the desired frequency response. To implement such a large order FIR filter in hardware involves large resources and sometime difficult to implement in resource constrained application. Keeping this in view, we have used Multirate approach to design the narrowband filter. We have used down sampling factor 2 and 4 for this purpose and found that, down sampling factor 4 requires significantly less filter constants than 2. To implement the narrowband filter, we therefore chosen down sampling factor 4 and designed the decimator, interpolator and narrowband filter. The total number of filter coefficients required to realize the decimator, interpolator and the narrowband filter 64 which is almost 58% less than the direct method.

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