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A Proposed Synthesis of Balanced Quaternary Reversible Logic Gates

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Abstract- ***To realize multi-input quaternary logic functions, quaternary logic synthesis plays a significant role. A balanced quaternary logic contains four balanced states -2, -1, +1 and +2 corresponds to four standard states 0, 1, 2 and 3, respectively. In this paper, we introduce the design of balanced quaternary reversible double Feynman gate, Fredkin gate, Peres gate with their operations. A balanced quaternary Muthukrishnan-Stroud gate (M-S gate) is also introduces in this paper work.***

Keywords- ***Balanced quaternary logic, double Feynman gate, Fredkin gate, Peres gate, M-S gate.***

I. INTRODUCTION

A large number of research works has been done on multi-valued logic synthesis but efficient realization of work is still immature [1]. From these existed works, however, it is evident that balancing in multi-valued logic synthesis is a good choice for researchers. This paper focuses only on the synthesis of balanced quaternary reversible logic gates.

The binary logic with classical computation plays a significant role in quantum computation [2]. Qubit is the memory (information) unit of binary quantum computation with two label states |0> and |1>. By that logical computation, a large computation can be performed by using universal logic gates that operate on a small, fixed number of qubits. But a binary computation has some limitations which are not followed on large computational system, so a ternary logical computation with three label states |0>, |1> and |2> exist [3] [4] [5].

To overcome the complexities of ternary computation, a four states standard computation is required, called standard quaternary computation. That computation uses four label states |0>, |1>, |2> and |3> [6]. Quqtit (quantum quaternary digit) is the memory (information) unit of quaternary quantum computation. To produce the quaternary balanced gates four quaternary balanced states |-2>, |-1>, |+1> and |+2> are used corresponds to the standard quaternary states.

This paper is organized as follows: Section II describes the quaternary galois field arithmetic. Section III presents the background and literature survey of ternary and quaternary reversible logic gates. Section IV describes our proposed work with following the assumptions on balanced quaternary states. Section V summarizes the results of proposed logics. Conclusion of the paper and future scope are shown in section VI.

II. QUATERNARY GALOIS FIELD ARITHMETIC

A Quaternary Galois Field [QGF or GF (4)] is an algebraic structure that consists of the set of elements Q = {0, 1, 2, 3} and two binary operations addition (denoted by +) and multiplication (denoted by. or * or any absence operator). These both operations are defined in Table I and Table II and satisfies the following axioms [7] [8]:

TABLE I GF (4) ADDITION

+	0	1	2	3
0	0	1	2	3
1	1	0	3	2
2	2	3	0	1
3	3	2	1	0

TABLE II GF (4) MULTIPLICATION

·	0	1	2	3
0	0	0	0	0
1	0	1	2	3
2	0	2	3	1
3	0	3	1	2

(A1) Associative law: a + (b + c) = (a +b) + c.
(A2) Commutative law: a + b = b + a.
(A3) a + 0 = a for all a.
(A4) For any a, there is an element (-a) such that a + (-a) = 0 [For GF (4), a = -a for all a].
(M1) Associative law: a · (b · c) = (a · b) · c.
(M2) Commutative law: a · b = b · a.
(M3) a · 1 = a for all a.
(M4) For any a ≠ 0, there is an element a^{-1} such that $a \cdot a^{-1} = 1$
(D) Distributive law: a · (b + c) = (a · b) + (a · c).

III. BACKGROUND AND LITERATURE SURVEY

By analyzing the different research papers, we conclude the important background results are as following in subsections:

A. BASIC REVERSIBLE GATES

A gate is said to be reversible gate if it follows the conditions of [9]. A reversible gate maps n input vectors into n output vectors means n*n vectors [10]. A one-to-one correspondence must be followed by them. By the literature survey of reversibility, we found many reversible gates are as follows: a 1*1 NOT gate [11], 2*2 Feynman gate [12], 3*3 Toffoli gate [11], 3*3 Double Feynman gate [13], 3*3 Peres gate [14] and 3*3 Fredkin gate [15]. Some of them are shown in Figure 1 with their symbolic representation.

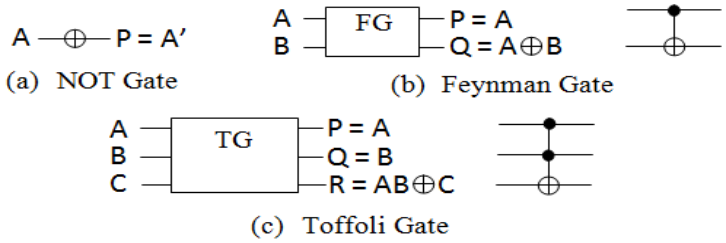

Fig.1 Basic reversible gates: Block diagrams and symbolic forms.

B. BALANCED TERNARY AND QUATERNARY GATES

In 2013 by B. mondal et. al [16], it is shown that a balanced ternary uses three balanced states -1, 0, +1 corresponds to 0, 1, 2 standard states and proposed the different balanced ternary reversible logic gates and circuits, but that is not properly following for higher multi-valued logic. So in 2015 by J.K. Meena et. al [17] proposed quaternary balanced gates and circuits using four balanced states -2, -1, +1, +2 corresponds to 0, 1, 2, 3 standard states for reducing the problems faced in balanced ternary and found the natural circuits representation of balanced quaternary for all multi-valued logic. There are some balanced ternary and quaternary gates which are shown in Figure 2 and Figure 3, respectively.

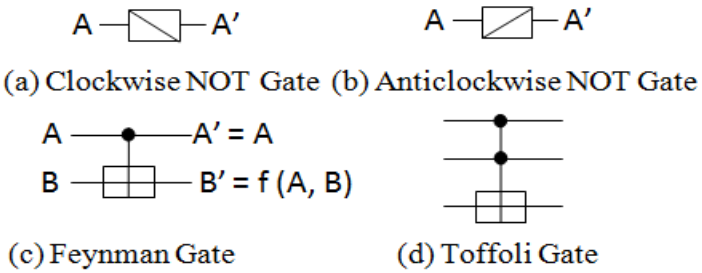

Fig. 2 Balanced Ternary: (a) Clockwise NOT Gate, (b) Anticlockwise NOT Gate, (c) Feynman Gate and (d) Toffoli Gate

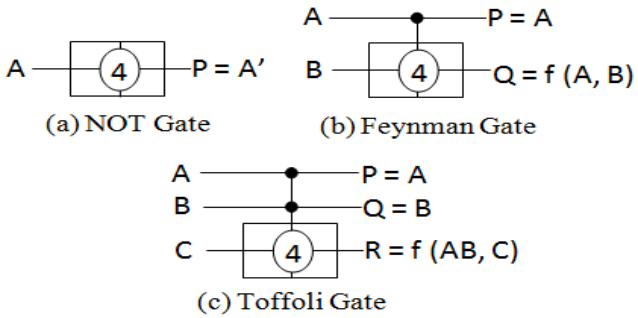

Fig. 3 Balanced Quaternary: (a) NOT Gate, (b) Feynman Gate and (c) Toffoli Gate

C. Muthukrishnan-Stroud Gate (M-S Gate)

M-S gate is a 2*2 reversible logic gate that follows the reversibility condition on the ternary logic when inputs are 0, 1, 2 and same condition is followed when inputs are 0, 1, 2, 3 for quaternary logic. The symbolic representation of standard quaternary is shown in Figure 4 when the controlling input A is 3.

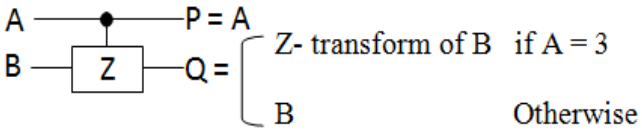

Fig. 4 2-qudit M-S gate family

Here Z is the process of translating the controlled input to the controlled output. A is the controlling input and B is the controlled input. For ternary logic Z can be any one from 6 (3!) shift gates [16] and for quaternary logic it can be any one from 24 (4!) shift gates [7].

IV. PROPOSED WORK

In this paper, we propose four balanced quaternary reversible logic gates with following their symbolic representation, truth table, unitary matrix and their unitary operations. The propose work is as Follows:

A. BALANCED QUATERNARY DOUBLE FEYNMAN GATE

It is a 3*3 reversible logic gate with a combination of two Feynman gates. The symbolic representation of that gate is shown in Figure 5. This gate contains a large truth table (64 rows and 6 columns) shown in Table III.

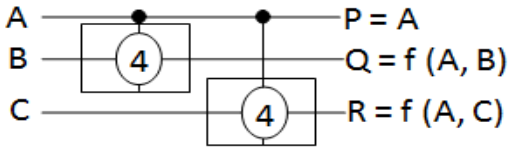

Fig. 5 Symbolic representation of Balanced Quaternary Double Feynman Gate

By following the properties of quaternary balancing its unitary matrix, column vector representation and unitary operations are not shown here, due to its large size, but it is possible not imaginary.

B. BALANCED QUATERNARY PERES GATE

It is a 3*3 reversible logic gate with a combination of a Feynman and a Toffoli gate. The symbolic representation of that gate is shown in Figure 6. This gate contains a large truth table (64 rows and 6 columns) shown in Table IV.

By following the property of quaternary balancing its unitary matrix and operations are not shown here, due to its large size tables, but it is possible not imaginary.

Proposed balanced quaternary reversible Peres gate has same architecture like Half-adder circuit design but it has some differences compare to half-adder like it does not uses ancilla lines, garbage outputs etc.

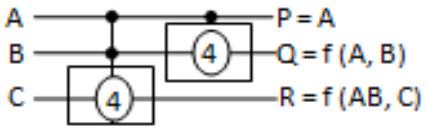

Fig. 6 Symbolic representation of Balanced Quaternary Peres Gate

C. BALANCED QUATERNARY FREDKIN GATE

It is a 3*3 reversible logic gate which contains a balanced quaternary NOT gate and two balanced quaternary Toffoli gate. The symbolic representation of that gate is shown in Figure 7. The truth table of that gate is not shown here due to its large size.

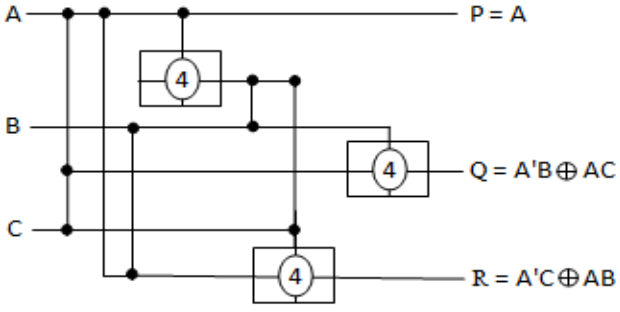

Fig. 7 Symbolic representation of Balanced Quaternary Fredkin Gate

TABLE III TRUTH TABLE OF BALANCED QUATERNARY DOUBLE FEYNMAN GATE

A	B	C	P = A	Q = f(A,B)	R = f(A,C)
-2	-2	-2	-2	-2	-2
-2	-2	-1	-2	-2	-1
-2	-2	+1	-2	-2	+1
-2	-2	+2	-2	-2	+2
-2	-1	-2	-2	-1	-2
-2	-1	-1	-2	-1	-1
-2	-1	+1	-2	-1	+1
-2	-1	+2	-2	-1	+2
-2	+1	-2	-2	+1	-2
-2	+1	-1	-2	+1	-1
-2	+1	+1	-2	+1	+1
-2	+1	+2	-2	+1	+2
-2	+2	-2	-2	+2	-2
-2	+2	-1	-2	+2	-1
-2	+2	+1	-2	+2	+1
-2	+2	+2	-2	+2	+2
-1	-2	-2	-1	-1	-1
-1	-2	-1	-1	-1	+1
-1	-2	+1	-1	-1	+2
-1	-2	+2	-1	-1	-2
-1	-1	-2	-1	+1	-1
-1	-1	-1	-1	+1	+1
-1	-1	+1	-1	+1	+2
-1	-1	+2	-1	+1	-2
-1	+1	-2	-1	+2	-1
-1	+1	-1	-1	+2	+1
-1	+1	+1	-1	+2	+2
-1	+1	+2	-1	+2	-2
-1	+2	-2	-1	-2	-1
-1	+2	-1	-1	-2	+1
-1	+2	+1	-1	-2	+2
-1	+2	+2	-1	-2	-2

TABLE IV TRUTH TABLE OF BALANCED QUATERNARY PERES GATE

A	B	C	P = A	Q = f(A,B)	R = f(AB,C)
-2	-2	-2	-2	-2	-2
-2	-2	-1	-2	-2	-1
-2	-2	+1	-2	-2	+1
-2	-2	+2	-2	-2	+2
-2	-1	-2	-2	-1	-2
-2	-1	-1	-2	-1	-1
-2	-1	+1	-2	-1	+1
-2	-1	+2	-2	-1	+2
-2	+1	-2	-2	+1	-2
-2	+1	-1	-2	+1	-1
-2	+1	+1	-2	+1	+1
-2	+1	+2	-2	+1	+2
-2	+2	-2	-2	+2	-2
-2	+2	-1	-2	+2	-1
-2	+2	+1	-2	+2	+1
-2	+2	+2	-2	+2	+2
-1	-2	-2	-1	-1	-2
-1	-2	-1	-1	-1	-1
-1	-2	+1	-1	-1	+1
-1	-2	+2	-1	-1	+2
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-1	+1	-1	-1	+2	+2
-1	+1	+1	-1	+2	-2
-1	+1	+2	-1	+2	-1
-1	+2	-2	-1	-2	+2
-1	+2	-1	-1	-2	-2
-1	+2	+1	-1	-2	-1
-1	+2	+2	-1	-2	+1

D. BALANCED QUATERNARY MUTHUKRISHNAN-STROUD GATE (M-S GATE)

It is a 2*2 reversible logic gate and its working design from standard quaternary to balanced quaternary is shown with the following steps:

Step1: Changed the balanced quaternary states into their standard quaternary states, respectively.
Step2: Perform the Z-operation on the controlled input when the controlling input is 3, otherwise no change.
Step3: Find the all results in standard quaternary.
Step4: Change the resultant standard quaternary into balanced quaternary.
Step5: Finally, the obtained gate is balanced quaternary M-S gate.

TABLE V RESULT OF BALANCED QUATERNARY MUTHUKRISHNAN-STROUD GATE FAMILY WHEN A = +1

A	B	P	Q
-2	-2	-2	-2
-2	-1	-2	-1
-2	+1	-2	+1
-2	+2	-2	+2
-1	-2	-1	-2
-1	-1	-1	-1
-1	+1	-1	+1
-1	+2	-1	+2
+1	-2	+1	-2
+1	-1	+1	-1
+1	+1	+1	+1
+1	+2	+1	+2
+2	-2	+2	-1
+2	-1	+2	+1
+2	+1	+2	+2
+2	+2	+2	-2

The symbolic representation of that gate is shown in Figure 8 with its balanced quaternary truth table V (here Z is the +1 shift operation).

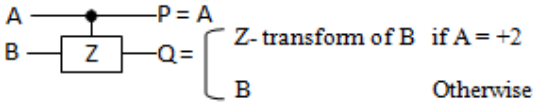

Fig. 8 Symbolic representation of Balanced Quaternary M-S gate

V. RESULTS

In this research paper, we propose some balanced quaternary reversible logic gates and circuits based on the following the assumptions of [17]. The proposed balanced quaternary reversible logic gates and circuits are as following:

- We propose the balanced quaternary reversible double Feynman gate.
- We propose the balanced quaternary reversible Peres gate.
- We propose tha balanced quaternary reversible Fredkin gate.
- We propose the balanced quaternary reversible M-S gate.

VI. CONCLUSION AND FUTURE SCOPE

In this paper, we conclude that four balanced different quaternary reversible logic gate/circuits are proposed based on the following the assumptions of balanced quaternary logic. The all four presented balanced quaternary gates/circuits show itself as natural form, simplifies algorithms and easies synthesis.

By using the help of balanced quaternary assumptions and balanced gates/circuits, this work can be extended in higher multi-valued logic, ALU design and sequential reversible logic circuits.

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