



Review Paper on Reversible Multiplier Circuit using Different Programmable Reversible Gate

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Abstract— Reversible logic circuits are increasingly used in power minimization having applications such as low power CMOS design, optical information processing, DNA computing, bioinformatics, quantum computing and nanotechnology. The problem of minimizing the number of garbage outputs is an important issue in reversible logic design. In this paper we have design 5×5 reversible logic gate using programmable reversible gate. We have used different types of programmable reversible gate i.e. Peres gate (PG) and HNG gate, PG and DPG gate, PG and full adder, PG and MHNG to construct the reversible fault tolerant multiplier circuit. We show that the 5×5 reversible multiplier circuit has lower hardware complexity and it is much better and optimized in terms of number of reversible gates and number of garbage outputs with compared to the existing counterparts.

Keywords— Peres Gate, Toffoli Gate, Reversible Multiplier, Garbage Output, Quantum Cost

I. INTRODUCTION

In modern VLSI system power dissipation is very high due to rapid switching of internal signals. The complexity of VLSI circuits increases with each year due to packing more and more logic elements into smaller volumes. Hence power dissipation has become the main area of concern in VLSI design. Reversible logic has its basics from thermodynamics of information processing. According to this, traditional irreversible circuits generate heat due to the loss of information during computation. In order to avoid this information loss the conventional circuits are modeled using reversible logic. Landauer [1961] showed that the circuits designed using irreversible elements dissipate heat due to the loss of information bits [1]. It is proved that the loss of one bit of information results in dissipation of $KT \cdot \log_2$ joules of heat energy where K is the Boltzmann constant and T is the temperature at which the operation is performed. Benett [1973] showed that this heat dissipation due to information loss can be avoided if the circuit is designed using reversible logic gates [2]. A gate is considered to be reversible only if for each and every input there is a unique output assignment. Hence there is a one to one mapping between the input and output vectors. A reversible logic gate is an n -input, n -output device indicating that it has same number of inputs and outputs. A circuit that is built from reversible gates is known as reversible logic circuit. In this paper, we design 5×5 bit reversible multiplier that can perform multiplier operations simultaneously. All the modules are simulated in modalism SE 6.5 and synthesized using Xilinx ISE 14.1.

II. LITRATURE SURVEY

The research on reversible logic is being pursued towards both design and synthesis. In the synthesis of reversible logic circuits there have been several interesting attempts in the literature such as the work in [2-3]. A reversible arithmetic logic unit was designed by Thomsen, Gluck, and that was based on the V-shaped design of the Van Rentergem adder [5]. Majid Haghparast et al. [3], Reversible logic circuits are of interests to power minimization having applications in low power CMOS design, optical information processing, DNA computing, bioinformatics, quantum computing and nanotechnology. In this paper we a novel 4x4 bit reversible multiplier circuit. The reversible multiplier is faster and has lower hardware complexity compared to the existing counterparts. It is also better than the existing counterparts in term of number of gates, garbage outputs and constant inputs. Haghparast and Navi recently proposed a 4x4 reversible gate called "HNG". The reversible HNG gate can work singly as a reversible full adder. In this paper we use HNG gates to construct the reversible multiplier circuit. The proposed reversible multiplier circuit using HNG gate can multiply two 4-bits binary numbers. The proposed reversible 4x4 multiplier circuit can be generalized for NxN bit multiplication. We can use it to construct more complex systems in nanotechnology.

Md. Belayet Ali et al. [4], Reversible logic circuits are increasingly used in power minimization having applications such as low power CMOS design, optical information processing, DNA computing, bioinformatics, quantum computing and nanotechnology. The problem of minimizing the number of garbage outputs is an important issue in reversible logic design. In this paper we design 4×4 universal reversible logic gate. The reversible gate can be used to synthesize any given Boolean functions. The reversible gate also can be used as a full adder circuit. In this paper we have used Peres gate and the proposed HNG gate to construct the reversible fault tolerant multiplier circuit.

Indrayani Patle et al. [5], This Paper presents the work on implementation of Baugh-Wooley multiplier based on soft-core processor. Micro Blaze soft core is high performance embedded soft core processor developed by XILINX Company. This soft core enjoys high configurability and allows designer to make proper choice based on his own design requirements to build his own hardware platform. Custom hardware of power optimized Baugh-Wooley signed multiplier is interface with Micro Blaze soft core processor. The major objective for using hardware for realizing Baugh-Wooley multiplier is to utilize hardware for realizing fast and efficient processing capacity.

Hatkar A. P. et al. [6], Reversible logic is very much in demand for the future computing technologies as they are known to produce low power dissipation having its applications in Low Power CMOS, Quantum Computing, Nanotechnology, and Optical Computing. Adders and multipliers are fundamental building blocks in many computational units. In this paper we have presented and implemented reversible Wallace signed multiplier circuit in ASIC through modified Baugh-Wooley approach using standard reversible logic gates/cells, based on complementary pass transistor logic and have been validated with simulations, a layout vs. schematic check, and a design rule check. It is proved that the multiplier is better and optimized, compared to its existing counterparts with respect to the number of gates, constant inputs, garbage outputs, hardware complexity, and number of transistors required.

III. REVERSIBLE GATES

Reversible logic is gaining importance in areas of CMOS design because of its low power dissipation. The traditional gates like AND, OR, XOR are all irreversible gates. Consider the case of traditional AND gate. It consists of two inputs and one output. As a result, one bit is lost each time a computation is carried out. According to the truth table there are three inputs (1, 0), (0, 1) and (0, 0) that corresponds to an output zero. Hence it is not possible to determine a unique input that resulted in the output zero. In order to make a gate reversible additional input and output lines are added so that a one to one mapping exists between the input and output. This prevents the loss of information that is main cause of power dissipation in irreversible circuits. The input that is added to an $m \times n$ function to make it reversible is known as constant input (CI). All the outputs of a reversible circuit need not be used in the circuit. Those outputs that are not used in the circuit is called as garbage output (GO). The number of garbage output for a particular reversible gate is not fixed. The two main constraints of reversible logic circuit is

- Fan out not allowed
- Feedbacks or loops not allowed.

o BASIC REVERSIBLE GATES

Several reversible gates have come out in the recent years. The most basic reversible gate is the Feynman gate and is shown in figure 1. It is the only 2x2 reversible gates available and is commonly used for fan out purposes. Consider the input B as constant. When B is zero, the gate acts as a copying gate or a buffer where both the output lines contain the input A. When B is one, the complement of A is obtained at the output Q. The 3x3 reversible gates include Toffoli gate, Fredkin gate, new gate and Peres gate, all of which can be used to realize various Boolean functions. Fredkin gate is shown in figure 2.

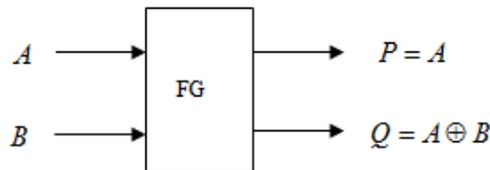


Figure 1: Feynman Gate

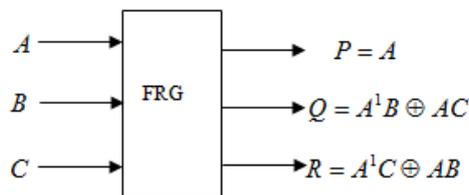


Figure 2: Fredkin Gate

Figure 3 shows the Peres gate. Some of the 3x3 gates are designed for implementing some important combinational functions in addition to the basic functions. Most of the above mentioned gates can be used in the design of reversible multiplier.

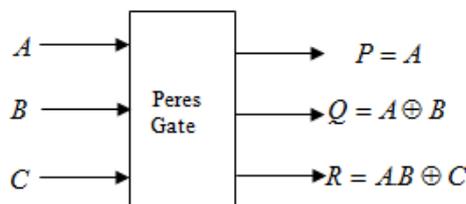


Figure 3: Peres Gate

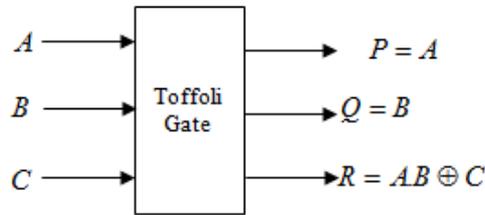


Figure 4: Toffoli Gate

The Toffoli gate is a 3X3 gate has quantum cost of 5 and garbage outputs of 2. The Peres gate is also a 3X3 reversible gate whose quantum cost is 4 and garbage outputs are 2.

Several 4x4 gates have been described in the literature targeting low cost and delay which may be implemented in a programmable manner to produce a high number of logical calculations. The HNG gate, presented in [7], produces the following logical output calculations:

$$P = A \quad (1)$$

$$Q = B \quad (2)$$

$$R = A \oplus B \oplus C \quad (3)$$

$$S = (A \oplus B).C \oplus (AB \oplus D) \quad (4)$$

The quantum cost and delay of the HNG is 6. When $D = 0$, the logical calculations produced on the R and S outputs are the required sum and carry-out operations for a full adder. The block diagram of the HNG is presented in Fig. 5.

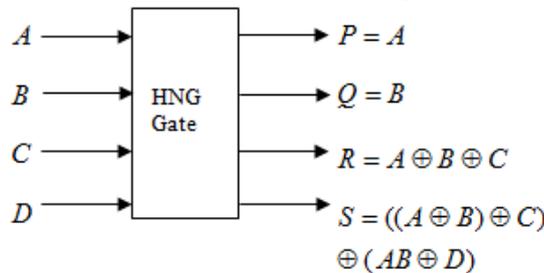


Figure 5: HNG Gate

IV. REVERSIBLE MULTIPLIER

To compute product of two signed numbers we have used modified Baugh-Wooley approach [8]. Both logical and reversible multiplier design is divided into two parts: partial product generation circuit and then multi-operand addition circuit.

Design of Logical Multiplier:-

First to compute partial product, we used 17 AND and 8 NAND employing the procedure given in figure 6. After generating partial products, next step is a multi-operand addition. We should add the bits of each column given in figure 6. To add these bits, we need FA and HA. We have to add these bits in the way that our circuit will give the best results. Figure 6 shows the way of adding these bits in our proposed circuit. The Wallace approach has been used to construct a circuit with less delay. To minimize delay in our proposed circuit, P_9 is computed by inverting carry output from earlier FA (FA13). The resulting circuit for multi-operand addition needs one 1-NOT gate, 4-HA and 16-FA.

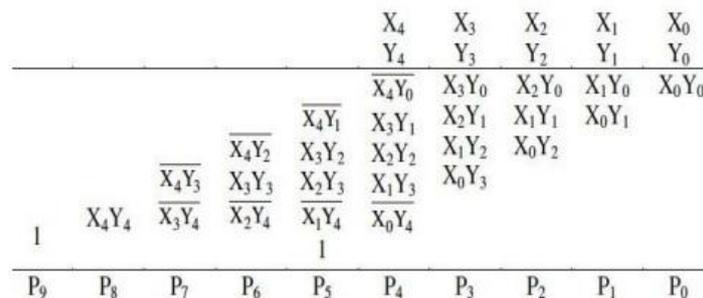


Figure 6: Baugh-Wooley 5 x 5 Signed Multiplier

Design of reversible multiplier:-

The operation of the 5x5 multiplier is depicted in figure 7. It consists of 25 partial product bits of the form X_iY_i . The reversible 5x5 multiplier circuit has two parts. First, the partial products are generated in parallel using Toffoli gate. We used 25 Toffoli gates to create 17 ANDs and 8 NANDs as shown in figure. The modified partial the last low replace by Peres gate because Peres gate has quantum cost of 4 as shown if figure 8.

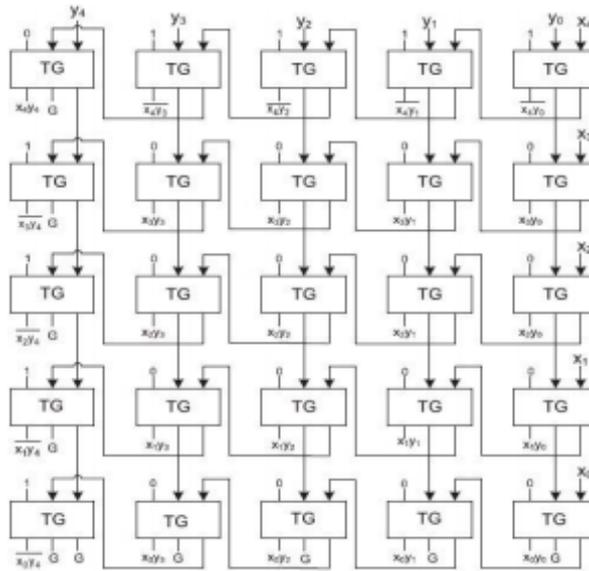


Figure 7: Partial Product Generation by Toffoli Gates

Next step is a multi-operand addition. After generating partial products, we should add the bits of each column given in Hatkar A.P. et al. [6]. To add these bits, we need FA and HA. We have to add these bits in the way that our circuit to give the best results.

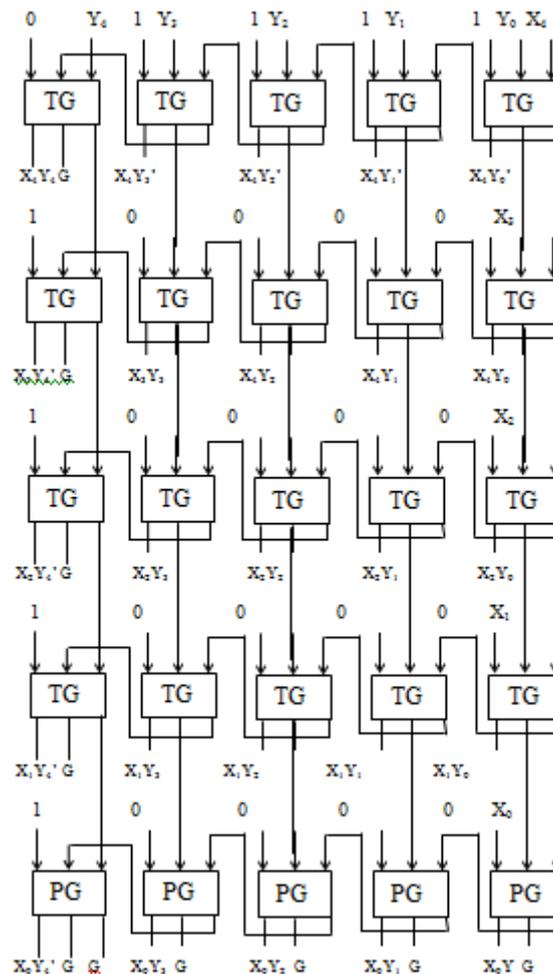


Figure 8: Modified Partial Product Generation by Toffoli Gates and Peres Gate

V. SIMULATION RESULT

The proposed reversible multiplier circuit is more efficient than the existing circuit presented by [6], [7], [8] and [9]. The proposed reversible multiplier circuit is divided two part i.e. partial product circuit and multi-operand addition. The proposed partial product is minimize 5 quantum cost in the design. Increase the number bit of the reversible multiplier circuit so reduced the quantum cost.

Table I: Comparative results of partial product generation circuit

Method	No. of Gate	No. of garbage output	Hardware Complexity	Quantum Cost
Proposed	25	10	$25\alpha+25\beta$	120
[6]	25	10	$25\alpha+25\beta$	125
[7]	25	10	$34\alpha+25\beta$	135
[8]	25+20	30	$45\alpha+25\beta$	145
[9]	25+25	35	$45\alpha+30\beta$	155

Table II: Comparative results of reversible signed multiplier circuit

Method	No. of Gate	No. of garbage output	Hardware Complexity	Quantum Cost
Proposed	45	46	$25\alpha+25\beta$	232
[6]	45	46	$113\alpha+61\beta$	237
[7]	45	46	$122\alpha+61\beta$	228
[8]	65	70	$205\alpha+105\beta$	-
[9]	85	80	$275\alpha+132\beta$	-

VI. CONCLUSION

In this paper we presented and successfully implemented Wallace reversible signed multiplier circuit. It is proved that not only the proposed multiplier is better and optimized, compared to its existing counterparts with respect to the number of gates, garbage outputs, hardware complexity, and quantum cost.

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