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A Survey on Different CMOS Full Adder Design Techniques

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Abstract: -Full adder is the basic and most common element in the designing of basic arithmetic circuits like Adders, Substractors, Multipliers, and Dividers etc. It is the heart of Arithmetic and Logic Unit. Any change in the adder cell will degrade the overall performance of the designed circuit, so high care must be taken while designing these adder cells. The paper proposes a survey on different CMOS full adders design methodologies, each have its own advantages and disadvantages. A new hybrid design which is a combination of Transmission gate and pass transistor logic is proposed. A comparison is also made on the basis of area, power and delay to find out the best Possible design technique.

Key Words— Full adder, hybrid design, CMOS technologies, delay.

I. INTRODUCTION

Full adder is a core unit in many of the electronic devices that performs arithmetic and logical operations. It is the basic element in many of complex arithmetic circuits like adders, multipliers, dividers, exponentiation, comparators parity checkers etc[1][5-7]. Most of the VLSI applications, such as Digital Signal Processing (DSP), image processing, video processing and microprocessors extensively use arithmetic operations. Binary addition is considered as the most crucial and important part of the arithmetic unit because all other arithmetic operations involve addition. Therefore, making the full adder cell efficient, reducing its delay, area and increasing its speed, will reduce the overall delay of the whole system. That's why design of low-power, high performance full adder cells are of great interest and any modifications made to the full adder would affect the whole system. In current VLSI technology designs delay and power consumption improvement are the most important performance parameters of a circuit. To reach this goal, reduce scaling of the feature size is mostly prefered. In complementary metal oxide semiconductor (CMOS) technology, reducing the length of channel to below about 65nm leads to critical problems and challenges such as decreasing gate control, short channel effect, high power density, high sensitivity to process variation and exponential leakage current increment[2]. For this reasons reducing the transistors size finally will stop at a point, leading to taking advantage of new technologies that do not have above problems may be felt. The vast use of this operation in arithmetic functions attracts many researchers to this field. In recent years several variants of different logic styles have been proposed to implement 1-bit adder cells.[11][12-17]

The main focus of the work presented here is to compare different CMOS full adder design methodologies and to introduce a new design technique which is a combination of TG and PT logic style.

II. BASIC CMOS FULL ADDER

Full Adder is a combinational circuit with three inputs i.e. A, B and C and two outputs i.e. SUM and CARRY. It is one of the basic building blocks of the digital design.[2]-[5] The truth table of full adder is shown in table 1

TABLE 1 TRUTH TABLE OF FULL ADDER

A	B	C	SUM	CARRY
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

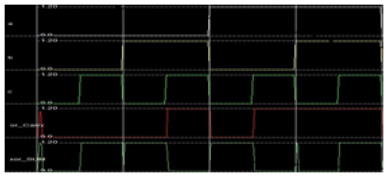

Figure 1 Waveform Of Full Adder

SUM = A XOR B XOR C
CARRY = AB + BC + CA

The CMOS structure combines PMOS pull-up and NMOS pull-down networks to produce considered outputs. In this style all transistors are arranged in completely separate branches, each may consist of several sub-branches. Mutually exclusiveness of pull-up and pull-down networks is of a great concern. Figure 2 shows the conventional CMOS 28-transistor adder

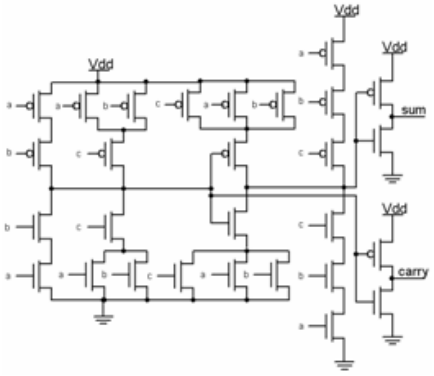

Figure 2.Conventional CMOS full adder

III. REVIEW OF DIFFERENT FULL ADDER DESIGN

Hybrid adders consist of more than one logic styles in its implementation they are classified in various categories depending upon their output structure and signals.

A. Design Approaches for Full Adder Module.

Adder topologies are based on basic two circuits: one to generate H (XOR) with H (XNOR), and the other to generate the Sum output function as shown in Figure 3. The Carry signal is obtained by using one MUX (multiplexer).[8]

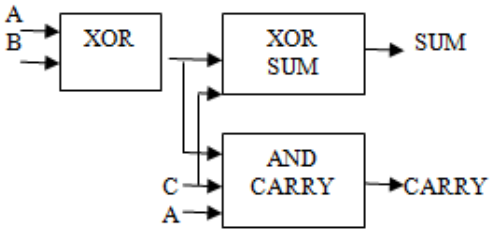

Figure 3 Basic Design Approach For Hybrid Full Adder

Sum = A XOR B XOR C and Carry = AB + C (AXOR B)
Powerless P-XOR and Groundless G-XNOR are as new set of low power. The P-XOR and GXNOR consumes less power than other design because it has no power supply or ground connection.[8]

B. 10T Full Adder

This designs of 10T adder requires two XOR operations to calculate the Sum function. Each XOR operation requires 4T transistors. 2X1 MUX is used for Carry function implemented using two transistors, the module having lowest propagation delay amongst all the 10T full adder circuits.[4][13]

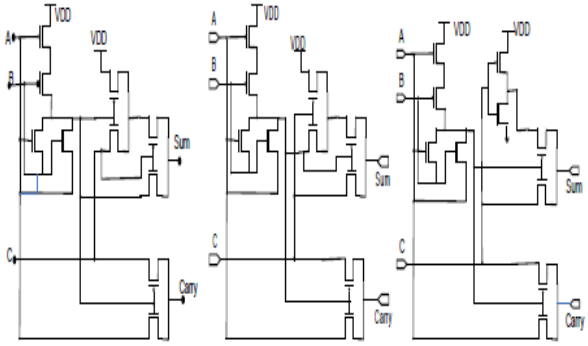

Figure 4(a) 9A Full Adder (b)9B Full Adder (c)13A Full Adder

The 9A full adder is shown in Figure 4(a), implements 4- transistor XOR-XNOR circuit, 4-transistor groundless XNOR circuit and 2X1 multiplexer.
The 9B full adder has shown in Figure 4(b), implements using 4-transistor XORXNOR circuit, 4-transistor groundless XNOR circuit and 2X1 multiplexer.

A transistor –level implementation for 10 transistor full adder 13A is shown in Figure 4(c). 10 transistors full adders 13A and 9B have better critical delay than the 10 transistors SERF full adder in all loading condition.[4][12]

C. 14 T and 16T Full Adder with Full Swing output Logic

A full adder circuit 14T & 16T has been designed using low power 4T XOR-XNOR design and transmission gates as shown in Figure 5. 14T transistors utilizes the low power XOR/XNOR circuit and a pass transistor network to produce a non full swing sum signal and uses four transistors to generate a full swing carry signal, which do not provide enough driving power .

A 16T adder is derived from the 14 transistors circuit, which has 16 transistors, generates full swing XOR and XNOR signals by utilizing a pass transistor based DCVS circuit.[4]15]

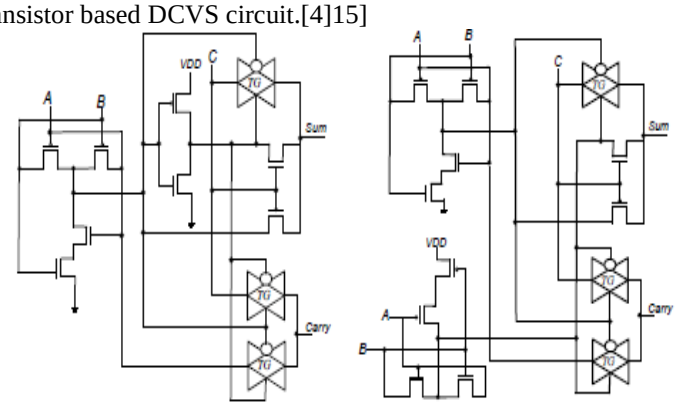

Figure 5 (a) 14 T Full Adder (b) 16 T Full Adder

D. DOUBLE PASS TRANSISTOR WITH ASYNCHRONOUS ADIABATIC LOGIC DPTAAL

Asynchronous adiabatic full adder cell logic uses double pass-transistor logical block with C&R structures. It has been designed and tested to get the best power efficiency. It is a full adder cell, with the logical part designed using DPTAAL, and whereas the control part of the C&R block and regeneration part is made of pass-transistor logic[3].

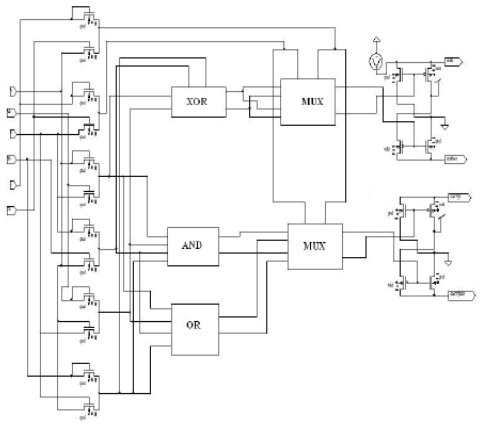

Figure 6 DPTALL Full Adder

E. SERF Full Adder

The Static Energy Recovery Full adder (SERF) is a 10 transistor (10T) adder shown in Figure 7. The circuit is claimed to be extremely low power consuming because it does not contain direct path to the ground . The elimination of the path to the ground reduces the total power consumption by reducing the short circuit power consumption.[4][11]

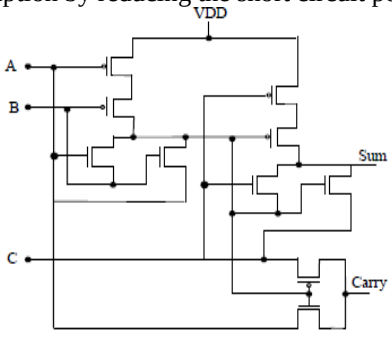

Figure 7 SERF Full Adder

There are some problems in this circuit. First Sum is generated from two cascaded XNOR gates which leads a long delay. Second, it cannot work correctly with a low voltage.

E. CLRCL Full Adder

Threshold loss problem in a 10T full adde can be removed in a Complementary and Level Restoring Carry Logic (CLRCL) figure 8 full adder. In the CLRCL adder, 2X1 MUX and. CMOS inverters are used to realize the Sum and Carry functions. [17]

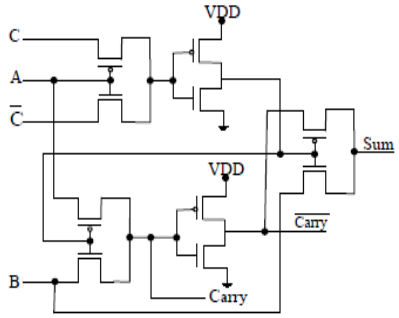

Figure 8 CLRCL based adder

The limitation of CLRCL full adder design is a skew between inputs to the various sub-sections in CLRCL full adder.

F. USING GDI LOGIC

The full adder is designed using Gate Diffusion Injection technique.It outperforms the adder based on CMOS PTL and Transmission gate. The proposed adder achieves better performance in terms of delay and power consumption. The design requires 21 Transistor.[1]

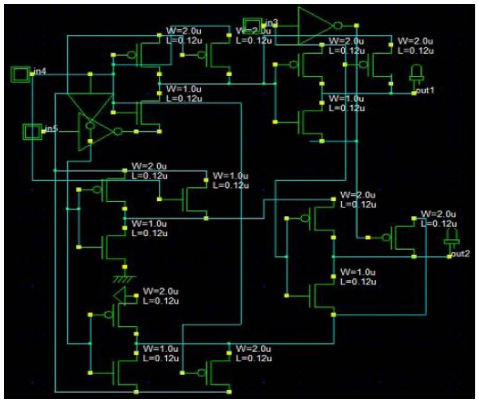

Figure 9 GDI logic Full Adder

IV. PROPOSED PT & TG BASED ADDER.

Pass transistor logic designing is an attractive approach as few number of transistors are required to implement various important logic functions. It is faster than conventional CMOS and also having an additional advantage of smaller transistor sizes and capacitances. A new sum circuit using pass transistor logic in proposed here. The design requires 8 Transistors to perform the sum function. While carry function is implemented using Transmission gate which also requires 8 transistors.

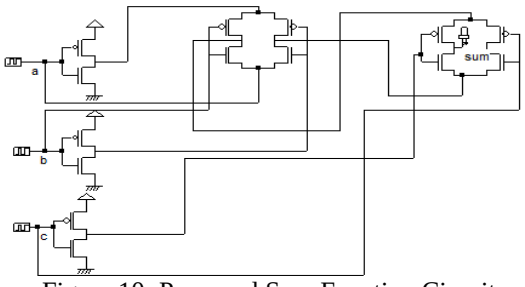

Figure 10: Proposed Sum Function Circuit

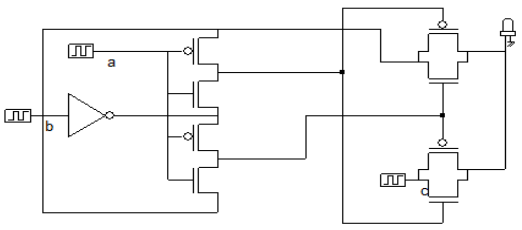

Figure 11: Proposed Carry Function Circuit

The logic function for sum and carry is.

$$SUM = a \text{ XOR } b \text{ XOR } c$$

$$Carry = a.b + a.c + b.c$$

A total of 16 Transistors are needed to implement the design. The advantage of having a Hybrid Design methodology helps in reducing the delay and area which overall reduce the overall PDP of the circuit.

V. SIMULATION RESULTS

Simulation of the proposed design has been performed in CMOS 120 nm technology in Microwind at room temperature (27^0C). Transistor sizes are kept at default for 120nm. The layout and waveform of sum and carry is shown in fig 12 and 13.

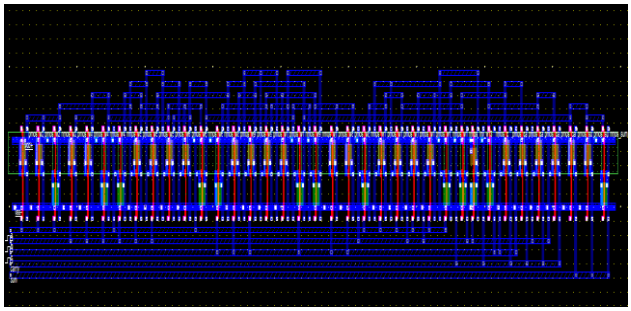

Figure 12: Layout of proposed Sum and Carry Function Circuit in CMOS 120nm technology

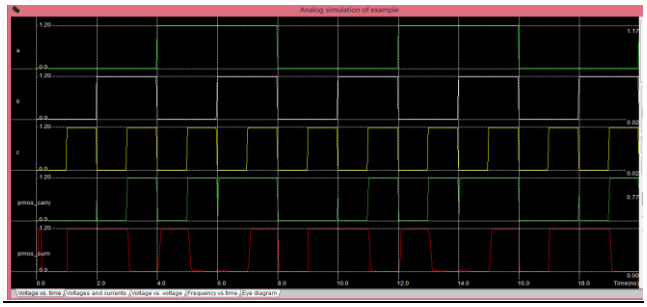

Figure 13:Simulation result of proposed Sum and Carry Function Circuit

VI. CONCLUSION

A survey is done for different design methodology for full adder .The standard implementation of full adder (FA) uses CMOS Logic which requires 28 transistors and consists of both pull up and pull down transistor. The input capacitance is large due to increase in transistor count. A new design using PT and TG logic is proposed here which requires 16 transistors The lesser number of transistor realization is possible using pass transistor logic for Sum .The full adder carry designed using transmission gate consists of PMOS and NMOS connected in parallel controlled by the gate. The design proposed will have less area and a better power delay product.

REFERENCE

[1] Shoba Mohan, Nakkeeran Rangaswamy "Performance Analysis of 1 bit Full Adder Using GDI Logic" ICICES2014 S.A.Engineering College, Chennai, Tamil Nadu, India ISBN No.978-1-4799-3834-6/14/$31.00©2014 IEEE

[2] Mehdi Masoudi1, Milad Mazaheri1, Aliakbar Rezaei1 and Keivan Navi , "Designing High-Speed, Low-Power Full Adder Cells Based On Carbon Nanotube Technology" International Journal of VLSI design & Communication Systems (VLSICS) Vol.5, No.5, October 2014.

[3] A.Kishore Kumar, Dr.D.Somasundareswari, Dr.D.Duraisamy G.Sabarinathan "Asynchronous Design of Energy Efficient Full Adder", 2013 International Conference on Computer Communication and Informatics (*ICCCI* - 2013), Jan. 04 – 06, 2013, Coimbatore, INDIA.

[4] Subodh Wairya, Garima Singh,Vishant, R. K.Nagaria, S. Tiwari Design Analysis of XOR (4T) based Low Voltage CMOS Full Adder Circuit INSTITUTE OF TECHNOLOGY, NIRMA UNIVERSITY, AHMEDABAD – 382 481, 08-10 DECEMBER, 2011.

[5] John P. Uyemura, "Introduction to VLSI circuits and systems," Wiley John & Sons, Inc, 2002.

[6] N. Weste, D. Harris, "CMOS VLSI Design," Pearson Wesley, 2005.

[7] A.P. Chandrakasan, S. Sheng and R. W. Bordersen, "Low-power CMOS digital design," *IEEE J. Solid-State Circuits, vol*. 27, pp. 473- 483, April 1992.

[8] Uming Ko, PorasT.Balsara and Wai Lee, "Low-Power Design Techniques for High-Performance CMOS Adders,*" IEEE Trans. On very Large Scale Integration (VLSI) Systems*, vol. 3, no.2, pp. 327-333, June 1995.

[9] Ahmed M. Shams, and Magdy A. Bayoumi, "A Novel High- Performance CMOS 1-Bit Full-Adder Cell," *IEEE Trans. on Circuits & Systems. II*, Analog and Digital Signal Processing, vol. 47, no. 5, pp. 478–481, May 2000.

[10] D. Radhakrishnan, "Low-voltage low-power CMOS full adder," *Proc. Inst. Elect. Engg. Circuits Devices Systems*, vol. 148, no. 1, Feb. 2001, pp. 19-24.

[11] Sumeer Goel, Ashok Kumar, Magdy A. Bayouni, "Design of Robust, Energy-Efficient Full Adders for Deep-Submicrometer Design Using Hybrid-CMOS Logic Style," *IEEE Trans. on Very Large Scale Integration (VLSI) Systems*, vol. 14, no. 12, pp. 1309-1321, Dec. 2006.

[12] Ahmed M. Shams, Tarek K. Darwish, and Magdy A. Bayoumi, "Performance Analysis of Low-Power 1-Bit CMOS Full Adder Cells," *IEEE Trans.on Very Large Scale Integration (VLSI) Systems*, vol. 10, no. 1, pp. 20–29, Feb. 2002.

[13] Mark Vesterbacka, "A 14-Transistor CMOS Full Adder With Full Voltage-Swing Nodes," *Proc. IEEE Workshop Signal Processing Systems*, Oct 1999, pp. 713-722.

[14] R. Shalem, E. John and L. K. John "A NOVEL LOW POWER ENERGY RECOVERY FULL ADDER CELL," in *Proc. Great Lake Symp. VLSI*, 1999, pp. 380–383.

[15] Hung Tien Bui, Yuke Wang and Yingtao Jiang, "Design and Analysis of Low-Power 10-Transistor Full Adders Using Novel XOR-XNOR Gates," *IEEE Transactions on Circuits & Systems II: Analog and Digital Signal Processing*, vol. 49, no. 1, pp. 25-30, Jan. 2002.

[16] Chip-Hong Chang, Jiangmin Gu, Mingyan Zhang, "A Review of 0.18μm Full Adder Performances for Tree Structured Arithmetic Circuits," *IEEE Trans. on Very Large Scale Integration (VLSI) Systems*, vol. 13, no. 6, pp. 686-695, June 2005.

[17] J. Wang, S. Fang, W. Feng, New Efficient Designs for XOR and XNOR functions on the Transistor Level. IEEE Journal of Solid State Circuits,Vol. 29, No. 7, 1994, pp. 780-786

[18] R. Zimmermann, W. Fichtner, "Low-power logic styles CMOS versus pass-transistor logic," *IEEE J. Solid-StateCircuits*, Vol. 32, pp. 1079–1090, July 1997

[19] S .R. Chowdhury, A. Banerjee, A. Roy, H. Saha, "A High Speed 8 Transistor Full Adder Design using Novel 3 Transistor XOR Gates". International Journal of Electronics, Circuits and Systems II, 2008, pp. 217-223.

