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Simulative Analysis of Low-Power CMOS Comparators for Wireless Communication

Sharmila Kumari*
M.Tech Student, Department of ECE,
Guru Jambheshwar University of Science & Technology, Hisar, Haryana, India

Kuldeep Singh
Assistant Professor, Department of ECE,
Guru Jambheshwar University of Science & Technology, Hisar, Haryana, India

Abstract- This paper presents two topologies of low power CMOS comparators that are simulated in Mentor Graphics software using TSMC.18µm technology. The circuits studied and simulated in this paper are Dynamic Latched Comparator using Pre-amplifier and Latched Comparator using Preamplifier and Post amplifier. The power dissipation of these comparators operating at frequency 80 MHz with 1.5V power supply are 146.890 µW and 3.6958 nW respectively. Analysis for Power Dissipation, Slew Rate and delay at different values of power supply, input signal frequency and bias current is done.

Keywords: CMOS Comparator, Low Power, High Speed, ADC, Power Dissipation

I. INTRODUCTION

High speed low power comparators are the main building blocks for high speed analog to digital convertors (ADC). Performance of the whole system depends to a large extent on this component. In ADC comparator are used for quantization process and are mainly responsible for the delay produced and power consumed by an ADC. [7] Today, the demand for smaller, lighter and more durable electronic products powered by batteries is increasing. Battery life is becoming a product differentiator in many portable electronic markets. This indirectly translates to low power requirements for high speed applications. Designing high-speed comparators becomes more challenging when working with smaller supply voltage. So this block requires different topologies to be studied so as to make ADC accurate and efficient. Two designs of comparators that we examined are described below with their schematic diagram.

The comparator compares the voltages that appear at the inputs and outputs a binary signal which represents a difference between them.

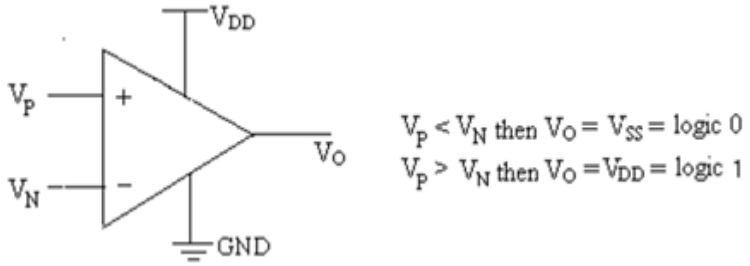


Fig. 1 Comparator operation

This paper is organized into four sections. CMOS comparator architectures are described in section II. Simulation results and graphs are presented in section III. Finally, conclusions are drawn in section IV.

II. CMOS COMPARATOR ARCHITECTURES

A. Dynamic Latched Comparator using Pre-amplifier

In preamplifier latched topology an amplifier is added before a latched comparator which significantly decreases the effects of the offset voltage errors caused by device mismatch.

Preamplifier: The preamplifier uses fully differential circuit structure as shown in figure 2.

The preamplifier should have wide bandwidth and small gain to achieve high speed. The preamplifier decreases the effects of the offset voltage and kickback noise.

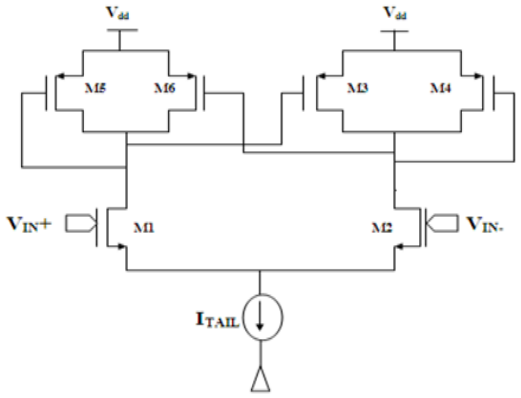


Fig. 2 Preamplifier circuit

Dynamic Latch: In dynamic latch comparators two cross coupled CMOS inverters are used for regeneration. A clock is used to set the comparator in active or standby mode. If the output nodes of preamplifier are directly connected to the regeneration nodes, kickback noise is produced.
Hence, transmission gates are used to control the signal path between preamplifier and latch.
Offset in Dynamic Latch: The offset voltage of the dynamic latch can be expressed as:

$$V_{offset} = \Delta V_{th} + \frac{1}{2}\left(\frac{\Delta W}{W} - \frac{\Delta L}{L}\right)(V_{GS} - V_{th}) + \frac{\Delta Q}{C_D} \qquad (1)$$

Where ΔVth is the standard deviation of the threshold voltage, V_{GS}-Vth is the overdrive voltage, ΔQ is the charge due to switches controlling nodes Vout+ and Vout- and C_D denotes the total capacitance in the output nodes of the dynamic latch. [5]

Preamplifier Dynamic Latch Comparator:
Figure 3 shows the dynamic latch comparator with preamplifier. When the clock signal CLK goes high the comparator enters the reset phase. The comparator is resetting through the shorted transistor M10 between the two cross coupled inverters. When CLK goes low the circuit enters the comparison phase. Transistor M7 is connected to the voltage supply and M13 is connected to ground. The transmission gate is closed and the comparator enters the regenerative phase.

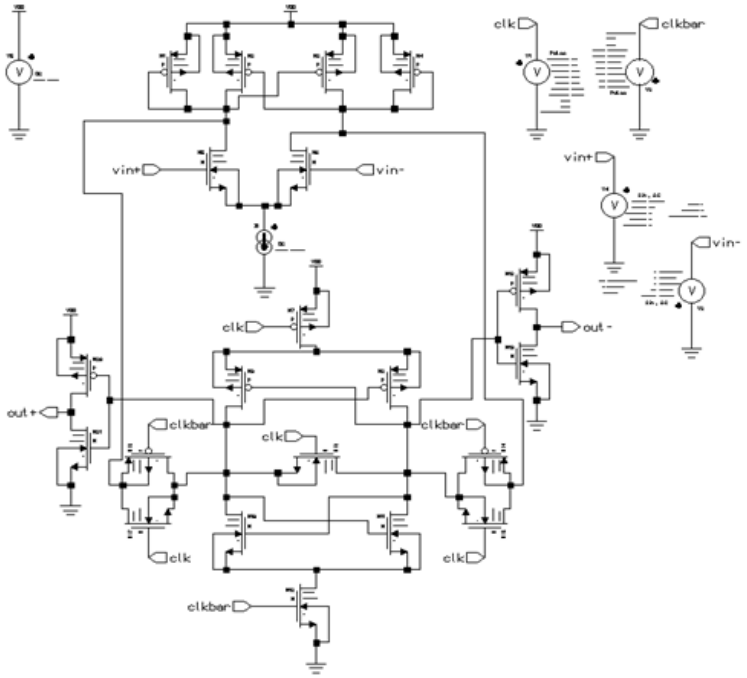


Fig. 3 Schematic of clock driven Preamplifier Dynamic latch comparator (comparator1)

B. Latched Comparator using Preamplifier and Post amplifier

This comparator consists of three stages known as input stage, decision stage and output stage.
Pre-amplification: This circuit is a differential amplifier with active loads. The sizes of M1 and M2 are set by considering the differential amplifier transconductance and the input resistance. The transconductance sets the gain of the stage.

Decision circuit: The decision circuit is the heart of the comparator and should be capable of discriminating mV level signals. The circuit uses positive feedback from the cross-gate connection of M9 and M10 to increase the gain of the decision element. [6]

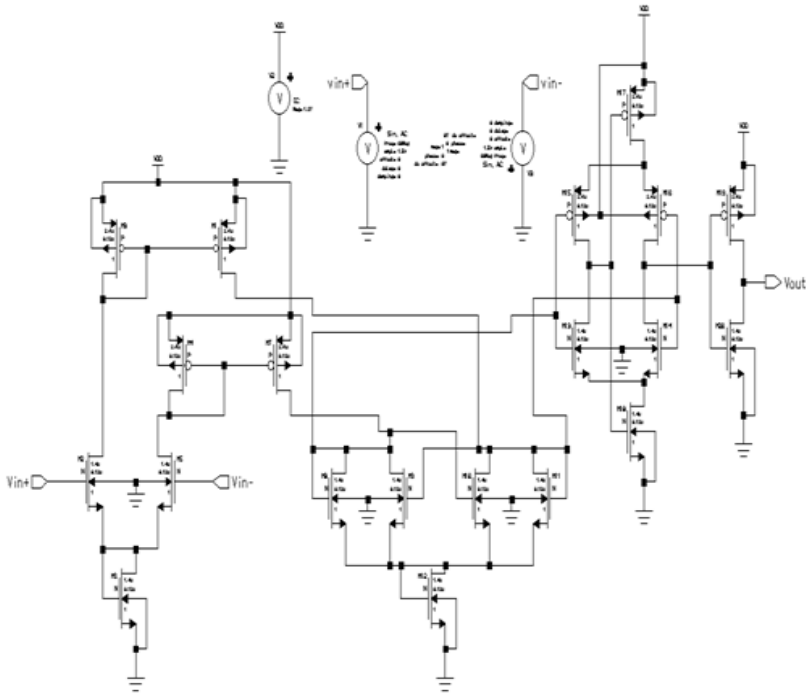


Fig. 4 Schematic of Latched Comparator implemented using Preamplifier and Post amplifier (comparator2)

Output Buffer: The final component in our comparator design is the output buffer or post-amplifier. The main purpose of the output buffer is to convert the output of the decision circuit into a logic signal (i.e., 0 or 1V). The circuit used as an output buffer in our comparator design is a self-biasing differential amplifier. We can see a problem in connecting the decision circuit directly to the output buffer. The MOSFET M12 is added in series with the decision circuit to increase the average voltage out of the decision circuit.

The complete schematic of the comparator is shown in figure 4.

III. SIMULATION RESULTS AND DISCUSSIONS

Simulation of the comparators is done using Mentor Graphics tool in 0.18µm technology. A sinusoidal signal of frequency 80MHz is applied at Vin+ and an 180◦ phase shifted signal of this Vin+ (reverse of sinusoidal signal) is applied at Vin- . Power supply of 1.5v is used for transient analysis of these circuits. Output is high when Vin+ > Vin- and low when Vin+ < Vin- . This can be verified from output waveforms. These architectures have been analyzed in TSMC 180nm in terms of Transient Response, Power Dissipation, Slew Rate and Delay.

A. Analysis of Comparator1

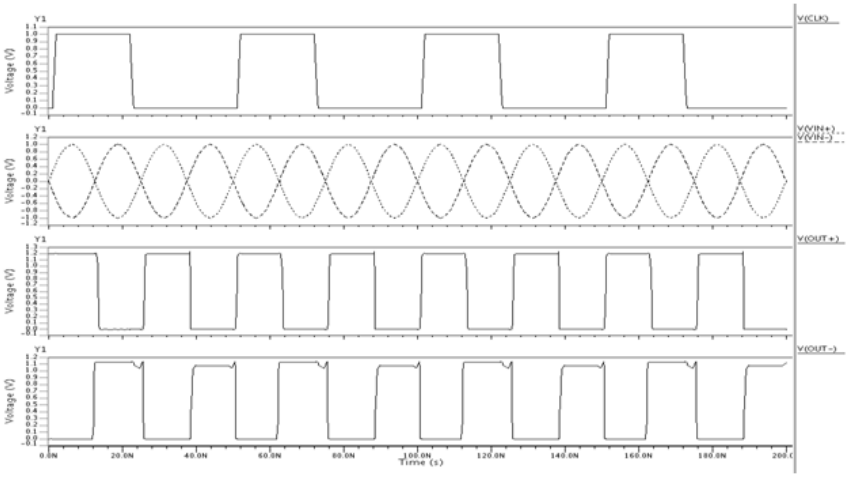
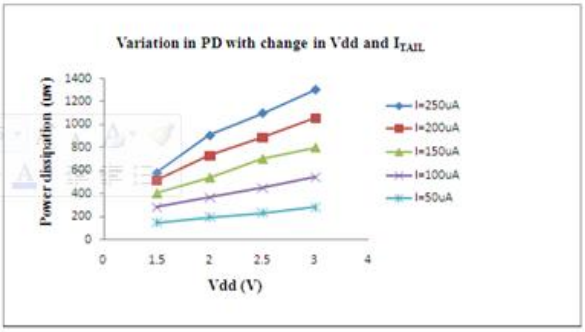


Fig. 5 Transient Response of comparator1

Table 1 shows the variation of Power Dissipation with increase in Vdd and I_{TAIL}. It is clear from this table and graph1 that power dissipation increases continuously with increase of vdd and it also shows the same trend with increment in I_{TAIL}.

Table 1: Power Dissipation at Different Values of Vdd and I_{TAIL}

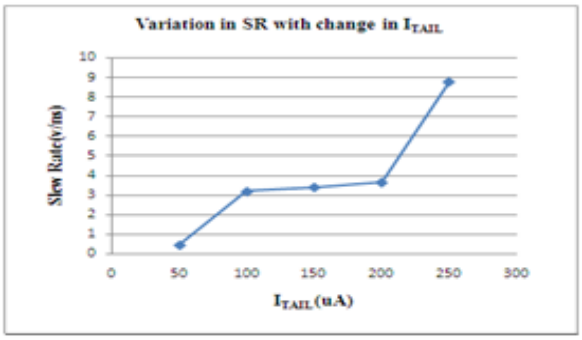
I_{TAIL}(µA)	**Power Dissipation(µw)**			
	V_{dd} =1.5V	V_{dd} =2V	V_{dd} =2.5V	V_{dd} =3V
50	146.890	192.440	230.672	280.670
100	280.420	362.817	447.815	542.984
150	406.980	541.748	701.164	797.760
200	513.004	729.044	890.749	1056.000
250	584.006	905.123	1098.600	1300.400



Graph 1: Shows variation in PD with change in Vdd and I_{TAIL}

Table 2: Slew rate at Different Values of I_{TAIL}

I_{TAIL}(uA)	**Slew Rate(v/ns)**
50	0.4245
100	3.1663
150	3.384
200	3.628
250	8.78



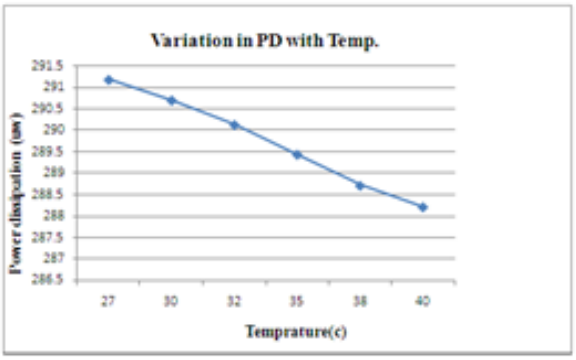
Graph 2: Shows variation in slew rate with change in I_{TAIL}

Power dissipation decreases with increment in temperature as shown in table 3 and graph 3. However variation in PD is very small.

Table 3: PD at Different Values of Temp.

Temp(◦c)	**PD(uw)**
27	291.182
30	290.700
32	290.127

35	289.433
38	288.705
40	288.204



Graph 3: Shows variation in PD with change in Temp.

B. Analysis of Comparator2

The main drawback of Pre-amplifier Dynamic Latch comparator is the high power consumption in range of µw. To overcome this problem, Latched Comparator implemented using Preamplifier and Post amplifier is used that requires much less power in range of nw as compared to the Pre-amplifier Dynamic Latch comparator.

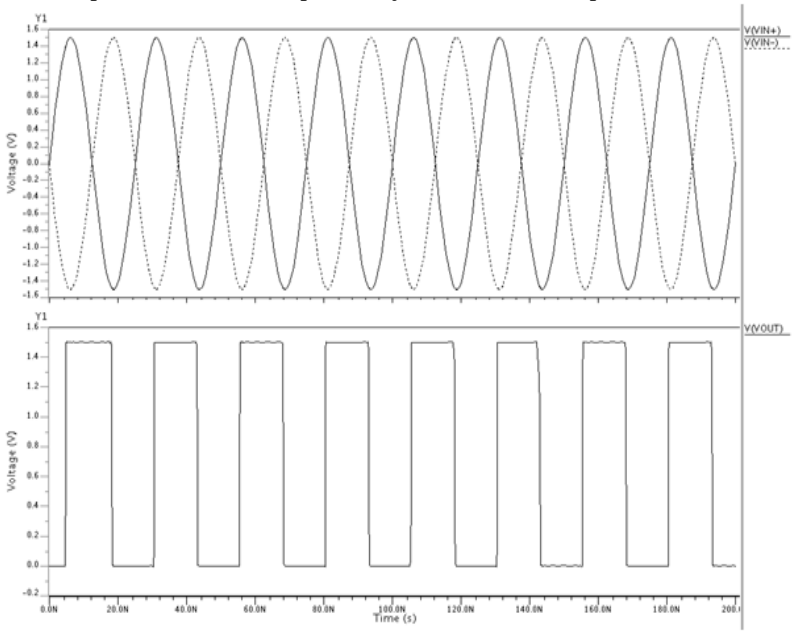
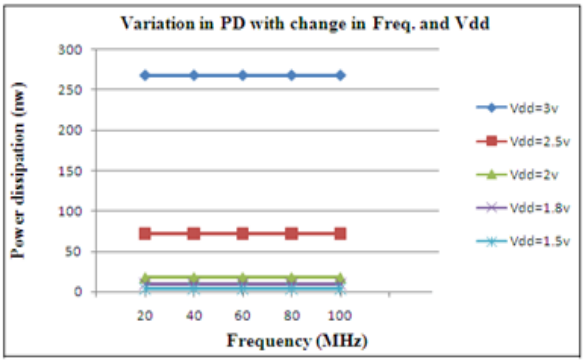


Fig. 6 Transient Response of Comparator2

Similar analysis for Power Dissipation, Slew Rate and delay at different values of power supply, input signal frequency and temperature is done for this comparator also.

Table 4: Power Dissipation at Different Values of Vdd and Freq.

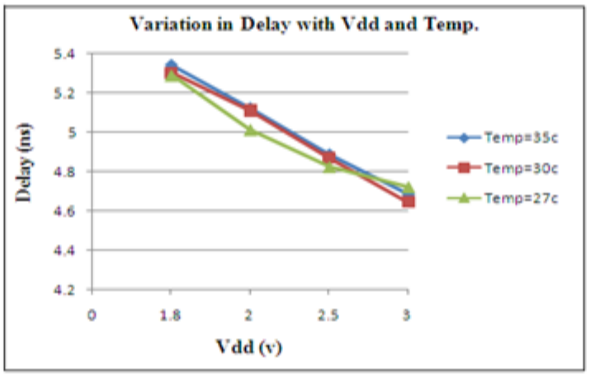
Freq.(MHz)	**Power Dissipation(nw)**				
	Vdd=1.5V	Vdd=1.8V	Vdd=2V	Vdd=2.5V	Vdd=3V
20	3.6958	9.4641	17.2709	71.6420	267.8555
40	3.6958	9.4641	17.2709	71.6420	267.8555
60	3.6958	9.4641	17.2709	71.6420	267.8555
80	3.6958	9.4641	17.2709	71.6420	267.8555
100	3.6958	9.4641	17.2709	71.6420	267.8555



Graph 4: Shows variation in PD with change in Vdd and Freq.

Table 5: Delay at Different Values of Vdd and Temp.

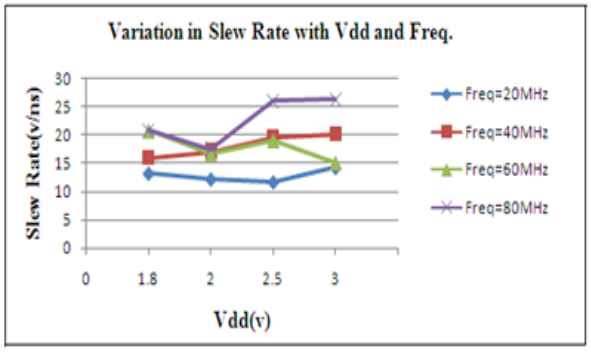
Vdd(V)	**Delay(ns)**		
	Temp=27˚c	Temp=30˚c	Temp=35˚c
1.8	5.2890	5.3008	5.3404
2	5.0126	5.1105	5.1216
2.5	4.8245	4.8677	4.8861
3	4.7213	4.6449	4.6819



Graph 5: Shows variation in Delay with change in Vdd and Temp.

Table 6: Slew Rate at Different Values of Vdd and Freq.

Vdd(V)	Slew Rate(v/ns)			
	Freq=20MHz	Freq=40MHz	Freq=60MHz	Freq=80MHz
1.8	13.173	15.978	20.842	20.789
2	12.737	17.117	16.798	17.534
2.5	11.604	19.611	19.090	26.222
3	14.220	20.093	15.106	26.355



Graph 6: Shows variation in SR with change in Vdd and Freq.

IV. CONCLUSION

This paper explains about the Comparator and its design in two different topologies. Detailed analysis of these Comparators has been carried out in TSMC.18μm technology using Mentor Graphics tool and power analysis is made by analyzing pre-layout simulation results. Power Dissipation is the main parameter to be considered in any design. Power dissipation is low in case of Latched Comparator implemented using Preamplifier and Post amplifier at low values of power supply and transient response is also good. Its power dissipation is 3.6958 nW whereas that of Dynamic Latched Comparator using Pre-amplifier is 146.890 μW at 1.5V power supply.

REFERENCES

[1] David A. Johns and Ken Martin "Analog Integrated Circuit Design" Analog Integrated Circuit Design".

[2] Paul R. Gray , Paul J. Hurst , Stephen H. Lewis , Robert G. Meyer " Analysis And Design Of Analog Integrated Circuits " Fifth Edition.

[3] S. A. Mahmoud and I. A. Awad, "New CMOS balanced output transconductor and application to GM-C biquad filter," in *IEEE INTERNATIONAL SYMPOSIUM ON CIRCUITS AND SYSTEMS*, pp. I–385,2003.

[4] S. Sheikhaei, S. Mirabbasi, and A. Ivanov, "A 0.35 mu;m CMOS comparator circuit for high-speed ADC applications," in *IEEE International Symposium on Circuits and Systems*, pp. 6134–6137,Vol. 6,2005.

[5] T. Sundstrom, B. Murmann, and C. Svensson, "Power dissipation bounds for high-speed Nyquist analog-to-digital converters," *Circuits and Systems I: Regular Papers, IEEE Transactions on*, vol. 56, no. 3, pp. 509–518, 2009.

[6] C. J. Solis and G. O. Ducoudray, "High resolution low power 0.6 #x00B5;m CMOS 40MHz dynamic latch comparator," in *53rd IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)*, pp. 1045–1048,2010.

[7] S. Shubhanand, D. H. Shukla, and A. G. Rao, "Design and Simulation of a High Speed CMOS Comparator," *International Journal of Electronics and Communication Engineering, ISSN*, pp. 0974–2166,2013

[8] K. Kandpal, S. Varshney, and M. Goswami, "A High Speed-Low Power Comparator with Composite Cascode Preamplification for Oversampled ADCs," *Journal of Automation and Control Engineering in*, vol. 1, no. 3, 2013.

[9] Sandeep K. Arya and Neelkamal, "A Comparative Study of Dynamic Latch Comparator", Seek Digital Library, 2013.

[10] R. Mongre and R. C. Gurjar, "Design of Low Power & High Speed Comparator with 0.18 μm Technology for ADC Application" *Int. Journal of Engineering Research and Applications, ISSN*,pp.146-153, vol. 4,2014.

[11] D. Parashar, "Design of a CMOS Comparator using 0.18 μm Technology." *International Journal on Recent and Innovation Trends in Computing and Communication, ISSN*, pp. 977-982, Vol. 2, 2014.

