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Optimal Design of R2R DAC using Reversible Logic

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Abstract— Adoption of reversible logic circuits to achieve lower power and robust design is widely proved. The assumption of reversible logic to analog mixed circuit design is still navie. In this paper, a generic R2R Digital to Analog Converter (DAC) based on reversible logic design is proposed. Reversible logic circuitry for the DAC has been realized using Quasi-Floating Gate (QFG) technique and this helps in further reduction of power and improves the robustness of the converter. Results presented in this paper prove that by adopting of reversible logic concepts, average power of R2R DAC design is reduced by 51% when compared with conventional logic R2R DAC design concepts and substantial improvement has been observed for higher resolution DAC's.

Keywords— Conventional logic, Reversible logic, Quasi floating gate, CMOS Inverter, INL, DNL.

I. INTRODUCTION

In the past decade, attempts to scale down the CMOS based designs have put forth challenges to the industry people and researcher's. Circuit robustness and power consumptions will play an important role in major challenges that exist. In CMOS circuits, power dissipation and energy saving has been primarily considered due to clock generation mechanisms [1], power delivery systems [2] and bit erasure within the interconnected conventional CMOS circuits or devices [3] [4].

To reduce the power dissipation in CMOS circuits, researchers have proposed reversible logic circuit designs. Power reduction in reversible CMOS logic circuits have been mainly achieved by eliminating the bit erasures. Reversible logic has derived based on the quantum mechanics. A reversible logic is said to be bijective [4] since it has have equal number of inputs and outputs [5] which aids power reduction in the circuits. Thus the various researchers have proposed different designs on reversible logic circuits using Feynman [2], Toffoli [4], Fredkin [6], Peres [7] and some elementary reversible logic gates [8] etc., are most commonly used. In the recent time, research to realize digital system and synthesis of reversible logic circuits has been aggressively undertaken [9]. Design of digital circuits like adders [10], comparators [11], multiplexer [12], decoders and de-multiplexer [13], ALU [14] and many more have been proposed using reversible logic and yields in low power design. Based on the literature survey, it is evident that consider amount of power reduction will achieve in digital circuits using reversible logic.

The outline of this paper is as follows. Motivation and methodology has discussed in section 2. Review of the work carried out by various researchers using reversible logic has presented in section 3. A brief discussion on conventional R2R DAC design is discussed in section 4. The proposed R2R DAC design has presented in section 5. The comparison of results by considering 4-bit, 6-bit and 8-bit implementations of the conventional R2R DAC and proposed reversible R2R DAC has presented in section 6. The conclusion and scope of future work have presented in last section of this paper.

II. MOTIVATION AND METHODOLOGY

Digital to Analog Converter (DAC) and Analog to Digital Converter (ADC) are very essential elements of any mixed signal circuits. Limited work has carried out so far in adopting analog mixed signal designs using reversible logic circuits. This is a major motivating factor. This paper present's the design of CMOS based R2R DAC using reversible logic circuits thus reversible logic gates have designed using Quasi-Floating Gates (QFG) [15]. The QFG based reversible units of the DAC enables in effectively handling changes in the low voltages at the inputs [16], which have commonly observed in the DAC's. QFG based designs also enables in handling multiple inputs and aids in reducing the voltage drops or leakage at the gates of the CMOS transistors [18]. R2R DAC based on reversible logic has been designed using 45nm CMOS technological parameter and outputs are analyzed using spice simulator.

III. RELATED WORK

In this section, a brief work on the reversible logic based implementations currently in place has discussed. The authors have considered the design of shift registers using reversible logic gates such as HNFG and Fredkin reversible logic gates [2]. Novel online testable gate and its design using Fredkin and Toffoli reversible logic gates and the applicability of online testable gate as a reversible full adder design has been discussed [10]. A reversible binary comparator has proposed and the circuit is aids in low power dissipation [11]. Multiplexer design for optical networks is designed by adopting the Mach-Zehnder interferometer reversible switches [12]. Low power reversible optical switches and its adoption in multiplexer and de-multiplexer designs have been discussed [13]. Based on the hybrid SET-CMOS technology the design of a reversible arithmetic and logic unit has presented [14]. The optical switches have designed by

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using a combination of micro ring resonator switches and reversible logic gates. The multiplexers and de-multiplexers were designed using CMOS technology and are reconfigurable [19].

Based on the literature survey presented in this paper, shows that the limited work have been carried out in adopting reversible logic concepts for analog mixed signal circuit designs.

IV. CONVENTIONAL R2R DAC

DAC is a significant element of an analog-mixed signal circuits. It facilitate an interfacing the digital world that recognizes and appreciate the signal in analog domain. A DAC is a circuit that converts digital signal into an equivalent analog signal. A functional diagram of DAC is as shown in figure 1.

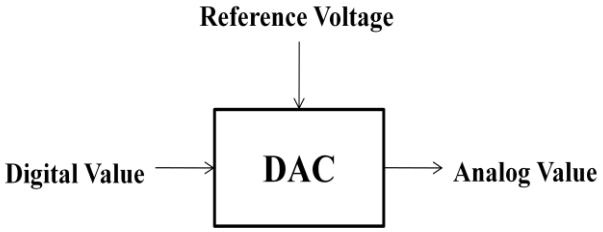

Fig. 1 Functional block diagram of Digital to Analog Converter (DAC).

Multiple architectures have been proposed to realize DAC namely, Binary weighted resistor DAC, R2R ladder DAC, Multiplier DAC and Non-Multiplier DAC etc. The R2R ladder DAC and binary weighted DAC are most commonly used.

A Conventional logic based N bit R2R ladder DAC is as shown in figure 2 and reference voltage (VRef) has supplied at the input. Design consists of driver/ latch circuits in which driver will drive the voltage and latch will hold the voltage. The reference voltage has propagates from one node to another node based on the digital inputs.

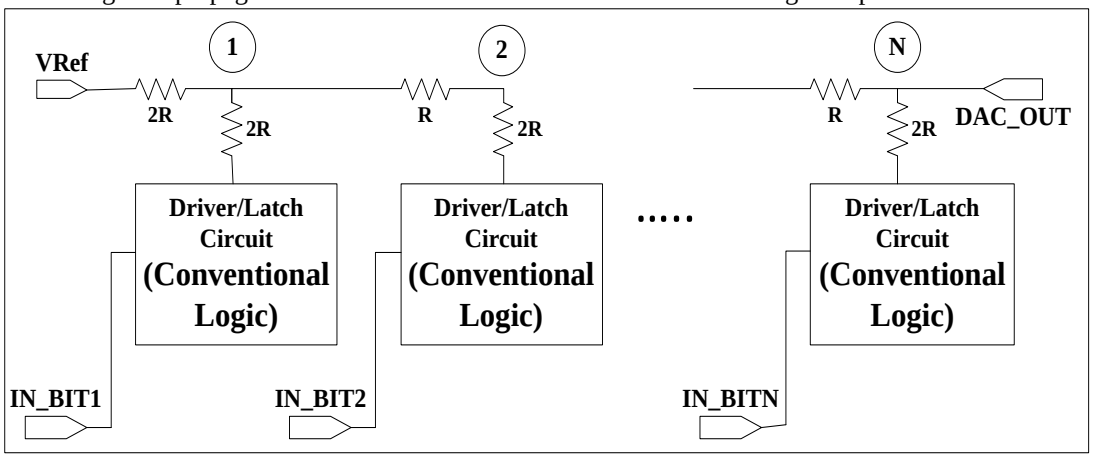

Fig. 2 N-bit Conventional R2R DAC

The input digital bits has represented by IN_BITX, where $X = \{1,2,3 \ldots N\}$. The LSB bit is (i.e. $X = 1$) is represented as IN_BIT1 and the MSB bit (i.e. $X = N$) is represented as IN_BITN. The matching of the resistors in the R2R ladder is critical. Considering the ideal case wherein all the resistors of the R2R ladder is perfectly matched and the switching logic (is achieved through the Driver/Latch) is ideal, then the output voltage of the N bit R2R DAC is defined by

$$DAC\_OUT_{IDEAL} = VRef \times \left(\left(\frac{IN\_BIT1}{2^1}\right) + \cdots + \left(\frac{IN\_BITN}{2^N}\right)\right) \quad \ldots\ldots\ldots\ldots (1)$$

In equation (1), $\left(\frac{IN\_BITN}{2^N}\right)$ represents N^{th} node on basis of the digital input IN_BITN. The above ideal equation can be simplified and represented as

$$DAC\_OUT_{IDEAL} = VRef \times \sum_{X=1}^{N} \frac{IN\_BITX}{2^X} \quad \ldots\ldots\ldots\ldots (2)$$

Equation (2) shows the performance of R2R DAC is dependent on the core of R2R ladder structure. Achieving perfect matching of resistors in CMOS technology for R2R ladder design is difficult. Resistor mismatches occur due to process technology variations. The effects of resistor mismatches are clearly discussed [17]. Similarly, process variation of the CMOS transistor based driver/latch circuit is also inducing errors.

Let δ_V^{CONV} represents the variation of the output voltage for the conventional R2R DAC due to resistor mismatch and process variation of the CMOS transistors.

The output voltage of the conventional R2R DAC by considering voltage variation due to resistor mismatch is given as

$$DAC\_OUT_{CONV} = \delta_V^{CONV} + \left(VRef \times \sum_{X=1}^{N} \frac{IN\_BITX}{2^X}\right) \quad \ldots\ldots\ldots (3)$$

The errors induced due to the process variations effect into the performance of the conventional R2R DAC and it has been analyzed using Integral Nonlinearity (INL) and Differential Nonlinearity (DNL) parameters.

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V. PROPOSED R2R DAC BASED ON REVERSIBLE LOGIC

The proposed N bit R2R DAC using reversible logic circuit is as shown in figure 3. The core of R2R ladder structure is similar to the conventional R2R DAC as shown in figure 2. The Driver/Latch circuitry is used to steer the voltage through the various nodes of the ladder has been developed using reversible logic to minimize the power consumption in the circuit and these circuits primarily consists of inverter and buffer. The novelty of the proposed R2R DAC is that the reversible driver/latch circuitry is realized using QFG technique. The voltage is steering from one node to another based on the digital input and it is essential to have well defined DC operating points at the nodes 1, 2, 3…..N as shown in figure 3.

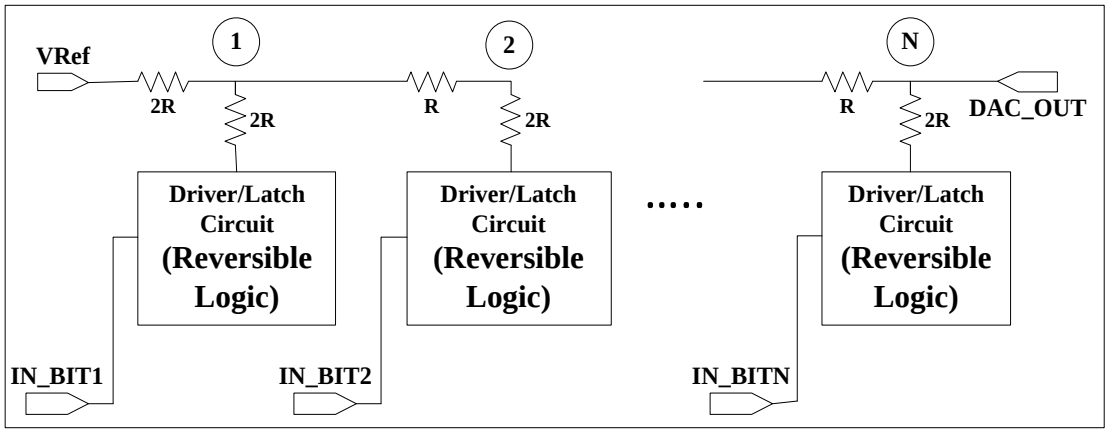

Fig. 3 N-bit Reversible R2R DAC

The QFG technique enables in achieving accurate DC operating points at the nodes to improve robustness [18]. The QFG transistors support capacitive based input circuits, which lowers the cut-off frequencies in the design of reversible inverter. In this paper, reversible inverter implementation circuit based on the QFG technique is as shown in figure 4.

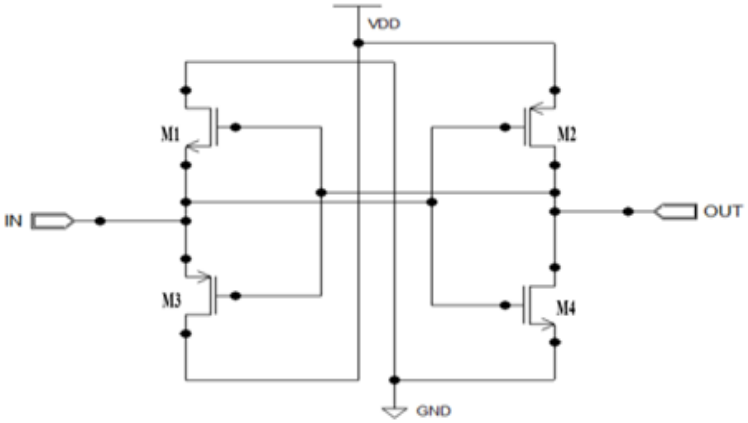

Fig. 4 Reversible CMOS Inverter using QFG Technique

The reversible inverter design mainly consists of four QFG transistors namely M1, M2, M3 and M4. Bias voltages for M1, M2, M3 and M4 transistors has maintained accurately. The output voltage of the proposed reversible R2R DAC can be defined as

$$\left.\begin{aligned} DAC\_OUT_{REV} &= \delta_V^{REV} + \left(VRef \times \sum_{ib=1}^{N} \frac{IN_{BI\,Tib}}{2^{ib}}\right) \\ &= \delta_V^{REV} + DAC\_OUT_{IDEAL} \end{aligned}\right\} \quad \text{..... (4)}$$

where δ_V^{REV} Represent's the voltage variations due to resistor mismatch and process variation of transistor in the reversible R2R DAC when compared to the ideal output voltage DAC_OUT_{IDEAL} and the performance of the proposed reversible R2R DAC is based on INL and DNL parameters.

VI. CMOS IMPLEMENTATION AND RESULT DISCUSSION

The Reversible R2R DAC and Conventional R2R DAC have designed using 45nm CMOS technology process and operating with a supply voltage $VDD = 1.8\,V$. The 1:2 ratio resistor values have been maintain in the design to implement R2R ladder core. The performance of the conventional R2R DAC is compared with reversible R2R DAC by considering 4-bit, 6-bit and 8-bit design implementations. Transient analysis has been carried out and average power consume is recorded. The performance of the both conventional and reversible R2R DAC design have compared based on INL and DNL parameters.

The DNL has computed by measuring the difference between the observed step width and ideal step width. Ideal step width has denoted as LSB^1. The computation of LSB^1 for N-bit R2R DAC has defined as

$$LSB^1 = \frac{Max\,(DAC\_OUT_{IDEAL})}{2^N} \quad \text{..... (5)}$$

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where $Max(DAC\_OUT_{IDEAL})$ is the maximum output voltage of the ideal DAC.

The DNL is computed at every transition of the digital input and it is computed using

$$DNL_X = \frac{\left((DAC\_OUT^{IN\_BIT\,(X+1)} - DAC\_OUT^{IN\_BITX}) - LSB^1\right)}{(LSB^1)} \quad \text{..... (6)}$$

where $DAC\_OUT^{IN\_BITX}$ represents the R2R DAC output considering the X^{th} digital input has represented in decimal.

The INL for the X^{th} digital input is computed using

$$INL_X = \frac{\left(\left(DAC\_OUT^{IN\_BITX} - DAC\_OUT_{IDEAL}^{IN\_BITX}\right)\right)}{(LSB^1)} \quad \text{..... (7)}$$

where $DAC\_OUT_{IDEAL}^{IN\_BITX}$ represents the ideal R2R DAC outputconsidering X^{th} digital input hasr represented in decimal.

A. 4-Bit R2R DAC Implementation

A 4-bit R2R DAC implementation based on conventional logic and reversible logic has designed. Transient response obtained is as shown in figure 5. The average power consumed by considering the conventional R2R DAC and reversible R2R DAC has found to be 122µW and 63.27 µW respectively. The results obtained shows the substantial power reduction with R2R DAC design using reversible logic by 51.8% when compared to conventional logic based R2R DAC. The average power consumed has recorded.

The transient response of a 4-bit ideal DAC has been computed and average error for all the 2^4digital inputs with the designed conventional and reversible DAC's has been computed and is found to be 6.37% and 6.29% respectively with respect to the ideal output.

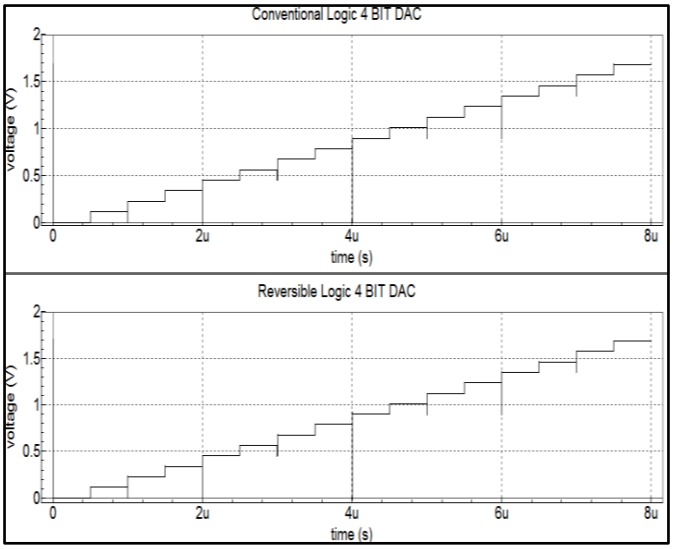

Fig. 5 Transient response of 4-bit R2R DAC considering conventional logic and reversible logic.

The INL and DNL parameters have been obtained and plotted is as shown in figure 6 respectively.

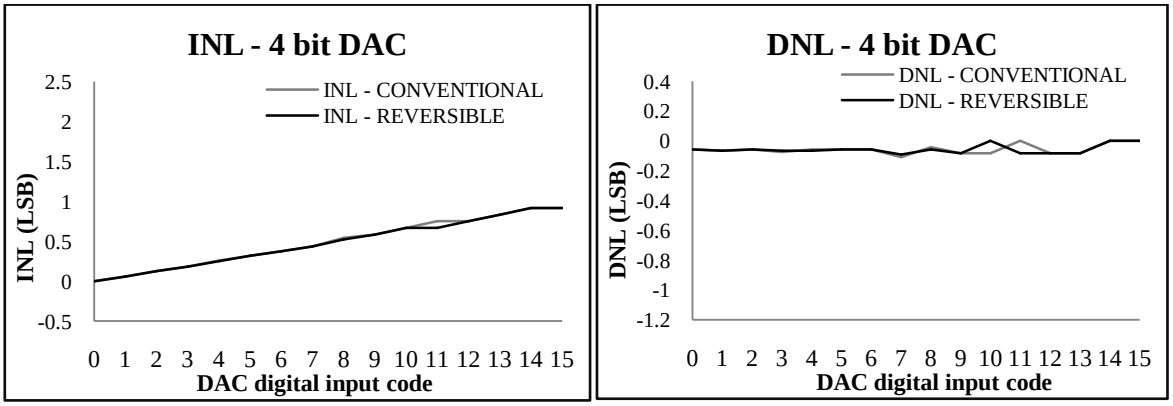

Fig. 6 INL and DNL analysis of 4-bit R2R DAC considering conventional and reversible logic based implementations

B. 6-Bit R2R DAC Implementation

6-bit (2^6 Digital inputs) R2R DAC has been designed based on the conventional circuit design and reversible circuit. The digital inputs i.e. 6-bit has varied linearly and respective output voltage is observed. The output voltage response of DAC_OUT_{CONV} and DAC_OUT_{REV} is as shown in figure 7. An average error of 1.54% has observed between DAC_OUT_{CONV} and DAC_OUT_{IDEAL} and DAC_OUT_{REV} and DAC_OUT_{IDEAL} was found to be 1.56%. The average power consumed by considering the conventional R2R DAC and reversible R2R DAC has found to be 172.81µW and 89.05 µW respectively and achieve 51.5% of power reduction in reversible logic circuit design.

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The INL and DNL parameter has computed with corresponding digital input codes and plotted, as shown in figure 8 respectively.

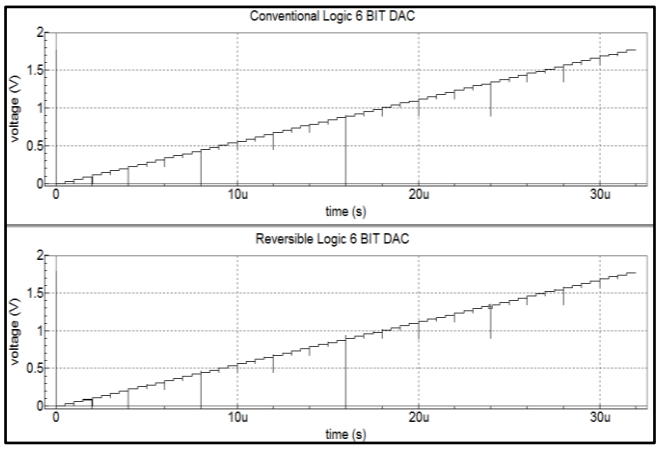

Fig. 7 Transient response of 6-bit R2R DAC considering conventional logic and reversible logic

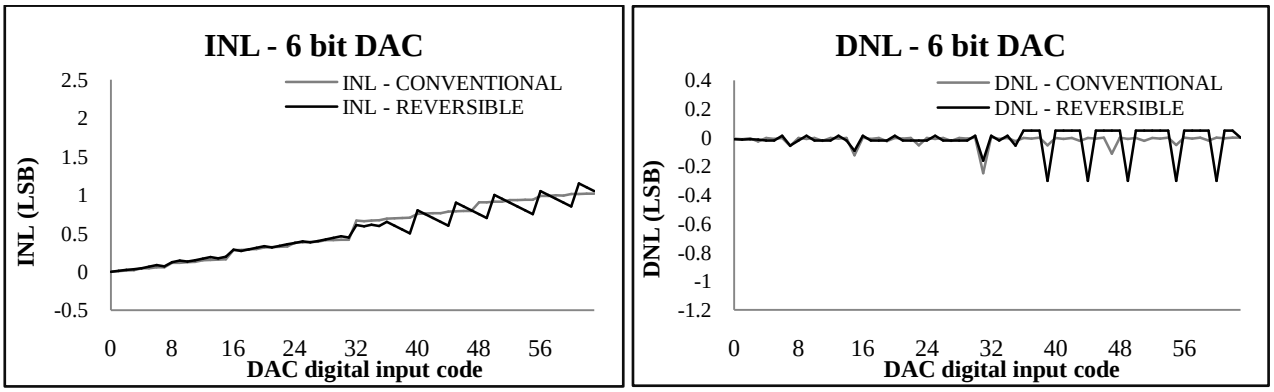

Fig. 8 INL and DNL analysis of 6-bit R2R DAC considering conventional and reversible logic based implementations

C. 8-Bit R2R DAC Implementation

Considering $N = 8$ i.e., 8-bit (2^8 Digital inputs) R2R DAC using conventional circuit and proposed reversible circuit have designed. Uniform resistance values has considered for both the R2R DAC designs. The digital input codes are varied from 0 to 255 in uniform intervals. The results has obtained is as shown in figure 9.

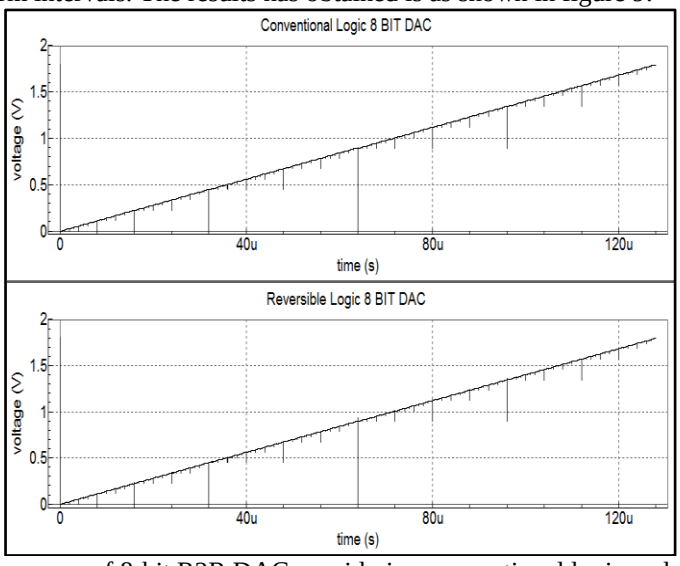

Fig. 9 Transient response of 8-bit R2R DAC considering conventional logic and reversible logic

On comparing with the ideal output voltage, a low average error of 0.47% and 0.37% was observed by considering DAC_OUT_{CONV} and DAC_OUT_{REV}. The average power consumed by the conventional logic and proposed reversible logic R2R DAC is 226.1μW and 116μW respectively. From the results, it can be stated that the substantial amount of power reduction in R2R DAC design using reversible logic is about 51.3% with respect to conventional logic. INL and DNL result's of 8-bit is as shown in figure 10. It has observed that the proposed reversible R2R DAC exhibits better performance when compared to the conventional R2R DAC.

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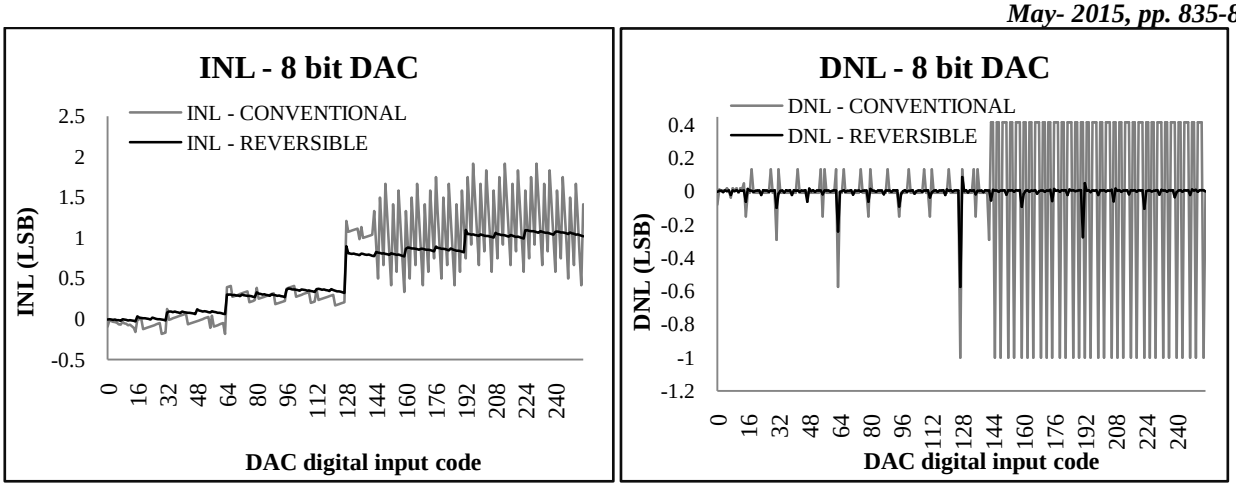

Fig. 10 INL and DNL analysis of 8-bit R2R DAC considering conventional and reversible logic based implementations

Based on the results presented in this paper, it clearly states that an average power reduction of 51% is observed in reversible logic based R2R DAC. We have recorded in table 1 and table 2 presents the performance parameters of R2R DAC in conventional logic design and reversible logic design respectively.

TABLE I.
ANALYSIS OF R2R DAC IN CONVENTIONAL LOGIC

No. of Bits	Average Power dissipation	Average Delay	Average		Average Error
			INL	*DNL*	
4-Bit	122.00µW	1.75µs	0.4817	-0.0572	6.3655 %
6-Bit	172.81µW	7.75µs	0.5306	-0.0158	1.5392 %
8-Bit	226.12µW	31.75µs	0.6257	-0.0058	0.4700 %

TABLE II.
ANALYSIS OF R2R DAC IN REVERSIBLE LOGIC

No. of Bits	Average Power dissipation	Average Delay	Average		Average Error
			INL	*DNL*	
4-Bit	63.27µW	1.75µs	0.4749	-0.0573	6.2872 %
6-Bit	89.04µW	7.75µs	0.5142	-0.0164	1.5550 %
8-Bit	116.03µW	31.75µs	0.5585	-0.0039	0.3757 %

VII. CONCLUSION

In this paper, R2R DAC incorporating novel reversible logic circuits has been proposed. The reversible logic inverter has realized using QFG techniques to overcome the voltage drops at each node. The performance of the proposed reversible R2R DAC has compared with the conventional R2R DAC. INL and DNL calculations have carried out so far and it proves that reversible logic based R2R DAC design gives low average error for higher resolution of DAC. Implementations of 4-bit, 6-bit and 8-bit R2R DAC resolution have been presented. The proposed reversible logic R2R DAC circuit design substantiate that there is a considerable amount of power consumption and the design is robust.

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