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Unified Systolic Architecture for High – Throughput VLSI Implementation of Prime – Factor Discrete Fourier, Discrete Hartley, and Discrete Cosine Transforms

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Abstract— In this paper, we have suggested unified systolic mesh architecture for the implementation of prime – factor discrete Fourier transform (DFT), discrete Hartley transform (DHT), and discrete cosine transform (DCT). Also, we have suggested a new decomposition scheme and a highly compact bilayer systolic architecture for high throughput computation of prime – factor DHT. It is shown further, that the proposed DHT structure can be used for efficient computation of prime – factor DFT, and DCT, as well. The transposition of the intermediate matrix is avoided in the unified systolic architecture by orthogonal processing of data during the pair of matrix multiplications. In the proposed bilayer DHT structure, the transposition of intermediate output is avoided by orthogonal alignment of the arrays of output layer with respect to the arrays of input layer. Both the structures, therefore, provide saving in hardware, as well as, time, which are required for transposition in the existing architectures. The area and time complexities of the proposed bilayer DHT structure is nearly (1/4) and (1/2) times that of the unified architecture, respectively, while both the structures require nearly the same amount of hardware.

Keywords— DCT, DHT, DFT, KLT

I. INTRODUCTION

Discrete orthogonal transforms have evolved quite rapidly over the last three decades for their speech and image processing applications. The discrete Fourier transform (DFT) is the most popular one, and the oldest among these orthogonal transforms. Following the first Fourier transform (FFT) of Cooley and Tukey [1], several algorithms have, therefore, been developed for the fast computation of the DFT [2-4]. The discrete Hartley transform [DHT] [5] has become popular, in the recent years, as a real - valued alternative to the DFT for several one and two dimensional signal processing applications for avoiding complex arithmetic operations. Hence, many fast algorithms have been reported in the literature [6 - 11] for efficient computation of the DHT. Amongst all the discrete orthogonal transforms, the discrete cosine transform (DCT) [12] is the most efficient for compression of speech and image data [13]. Performance of the DCT is shown to be comparable to the optimal Karhunen Loeve transform (KLT) [12-14] for the purpose of data compression, feature extraction and filtering applications. Therefore, several fast algorithm have been developed for the efficient implementation of the DCT, in general purpose computers [15, 22].

Along with the growth of integrated circuit technology, high – performance application – specific dedicated processors are evolving rapidly for digital signal processing applications. The VLSI systems yield high throughput of results by maximising the processing concurrency, so that they provide less expensive and, more suitable alternative to general – purpose computers, for real – time and on- line applications. Systolic architectures are emerging as the most popular and dominant class of VLSI structures due to the simplicity of their processing elements (PE), modularity of their structure, regular and nearest – neighbour interconnections between the PEs, high level of pipelineability, small chip – area, and low power dissipation [23]. In systolic architectures, the desired data are pumped rhythmically in a regular interval across the PEs for yielding high throughput by fully pipelined processing. Keeping these facts in view, some systolic architectures have been suggested for the VLSI implementation of the DFT, DCT and DHT [22, 24 -32].

Prime – factor decomposition of the DFT can be done directly, as$\mathrm{e}^{-j\,(l+m)} = \mathrm{e}^{-j\,l}\mathrm{e}^{-jm}$. But such a direct decomposition is not possible in case of the DHT and DCT, because $\mathrm{cas}(l+m) \neq \mathrm{cas}(l)cas(m)$and $\cos(l+m) \neq \cos(l)\cos(m)$, respectively. Yang [11] has suggested an index mapping scheme for the Prime – factor decomposition of the DHT, which requires complicated manipulation of the input. Chakrabarti and Ja' Ja' [28] have presented a bit serial solution for small DHT modules, and they have suggested a systolic architecture for prime – factor DHT [29] which is computed via four temporary outputs. Chang and Lee [30] have proposed two different CORDIC (Co-ordinate Rotation Digital Computer) systolic arrays for computation of the DHT of any given transform length. The structure of Chang and Lee has poor throughput rate, though they are hardware efficient due to their CORDIC processing, as they do not use any prime – factor scheme. Meher *et al*, [31] have proposed a systolic structure for computing the prime – factor DHT of transform length *N*-4*M*, where *M* is prime to 4. Yang and Narasimha [17] have suggested a prime-factor DCT algorithm which does not involve complex multiplications, unlike those of [27] and [32]. Lee [18] has proposed another index mapping scheme for prime-factor DCT which is more efficient compared with that of Yang and Narasimha [17]. But, the input index mapping of Lee [18] would not be feasible in variable – size applications, and it requires extra memory as it constructs and combines two index tables. Lee and Huang [22] have suggested a scheme for prime – factor decomposition of the DCT which involves simpler and more efficient index mapping compared with those of [17,18], and is devoid of complex arithmetic operations , as well. Also, they have proposed two systolic architectures comprising of two matrix multiplication units and a transposition unit.

In this paper, we have suggested a unified systolic mesh architecture for the implementation of prime – factor DCT, DFT and the DHT. To obtain the computing algorithm, we have proposed a new prime – factor decomposition scheme for the DHT, and we have used the decomposition scheme of Lee and Huang [22] for the DCT. Apart from that we have proposed a systolic algorithm for massively parallel implementation and a highly compact bilayer 2 – D architecture for high – throughput computation of the prime – factor DHT. It is shown that the proposed DHT structure can be used for efficient computation of the prime – factor DFT and DCT, as well.

In the following Section, we have presented the algorithm and the unified systolic architecture for the DFT, DHT and the DCT. Section III deals with the proposed bilayer DHT architecture and its algorithm. Concluding remarks are given in Section IV.

II. COMPUTING ALGORITHM AND THE UNIFIED SYSTOLIC ARCHITECTURE FOR THE DFT, DHT AND THE DCT

Due to the exponential nature of the Fourier kernel, the DFT is directly decomposable when the transform length is comprised of two relatively prime factors. In view of systolic implementation of the prime – factor DFT, we have outlined its decomposition scheme in Subsection A. In Subsection B, we have proposed a new decomposition scheme for prime – factor DHT. For implementing the prime – factor DCT, we have reviewed the decomposition scheme of Lee and Huang [22] in the Subsection C. The proposed unified structure is given in Subsection D.

A. Prime – factor Decomposition of the DFT

The DFT of sequence { x (n), n = 0, 1, 2, ………, N−1} may be defined as

$$F(k) = \sum_{n=0}^{N-1} x(n)\mathrm{e}^{-j2\pi kn/N} \text{ for } k = 0, 1, \dots\dots, N-1 \tag{1}$$

For the transform length $N = N_1$ x N_2, where N_1 and N_2 are relatively prime, the indices k and n in (1) may be mapped into pairs of indices (k_1, k_2) and (n_1, n_2), respectively, according to the following equations [33]:

$k = (k_1N_2s_1 + k_2N_1s_2)$ mod N (2a)

$n = (n_1N_2 + n_2N_1)$ mod N (2b)

for k_1 and n_1 = 0, 1, …….., N_1−1 and k_2 and n_2 = 0, 1, ……..N_2 – 1

where

N_2s_1 = 1 mod N_1 and N_1s_2 = 1 mod N_2 (3)

Using (2) and (3), (1) may be expressed in 2-D form as

$$F(k_1,k_2) = \sum_{n_1=0}^{N_1-1}\sum_{n_2=0}^{N_2-1} x(n_1,n_2)\, e^{-j2\pi k_1n_1/N_1} e^{-j2\pi k_2n_2/N_2} \tag{4}$$

B. Prime – factor Decomposition of the DHT

The DHT of a real – valued sequence { x (n), n = 0, 1, 2, ………, N−1} may be defined as

$$H(\mathrm{k}) = \sum_{n=0}^{N-1} x(n)(\cos\frac{2\pi kn}{N} + \sin\frac{2\pi kn}{N}) \qquad \text{for } k = 0,1,\dots\dots N-1 \tag{5}$$

Using the mapping of (2) and (3) for $N = N_1$ x N_2, (5) may be expressed as

$$H(k_1,k_2) = \sum_{n_1=0}^{N_1-1}\sum_{n_2=0}^{N_2-1} x(n_1,n_2)\left[\cos 2\pi\left(\frac{k_1n_1}{N_1}+\frac{k_2n_2}{N_2}\right) + \sin 2\pi\left(\frac{k_1n_1}{N_1}+\frac{k_2n_2}{N_2}\right)\right] \tag{6}$$

Equation (6) may be otherwise be written as

$$H(k_{1,}k_2) = \sum_{n_2=0}^{N_2-1}\left[\sum_{n_1=0}^{N_1-1} x(n_1,n_2)\cos\frac{2\pi k_1n_1}{N_1} + \sum_{n_1=0}^{N_1-1} x(n_1,N_2-n_2)\sin\frac{2\pi k_1n_1}{N_1}\right]\operatorname{cas}\frac{2\pi k_2n_2}{N_2} \tag{7}$$

assuming $x(n_1,N_2) = x(n_1,0)$

Besides, it can be found that,

$$\sum_{n_1=0}^{N_{1-}1} x\,(n_1,n_2)\cos\frac{2\pi k_1n_1}{N_1} = \frac{1}{2}\sum_{n_1=0}^{N_1-1}[\,x(n_1,n_2) + x\,(N_1-n_1,n_2)]\operatorname{cas}\frac{2\pi k_1n_1}{N_1} \tag{8}$$

and

$$\sum_{n_1=0}^{N_{1-}1} x\,(n_1,N_2-n_2)\sin\frac{2\pi k_1n_1}{N_1} = \frac{1}{2}\sum_{n_1=0}^{N_1-1}[\,x\,(n_1,N_2-n_2) - x(N_1-n_1,N_2-n_2)]\operatorname{cas}\frac{2\pi k_1n_1}{N_1} \tag{9}$$

Using (8) and (9) on (7), one may have

$$H(k_1k_2) = \sum_{n_2=0}^{N_2-1}\sum_{n_1=0}^{N_1-1} y(n_1,n_2)\,\mathrm{cas}\frac{2\pi k_1 n_1}{N_1}\mathrm{cas}\frac{2\pi k_2 n_2}{N_2} \tag{10}$$

where

$$y(n_1,n_2) = \frac{1}{2}[x(n_1,n_2) + x(N_1-n_1,n_2) + x(n_1,N_2-n_2) - x(N_1-n_1,N_2-n_2)] \tag{11}$$

C. Prime – factor Decomposition of the DCT

The discrete cosine transform (DCT) [12] of the sequence $\{x(n), n = 0, 1, \dots\dots N-1\}$ may be given by

$$C(k) = (2/N)^{1/2} \in(k)\sum_{n=0}^{N-1} x(n)\cos[\pi(2n+1)k/(2N)] \tag{12}$$

and the inverse discrete cosine transform (IDCT) is defined by

$$x(n) = (2/N)^{1/2}\sum_{k=0}^{N-1} \in(k)C(k)\cos[\pi(2n+1)k/(2N)] \tag{13}$$

where

$$\in(k) = \begin{cases} (2)^{-1/2} & \text{for } k = 0 \\ 1 & \text{for } 1 \le k \le N-1 \end{cases}$$

Scaling factor $\in(k)$ and normalising factor $(2/N)^{1/2}$ in (12) and (13), may, however be ignored to obtain

$$x(n) = \sum_{k=0}^{N-1} C(k)\cos[\pi(2n+1)k/(2N)] \tag{14}$$

When transform length $N = N_1 \times N_2$, N_1 and N_2 being relatively prime the indices n and k in (14) may be mapped into (n_1, n_2) and (k_1, k_2) as

$\overline{n_1} = n \bmod 2N_1$ and $\overline{n_2} = n \bmod 2N_2$

$$n_1 = \begin{cases} \overline{n_1} & \text{if } \overline{n_1} < N_1 \\ 2N_1 - 1 - \overline{n_1} & \text{otherwise} \end{cases} \tag{15a}$$

and $k = (N_2 k_1 + N_1 k_2) \bmod N$ (15b)

Using (15),(14) may be expressed as

$$x(n_1,n_2) = \sum_{k_1=0}^{N_1-1}\sum_{k_2=0}^{N_2-1} y(k_1,k_2)\cos\frac{\pi(2n_1+1)k_1}{(2N_1)}\cos\frac{\pi(2n_2+1)k_2}{(2N_2)} \tag{16}$$

where

$$y(k_1,k_2) = \begin{cases} C(k_1,k_2) & \text{if } (k_1,k_2) \in E \\ C(k_1,k_2) + C(k_1,N_2-k_2) & \text{if } (k_1,k_2) \in A \\ C(k_1,k_2) + C(N_1-k_1,k_2) & \text{if } (k_1,k_2) \in B \\ -C(N_1-k_1,N_2-k_2) + C(N_1-k_1,k_2) & \text{if } (k_1,k_2) \in C \\ -C(N_1-k_1,N_2-k_2) + C(k_1,N_2-k_2) & \text{if } (k_1,k_2) \in D \end{cases} \tag{17}$$

$$\begin{aligned} E &= \{ (k_1,k_2) \mid k_1 = 0 \text{ or } k_2 = 0 \} \\ A &= \{ (k_1,k_2) \mid f(k_1,k_2) < N \text{ and } g(k_1,k_2) > 0 : k_1k_2 \neq 0 \} \\ B &= \{ (k_1,k_2) \mid f(k_1,k_2) < N \text{ and } g(k_1,k_2) < 0 : k_1k_2 \neq 0 \} \\ C &= \{ (k_1,k_2) \mid f(k_1,k_2) > N \text{ and } g(k_1,k_2) < 0 : k_1k_2 \neq 0 \} \\ D &= \{ (k_1,k_2) \mid f(k_1,k_2) > N \text{ and } g(k_1,k_2) > 0 : k_1k_2 \neq 0 \} \end{aligned} \tag{18}$$

$f(k_1,k_2) = N_2k_1 + N_1k_2$ and $g(k_1,k_2) = N_2k_1 - N_1k_2$

Due to orthonormal feature of the DCT, the forward transform, may however, be realized by the transpose of the inverse transform.

D. Unified Systolic Architecture for Implementation of DFT, DHT and the DCT

Equations (4) (10) and (16) may be expressed in a common form :

$$\mathbf{X}^{T} = \mathbf{D}\,[\mathrm{C}\,\mathbf{Y}]^{T} \tag{19}$$

Where, **X** and **Y** are matrices of size $N_1 \times N_2$ while **C** and **D** are matrices of sizes $N_1 \times N_2$ and $N_2 \times N_2$, respectively, which represent the transform kernel. For avoiding the transpose operation, (4),(10) and (16) may otherwise be expressed as

$$X_{lm} = \sum_{j=0}^{N_2-1} Z_{lj} D_{mj} \tag{20a}$$

for

$$Z_{lj} = \sum_{i=0}^{N_1-1} C_{li} Y_{ij} \qquad (20b)$$

where l = 0 , 1, …, N_1 -1 and m = 0,1,…, N_2 -1

$$Y_{ij} = \left[\begin{array}{ll} x\,(i,j) & \text{for DFT} \\ Y\,(i,j) & \text{for DHT as given by (11)} \\ Y\,(i,j) & \text{for DCT as given by (17) and (18)} \end{array}\right. \qquad (21)$$

$$C_{lj} = \left[\begin{array}{ll} e^{-j\ 2\pi li/N_1} & \text{for DFT} \\ \text{cas}[\,2\pi li/N_1\,] & \text{for DHT} \\ \cos\,[\pi\,(2l+1)\,/\,(\,2N_1)] & \text{for DCT} \end{array}\right. \qquad (22)$$

$$D_{mj} = \left[\begin{array}{ll} e^{-j\ 2\pi mj\,/N_2} & \text{for DFT} \\ \text{cas}[\,2\pi mj/N_2\,] & \text{for DHT} \\ \cos\,[\pi\,(2m+1)\,j/\,2N_2)] & \text{for DCT} \end{array}\right. \qquad (23)$$

As given by (20), each of these transforms may be computed in two distinct stages. In the first stage, one has to perform multiplication of matrix [Y_{ij}] of size N_1 x N_2 with N_1 – point transform kernel [C_{li}] of size N_1 x N_1 to obtain an intermediate matrix [z_{lj}] of size N_1 x N_2 (20b) . In the second stage, each row of intermediate matrix [z_{lj}] is multiplied with the rows of N_2- point transform kernel [D_{jm}] of size N_2 X N_2 , according to (20a). Multiplications of both these stages may be mapped into a systolic mesh containing N_1x N_2 PEs for fully pipelined processing. The proposed systolic structure for computing N- point transform, ($N = N_1$ x N_2) , is shown in Fig. 1a. The function of each PE is depicted Fig . 1b. The first row of the N_1- point transform kernel [C_{li}] is fed to the first array. The successive rows of the transform kernels are fed to the successive arrays, staggered by one time-step with respect to the preceding one. The first column of the input matrix [Y_{ij}] is fed to the first PE of the first array. The successive columns are fed to the successive PEs of the first array in subsequent time-steps. The columns of the N_2 – point transform kernel [D_{jm}] are fed to the different PEs of the first array at the lag of N_1 time – steps with respect to the corresponding columns of the input matrix [Y_{ij}]. In the first stage of computation, the (j +1) th PE of (l + 1) th array computes an element Z_{lj} of the intermediate matrix in N_1 time – steps , where a PE performs a multiplication and adds the result to the content of the accumulator A_1 , in every time – step . At the end of N_1 time – steps , this accumulator content is transferred to the accumulator A_2 while A_1 is reset to zero . In the second stage of computation, in each array , the multiplication of one row of the intermediate matrix [Z_{lj}]

III. STRUCTURE FOR HIGH THROUGHPUT PRIME-FACTOR DHT, AND SCHEME FOR COMPUTATIONOF DFT FROM THE PROPOSED DHT STRUCTURE

A. Algorithm for Systolic Implementation of the DHT

The arguments of sine and cosine functions of (6) may be expanded to yield

$$H(\,k_1, k_2\,) = \sum_{n_2=0}^{N_2-1} w\,(\,k_1, n_2\,)\left[\cos\frac{2\pi k_2 n_2}{N_2} + \sin\frac{2\pi k_2 n_2}{N_2}\right] \qquad (24)$$

where S

$$w(k_1, n_2) = \sum_{n_1=0}^{N_1-1} y\,(\,n_1, n_2\,)\ \text{cas}\,\frac{2\pi k_1 n_1}{N_1} \qquad (25)$$

Equation (24) can be expressed as

$$H(k_1, k_2) = \sum_{n_2=0}^{(N_2-1)/2} \left[Z_1\,(\,k_1, n_2)\cos\frac{2\pi k_2 n_2}{N_2} + Z_2(k_1, n_2)\,\sin\frac{2\pi k_2 n_2}{N_2}\right]$$

for k_1 = 0,1,2,…, (N_1- 1) /2 and k_2 = 0,1,2,…, (N_2 - 1) /2 (26a)

and

$$H(k_1, N_2 - k_2) = \sum_{n_2=0}^{(N_2-1)/2} \left[Z_1\,(\,k_1, n_2\,)\cos\frac{2\pi k_2 n_2}{N_2} + Z_2(k_1, n_2)\,\sin\frac{2\pi k_2 n_2}{N_2}\right]$$

for k_1 = 0,1,2,…, (N_1- 1) /2 and k_2 = 1,2,…, (N_2 - 1) /2 (26b)

where

$$Z_1\ (\,k_1, n_2\,) = w\,(\,k_1, n_2\,) + w\,(\,k_1, N_2\text{-}\,n_2) \qquad (27)$$

$Z_2\ (k_1, n_2) = w\ (k_1, n_2) - w\ (k_1, N_2 - n_2)$

for $n_2 = 1,2,\ldots,(N_2 - 1)/2$, and $Z_1\ (k_1, 0) = Z_2\ (k_1, 0) = w\ (k_1, 0)$

Using (25) and (11), (27), may be simplified to yield

$$Z_1(k_1,n_2) = \sum_{n_1=0}^{(N_1-1)/2} \mathrm{A}(n_1,n_2)\cos\frac{2\pi k_1 n_1}{N_1} + \mathrm{B}(n_1,n_2)\sin\frac{2\pi k_1 n_1}{N_1} \tag{28}$$

and

$$Z_2(k_1,n_2) = \sum_{n_1=0}^{(N_1-1)/2} \mathrm{C}(n_1,n_2)\cos\frac{2\pi k_1 n_1}{N_1} + \mathrm{D}(n_1,n_2)\sin\frac{2\pi k_1 n_1}{N_1} \tag{29}$$

where ,

$$\mathrm{A}(n_1, n_2) = [x(n_1,n_2) + x(n_1,N_2-n_2) + x(N_1-n_1,n_2) + x(N_1-n_1,N_2-n_2)] \tag{30}$$

$$\mathrm{B}(n_1,n_2) = [x(n_1,n_2) + x(n_1,N_2-n_2) - x(N_1-n_1,n_2) - x(N_1-n_1,N_2-n_2)] \tag{31}$$

$$\mathrm{C}(n_1,n_2) = [x(n_1,n_2) + x(N_1-n_1,n_2) - x(N_1-n_1,N_2-n_2) - x(n_1,N_2,-n_2)] \tag{32}$$

$$\mathrm{D}(n_1,n_2) = [x(n_1,N_2-n_2) + x(N_1-n_1,n_2) - x(n_1,n_2) - x(N_1-n_1,N_2-n_2)] \tag{33}$$

for $n_1 = 1,2,\ldots.,(N_1 - 1)/2$ and $n_2 = 1,2,\ldots.,(N_2 - 1)/2$

and

$\mathrm{A}\ (0, n_2) = \mathrm{B}(0, n_2) = x\ (0, n_2) + x(0, N_2 - n_2)$

$\mathrm{C}\ (0, n_2) = \mathrm{D}\ (0, n_2) = x\ (0, n_2) - x(0, N_2 - n_2)$

for $n_2 = 1,2,\ldots\ (N_2-1)/2$

$\mathrm{A}(n_1,0) = \mathrm{C}\ (n_1, 0) = x\ (n_1,0) + x(N_1-n_1, 0)$

$\mathrm{B}(n_1,0) = \mathrm{D}(n_1,0) = x(n_1,0) - x\ (N_1-n_1, 0)$

for $n_1 = 1,2,..,(N_1 - 1)/2$

$$\mathrm{A}(0,0) = \mathrm{B}\ (0,0) = x(0,0)\ ,\ \mathrm{C}\ (0,0) = \mathrm{D}\ (0,0) = x(0,0) \tag{34}$$

Substituting (N_1-k_1) for k_1 in (26 a) and (26b), respectively, one may have

$$H(N_1-k_1,k_2) = \sum_{n_2=0}^{(N_2-1)/2}\left[Z_1(N_1-k_1,n_2)\cos\frac{2\pi k_2 n_2}{N_2} + Z_2(N_1-k_1,n_2)\sin\frac{2\pi k_2 n_2}{N_2}\right]$$

for $k_1 = 1,2,\ldots,(N_1-1)/2$ and $k_2 = 0,1,\ldots,(N_2-1)/2$ (35a)

and

$$H(N_1-k_1,N_2-k_2) = \sum_{n_2=0}^{(N_2-1)/2}\left[Z_1(N_1-k_1,n_2)\cos\frac{2\pi k_2 n_2}{N_2} - Z_2(N_1-k_1,n_2)\sin\frac{2\pi k_2 n_2}{N_2}\right]$$

for $k_1 = 1,2,\ldots,(N_1-1)/2$ and $k_2 = 1,2,\ldots,(N_2-1)/2$ (35b)

where

$$Z_1(N_1-k_1, n_2) = w\ (N_1-k_1, n_2) + w\ (N_1-k_1, N_2-n_2) \tag{36}$$

$Z_2(N_1-k_1, n_2) = w\ (N_1-k_1, n_2) - w\ (N_1-k_1, N_2-n_2)$

for $n_2 = 1,2,..,(N_2-1)/2$, $Z_1(N_1-k_1,0) = Z_2\ (N_1-k_1,0) = w\ (N_1-k_1,0)$

Using (25) and (11), (36) can be simplified to yield

$$Z_1(N_1-k_1,n_2) = \sum_{n_1=0}^{(N_1-1)/2} \mathrm{A}(n_1,n_2)\cos\frac{2\pi k_1 n_1}{N_1} - \mathrm{B}(n_1,n_2)\sin\frac{2\pi k_1 n_1}{N_1} \tag{37}$$

and

$$Z_2(N_1-k_1,n_2) = \sum_{n_1=0}^{(N_1-1)/2} \mathrm{C}(n_1,n_2)\cos\frac{2\pi k_1 n_1}{N_1} - \mathrm{D}(n_1,n_2)\sin\frac{2\pi k_1 n_1}{N_1} \tag{38}$$

B. Computation of the Prime – factor DFT and DCT from DHT

From (1) and (5) it may be shown that

$$F(k) = [\ H(k) + H(N-k)\ ]/2\ - j\ [\ H(k) - H(N-\mathrm{k})\ ]/2 \tag{39}$$

Using the mapping of (2a), the prime –factor DFT components may be computed from the DHT components as :

$$F(k_1, k_2) = [H(k_1,k_2) + H\ (N_1-k_1, N_2-k_2)]/2 - j\ [H\ (k_1,k_2) - H\ (N_1-k_1,N_2-k_2)]/2 \tag{40}$$

It is shown in (34) that the DCT of (12) can be expressed as

$$C(k) = \frac{1}{2}\ [\ H\ (k)\ \mathrm{cas}\ (k\pi/2N) + H\ (N-k)\ \mathrm{cas}\ (k\pi/2N)] \tag{41}$$

where { $H\ (k)$ } represents N – point DHT of { $\bar{x}(n)$ }

$$\text{given that}\quad \bar{x}(n) = \begin{cases} x\ (2n) & 0 \le n \le (\frac{N}{2}) - 1 \\ x\ (2N - 2n - 1) & \frac{N}{2} \le n \le N - 1 \end{cases} \tag{42}$$

The prime – factor DCT may be thus be obtained from DHT as

$$C\,(k_1\,,\,k_2) = \frac{1}{2}\quad [H\,(k_1\,,\,k_2)\ \text{cas}\ (-k\pi/2N) + H\,(N_1 - k_1,\,N_2 - k_2)\ \text{cas}\ (k\pi/2N)] \tag{43}$$

where k is given by (2a)

C. Systolic Architecture for High Throughput Computation of Prime – factor DHT

The proposed bilayer architecture for computation of prime – factor DHT consists of two layers of systolic arrays placed one over the other. For computation (N_1 x N_2) – point DHT, the lower layer consists of (N_2+1) / 2 linear arrays and the upper layer consists of (N_1+1)/2 linear arrays as shown in Fig. 2a and 3a, respectively. The input samples are fed to the arrays in the lower layer, while output samples are obtained from the arrays of the upper layer. Therefore the arrays of the lower layer termed as the input arrays and the arrays of the upper layer as the output arrays. Each input array consists of (N_1+1)/2 number of locally connected identical PE-1s. Function of each PE-1 is shown in Fig. 2b. Similarly, each output array consists of (N_2+1)/2 number of locally connected identical PE-2s. The function of each PE-2 is shown in Fig. 3b. The lower layer makes the first stage of computation to provide the intermediate results [Z_1(k_1, n_2)] and [Z_2(k_1, n_2)] to the upper layer. The upper layer makes the second stage of computation to yield the desired DHT components. The elements of n_2th column of A(n_1,n_2), B(n_1,n_2), C(n_1,n_2) and D(n_1,n_2) are fed to the (n_2+1) th input array staggered by one time – step with respect to the input of n_2 th input array. The output arrays of the upper layer are placed orthogonally with respect to the input arrays of the lower layer, such that each PE in the output array is placed over a PE of the input array. Each PE in the output array, therefore, receives its desired input in the proper sequence of time.

From the last PE-2s of the output arrays, the structure provides four DHT components H(k_1,k_2), H(N_1−k_1, k_2), H (N_1, N_2−k_2) and H(N_1−k_1, N_2−k_2) simultaneously. Therefore, the DFT of real-valued data, as well as, the DCT can conveniently be computed from the output of the structure according to equations (40) and (43).

IV. CONCLUSION

In this paper we have suggested a unified systolic mesh architecture for the implementing the prime – factor DFT, DHT and the DCT. For implementing DHT, we have suggested a simple scheme for prime – factor decomposition. Also, we have suggested an efficient algorithm for high throughput implementation of the prime – factor DHT using a highly compact 2-D systolic architecture. It is shown that the DCT, as well as, DFT of real-valued data can also be obtained from the output of the DHT structure.

The proposed unified systolic architecture (Fig. 1a) requires N_1 x N_2 number of identical PEs. In each PE there are two multipliers, two adders and two accumulators. The area complexity of the proposed structure is O (N_1 x N_2). The first transform component is obtained after (N_1+N_2) time – steps. The first set of transform components is obtained after 2 (N_1+N_2–1) time –steps. However, the successive sets of transform components are obtained in N_2 time–steps.

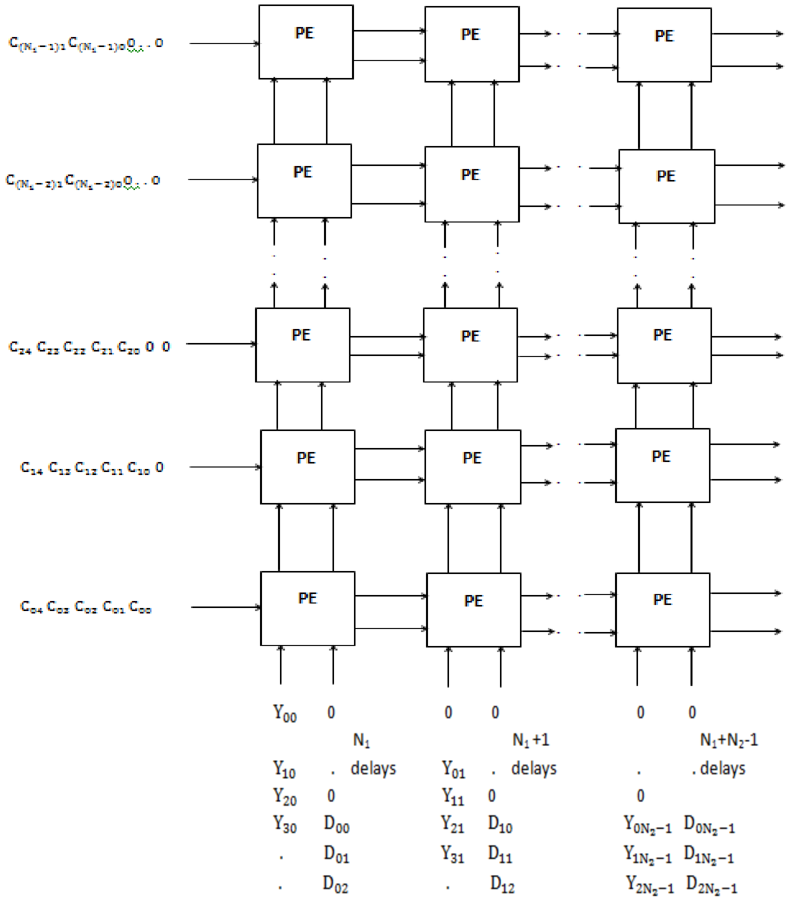
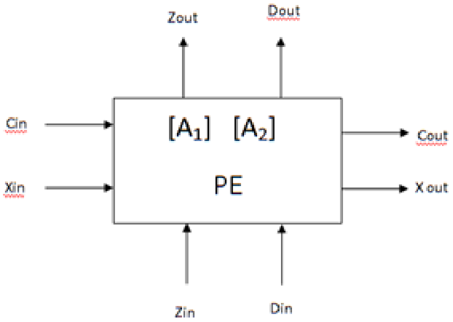

$C_{(N_1-1)1}\,C_{(N_1-1)0}\,0\ .\ .\ 0$
$C_{(N_1-2)1}\,C_{(N_1-2)0}\,0\ .\ .\ 0$
$C_{24}\,C_{23}\,C_{22}\,C_{21}\,C_{20}\ 0\ 0$
$C_{14}\,C_{13}\,C_{12}\,C_{11}\,C_{10}\ 0$
$C_{04}\,C_{03}\,C_{02}\,C_{01}\,C_{00}$
PE
Y_{00} 0 0 0 0 0
N_1 delays
N_1+1 delays
N_1+N_2-1 delays
Y_{10} . Y_{01} . .
Y_{20} 0 Y_{11} 0 0
Y_{30} D_{00} Y_{21} D_{10} Y_{0N_2-1} D_{0N_2-1}
. D_{01} Y_{31} D_{11} Y_{1N_2-1} D_{1N_2-1}
. D_{02} . D_{12} Y_{2N_2-1} D_{2N_2-1}

Fig. 1 a: Unified systolic architecture for implementation of the DFT, the DHT and the DCT

The throughput rate of the proposed structure would, therefore, be $R = (N_1 / T)$ where T is the duration of the time step given by $T = (T_{\text{mult}} + T_{\text{add}})$. T_{mult} and T_{add} are respectively the time required for performing a real multiplication and a real addition in the PE. It is interesting to note that the transposition of the intermediate matrix is avoided in this structure by orthogonal processing during the pair of matrix multiplication, i.e if the processing for the first matrix multiplication takes place along X – direction, the processing for the second matrix multiplication is carried out along Y– direction. Due this feature, the structure is highly compact, offers saving of transposition hardware and at the same time yields high thourghput with less latency. The proposed bilayer DHT structure (Fig. 2a) requires (N_1+1) (N_2+1) / 4 number of PEs. There are four multipliers, four adders and four accumulators in each PE. There are four multipliers and four adders in each PE- 2 of the output arrays. It gives the first DHT component after [$\frac{1}{2}(N_1 + N_2) + 1$] time – steps. First set of DHT components are obtained in $(N_1 + N_2 - 1)$ time – steps . However, successive sets of DHT are obtained in every $(N_2+ 1)/2$ times steps. The through put the rate of the structure would, therefore, be $R = 2\ (N_1 + 1)/T$. The transposition of the intermediate output is avoided here by orthogonal alignment of the output arrays with respect to the input arrays so as to save the hardware for transposition, to reduce the chip area and latency. The area and time complexities of the bilayer DHT structure are nearly (¼) and ½ times that of the proposed unified structure, while both the structure require nearly the same amount of hard ware.



ALGORITHM

```
1.  $A_2 = A_1$
    $A_1 = 0$
2.  $A_1 = A_1 + Cin.Zin$
    X out=Xin+$A_2$.Din
    Cout= Cin
    Dout= Din
    Zout = Zin
    Count=Count+1
    If(Count=$N_1$) goto 1
    else
    goto 2
    endif
```

Fig . 1b: Function of each PE.

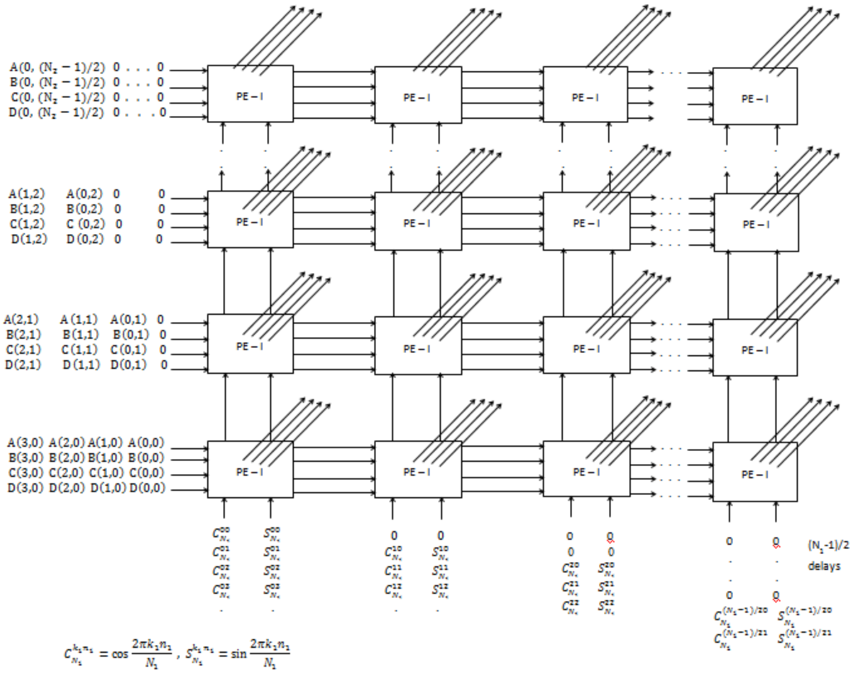
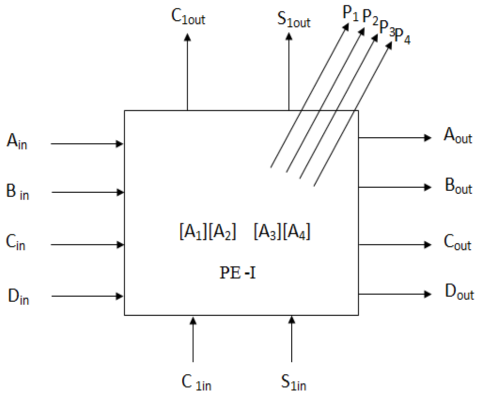

A(0, (N₂ – 1)/2) 0 . . . 0
B(0, (N₂ – 1)/2) 0 . . . 0
C(0, (N₂ – 1)/2) 0 . . . 0
D(0, (N₂ – 1)/2) 0 . . . 0
A(1,2) A(0,2) 0 0
B(1,2) B(0,2) 0 0
C(1,2) C(0,2) 0 0
D(1,2) D(0,2) 0 0
A(2,1) A(1,1) A(0,1) 0
B(2,1) B(1,1) B(0,1) 0
C(2,1) C(1,1) C(0,1) 0
D(2,1) D(1,1) D(0,1) 0
A(3,0) A(2,0) A(1,0) A(0,0)
B(3,0) B(2,0) B(1,0) B(0,0)
C(3,0) C(2,0) C(1,0) C(0,0)
D(3,0) D(2,0) D(1,0) D(0,0)
PE – I
(N₁-1)/2
delays
$C_{N_1}^{k_1 n_1} = \cos\frac{2\pi k_1 n_1}{N_1}$, $S_{N_1}^{k_1 n_1} = \sin\frac{2\pi k_1 n_1}{N_1}$

Fig.2a: Structure of the lower layer of the bilayer DHT architecture



```
1.      $P_1 = A_1 + A_2$
        $P_2 = A_3 + A_4$
        $P_3 = A_1 - A_2$
        $P_4 = A_3 - A_4$
        $A_1 = A_2 = A_3 = A_4 = 0$
        Count=0
2.
        $A_1 = A_1$ +Ain.$C_1$ in
        $A_2 = A_2$ +Bin.$S_1$ in
        $A_3 = A_3$ +Cin.$C_1$ in
        $A_4 = A_4$ +Din.$S_1$ in
        Aout = Ain
        Bout= Bin
        Cout=Cin
        Dout= Din
        Count=Count+1
        If(Count= $(N_1+1)/2$) then
        goto 1
        else
        goto 2
        end if
```

$$C_{1in} = \cos\frac{2\pi k_1 n_1}{N_1}$$

$$S_{1in} = \sin\frac{2\pi k_1 n_1}{N_1}$$

Fig.2b: Function of a processing element-I of the input array

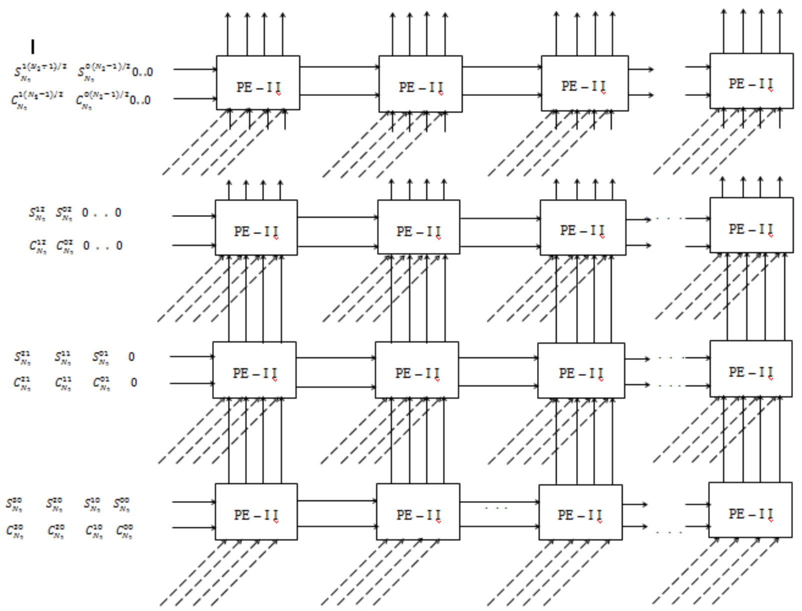
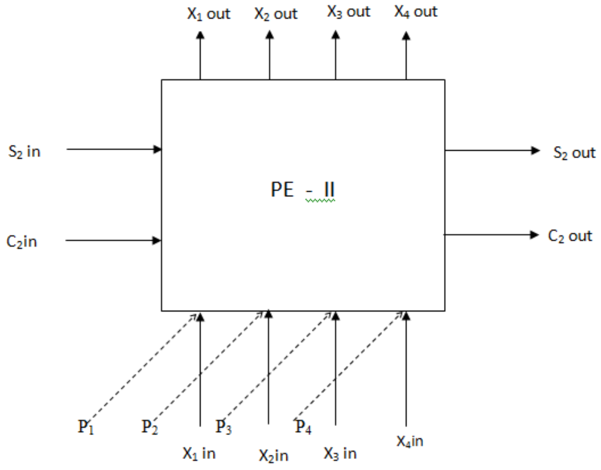


Fig. 3a: Structure of the upper layer of the bilayer DHT architecture



For continuous processing in every time-step

C_2out= C_2 in

S_2out=S_2 in

X_1out= X_1 in + P_1.C_2 in

X_2out= X_2 in + P_2. S_2 in

X_3out= X_3 in + P_3. C_2 in

X_4out= X_4 in + P_4. C_2 in

Fig.3b function of processing element – II of the output array

C_{2in} =cos$\frac{2\pi k_2 n_2}{N_2}$, S_{2in} = sin$\frac{2\pi k_2 n_2}{N_2}$

REFERENCE

[1] J. W. Cooley and J. W. Tukey, "An algorithm for machine calculation of complex Fourier series" *Math. Comput.* vol.19, pp.297-301, Apr.1965.

[2] C. M. Rader and N .M. Brenner,'' A new principle for fast Fourier transformation," *IEEE Tarns. Aoust., Speech, Signal Processing,* vol.ASSP-24, pp.264-266,Apr.1976.

[3] D. P. Kolba and T. W. Parks,'' A prime-factor FFT algorithm using high-speed convolution ," *IEEE Tarns. Acoust., Speech, Signal Processing*, vol.ASSP-25, No.4, pp.281-294, Aug.1977.

[4] H. F. Silverman, '' An introduction to programming the Winograd Fourier transform algorithm(WFTA)," *IEEE Tarns.Acoust., Speech, Signal Processing*, vol. ASSP-25, pp. 152-165, Aug. 1977.

[5] R. N. Bracewell, "The discrete Hartley transform," *J. Opt. Soc. Am.*, vol. 73, pp. 1832 – 1835, 1983.

[6] D. M. W. Evans, " An improved digit – reversal permutation algorithm for fast Fourier and Hartley transforms, " *IEEE Trans. Acoust., Speech, Signal Processing*, vol. ASSP – 35, No.8, pp.1120 – 1125 , Aug. 1987.

[7] H. Hao, "On fast Hartley transform algorithm," *Proc. IEEE*, vol.75, pp.961-962, July 1987.

[8] H. S. Hou, "The fast Hartley transform algorithm," *IEEE Tarns. Comput.*, vol.C-36, No. 2, pp.147-156, Feb. 1987.

[9] P. K. Meher, J. K. Satapathy, and G.Panda, '' New high speed prime-factor algorithm for discrete Hartley transform," *IEE Proceedings*-F, vol.140, No.1, Feb. 1993.

[10] H. V. Sorensen, D. L. jones, C. S. Burrus, and M. T. Heideman, "On computing the discrete Hartley transform," *IEEE Trans. Acoust., Speech, Signal Processing*, vol.ASSP-33, No 4, pp 1231 -1238, Oct.1985.

[11] D. Yang, " Prime-factor fast Hartley transform," *Electron Lett.*, vol. 26, No.2, pp. 119-121, Jan. 1990.

[12] N. Ahmed, T. Natarajan, and K. R. Rao, "Discrete cosine transform," *IEEE Trans. Comput.*, vol.C-23, pp. 90-93, Jan. 1974.

[13] N. S. Jayant and P. Noll, "*Digital coding of waveforms*," Englewood Cliffs, New Jersey, Prentice-Hall, 1984.

[14] R. J. Clarke," Relation between the Karhunen Loeve and cosine transform," *IEEE Proc.*, vol.128, Pt. F, No.6, Nov.1981.

[15] M. J. Narasimha and A. M. Peterson, " On the computation of discrete cosine transform, " *IEEE Trans. Commun.*, vol. COM – 26, pp. 934 – 936 , June 1978.

[16] J. Makhoul," A fast cosine transform in one and two dimensions, " *IEEE Trans. ASSP*, vol. ASSP – 28, pp.27 – 34 , Feb. 1980.

[17] P. P. N. Yang and M. J. Narasimha," Prime factor decomposition of the discrete cosine transform," in *Proc. IEEE Int. Conf. Acoust., Speech, Signal Processing*, pp. 772 – 775, 1985.

[18] B. G. Lee, " Input and output index mapping for a prime - factor decomposed computation of discrete cosine transform," *IEEE Trans. Acoust. , Speech, Signal Processing*. vol- 37, No.2, pp. 237-244, Feb. 1989

[19] H. S. Hou, "A fast recursive algorithm for computing the discrete cosine transform ," *IEEE Trans. Acoust. , Speech, Signal Processing,* vol. ASSP – 35, No. 10, pp. 1455-1461, Oct.1987.

[20] W. Li, "A new algorithm to compute the DCT and its inverse," *IEEE Trans. Signal Processing,* vol. 39, No. 6, pp.1305-1313. June 1991.

[21] M. T. Heideman, " Computation of an odd-length DCT from a real valued DFT of the same length," *IEEE Trans , Signal Processing,* vol.40, No.1, pp.54-61, Jan.1992.

[22] P. Z. Lee, and F. Y. Huang, "An efficient prime-factor algorithm for the discrete cosine transform and its hardware implementations," *IEEE Trans. Signal Processing,* vol.42, No.8, pp.1996-2005, Aug. 1994.

[23] H.T. Kung , " Why Systolic architecture," *IEEE Trans. Computer,* vol. 15, No. 1, pp.37-46, Jan. 1982.

[24] R. M. Owens and J. Ja' Ja', "A VLSI chip for the Winograd / prime factor algorithm to compute the discrete Fourier transform," *IEEE Trans. Acoust., Speech, Signal Processing* , vol. ASSP-34, pp.979-989, Aug.1986.

[25] J. A. Eldon," Fourier on chip," *VLSI Signal Processing, vol. III , R. W. Brodersen, H. S. Moscovitz, Eds. IEEE Press,* pp.15-20, 1988.

[26] S. Shen *et al*, "A high performance CMOS chip for FFT processors," in *Proc. IEEE Conf. Camp. Design, VLSI in Computers,* pp. 578 – 581, May 1988.

[27] N. I. Cho and S. U. Lee," DCT algorithms for VLSI parallel implementations," *IEEE Trans. Acoust., Speech, Signal Processing,* vol.38, No.1, pp. 121 – 127, Jan. 1990.

[28] C. Chakrabarti and J. Ja' Ja'," Optimal systolic designs for computing DHT and DCT, " in *VLSI Signal Processing, vol. III, R. Brodersen, H. Moscovitz, Eds. IEEE Press,* pp. 411 – 422 ,Nov. 1988.

[29] C. Chakrabarti and j. Ja' Ja' , " Systolic architecture for the computation of the discrete Hartley and discrete cosine transforms based on prime factor decomposition," *IEEE Trans . Comput.,* vol. 39 , pp. 1359-1368, Nov.1990.

[30] L. W. Chang and S.W. Lee, " Systolic arrays for the discrete Hartley transform, "*IEEE Trans. Signal Processing,* vol. SP-39, No. 11, pp. 2411-2418, 1991.

[31] P. K. Meher , J. K. Satapathy, and G. Panda " Efficient systolic solution for a new prime-factor discrete Hartley transform algorithm," *IEE Proc-G,* vol. 140, pp. 135-139, Apr.1993.

[32] S. C. Chan and K. L. Ho, " Prime-factor real-valued Fourier, Cosine, and Hartley transform" , *Sixth European Signal Processing Conf.,* pp. 1045-1048, Aug.1992.

[33] C. S. Burrus, "Index mappings for multidimensional formulation of the DFT and convolution," *IEEE Trans. Acoust., Speech, Signal Processing*, vol. ASSP-25 ,No.3, pp. 239-242, June 1977.

[34] H. Malvar ," Fast Computation of discrete cosine transform through fast Hartley transform," *Electron. Lett*., vol.22, pp. 353-354,Mar.1986.