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Single Electron Transistor Made Nano-Hybrid-Counters for Advanced High Speed Computing

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Abstract— Single Electron Transistor (SET) technology insights numerous possibilities of achieving ultra high functional density and exceptionally low power dissipation paralleled to conventional CMOS technology. In this work the authors enumerated the implementation of SET based Nano-Hybrid-Counter circuit based on logic realizations using SET. The schematic diagram along with simulation results is presented here. The novel circuit endorse excellent trade off when compared to conventional hybrid counters.

Keywords— Single electronics, tunnelling, Coulomb Blockade, tunnel junctions and Nano-Hybrid-Counter

I. INTRODUCTION

Single electronics initiated as an incipient meadow of rising interest from the point of view of both academic and industry owing to its applications to modern and future electronics [1]. Single electronics employs the transfer of single electron tunnelling properties to exemplify binary data values. The attainment of the Single Electron Devices is that it involves considerably less power than conventional technologies while operating at ample high speed [2]. Moreover, SET logic implementation rapidly pioneered as one of the innovative technologies where logic device sizes were limited only too few nano-scales and power dissipation reduced considerably. SET devices are requisite fundamentals in nano-electronics and thus Researchers emphasized in designing SET based memory [3], logic circuits [6], electron pumps [9] etc. Since its very inception, different logic gates, flip-flops, addition, multiplication, division and also other computational elements such as sequence generator, ALU etc. using single electron devices have been implemented [3] [4] [5] [7] [8].

Here, we present the nano IC design of a Hybrid Counter retaining Single Electron Devices (SED). The unique device comprises of more than 300 tunnel junctions and operates as a Hybrid Counter using single electron transport. The letter concisely confers the basic physics of single electron devices in the subsequent section; it is followed by deliberation of specific basic circuits of SET logic gates. Lastly, a novel nano Hybrid Counter is modelled and realized with SET logic devices.

II. SET ORTHODOX NOTION

A. SET Edifice

Fig. 1 depicts a SET encompassing two tunnel junction coupled in series known as a Coulomb Island. Electrons are permitted to enter by tunnelling in succession through one of the electrodes. The device configuration of SET is much identical to ordinary Field Effect Transistor (FET)s. The three terminals i.e. the outside terminal of each tunnel junction labelled as “Source and Drain” and the Gate terminal is capacitive-ly coupled to the node between the two tunnel junctions. Structurally the capacitor makes available the path of setting the electric charge on the Coulomb Island [10].

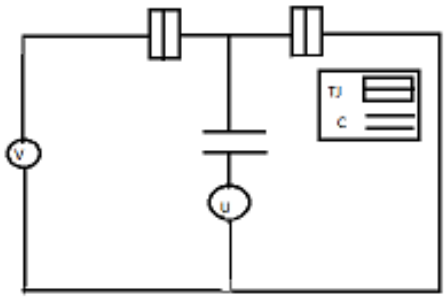

Fig. 1 SET Structural View

B. Coulomb Blockade Configuration

Coulomb Island promisingly is the most interesting portion in SET. The energy level of Coulomb Blockade is at much higher range compared to the tunnelling range of the electron on the source contact. Operationally, lower energy electrodes are placed entirely in the energy level of the island. Basically, at gate electrode positive voltage is applied; thereby the energy levels of the island electrodes are lowered.

There are three pre-conditions for Coulomb Blockade:-
The elementary charge (e) is greater than the bias voltage (V_{bias}) divided by the self-capacitance (C) of the island, i.e. V_{bias}<e/c.
The thermal energy that lies proximity to the source contact along with the thermal energy in the island which is aptly denoted by K_bT; it is required to be lower than the charging energy i.e K_bT<e^2c. [11]
The tunnelling resistance R_t is approximated to be higher than (h/e^2) (derived from Heisenberg's Uncertainty Principle).

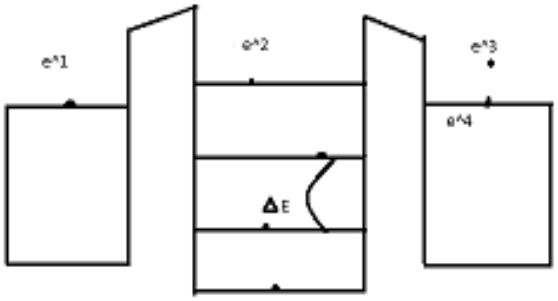

Fig. 2 Energy Level of the Island Electrode Coulomb Blockade

C. Passing of Electron through Tunnel Junction

The tunnelling of electron transpires from point to point of a tunnel junction to the opposite end point of the tunnel junction. The controlling strategic is that we requires Coulombs energy E_c to charge an island with an electron where E_c=e^2/2c>K_b.T
Where,
K_b= Boltzmann constant=1.38*10^-34 J/K
In this case coulomb energy is greater than available thermal energy and the movement of electron can be control by controlling the available energy supplied by voltage source [12 &13] as shown in Fig.3

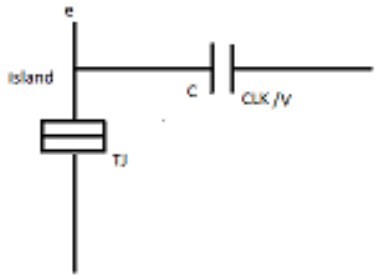

Fig. 3 Simple Electron Tunnelling Phenomena

III. MODELLING OF SET BASED HYBRID COUNTER

SETs are optimized as a competent authority in the next generation ICs. It is an obvious to explore all intrinsic qualities of SETs to develop fundamental logic gates in a wide-ranging manner. In this regard numerous research attempts have been categorically reported since the last decade [14-20].
This particular endeavour is an extended 'future work' of J. Gope et.al., [21-32] and here the authors accentuated to design unconventional hybrid counters using SETs.
Conventionally a Hybrid Counter is an extraordinary counter where the output behaves as a synchronous counter and drives the clock input of another counter to get a divide by 'N' operation. They are extensively used to acquire a symmetrical divided by 'N' output. For instance when' N' is any number divisible by 2 we can obtain a symmetrical divide by 'N' counters.

SET Circuit of Hybrid Counters

Fig.4 enumerates the proposed SET Hybrid Counter consisting of roughly 300 Tunnel Junctions and nearly same number of capacitors. The authors humbly admit that the design was quite complex; thus it was fascinating but challenging. Moreover, owing to circuit clarity the metaphors of input voltage and other few common peripherals was intentionally limited. The output waveform is annexed subsequently in Fig.5

Comparative Study of the Circuit

The significant of this proposed design is that it has the potential of providing much more component density thereby reducing the future IC sizes. Apart of this, the proposed circuit is quite faster than any conventional CMOS based circuit. Such comparisons provide a valuable reason to adopt SET based designing of such computational tools. The power dissipation for switching a single bit is of few nW which is considerably small when compared to conventional devices.
Fig. 6 and Fig.7 shows the comparison of propagation delay and fastness for the designed decision making system using conventional and Spin based gates.

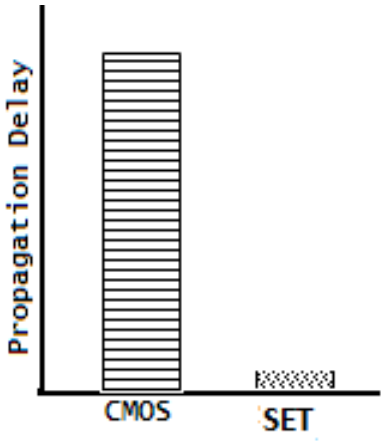

Fig. 6 Comparative Study of Propagation Delay

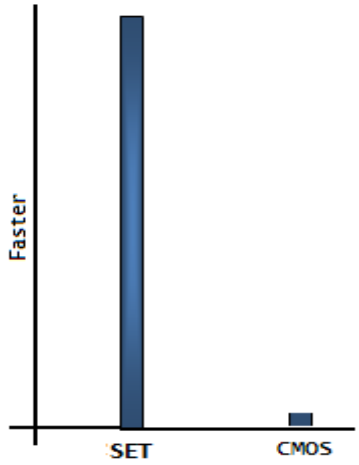

Fig. 7 Comparative Study of Speed

IV. CONCLUSIONS

The authors once again take the privilege to reveal the salient features and performance of SETs. Materialistically, it is absolutely superior equated to conventional FETs due to their nano size. Other noteworthy incentives related to CMOS circuit are low energy consumption, high sensitivity, higher operating speed and simplified operational principle. The contemporary era that stresses in supremacy includes nano dimensional, longer battery life and easy portable consumer electronics into daily life and the same can be apprehended only by SET. Moreover, it is quite simple but robust. In such circumstances SET has positioned in the premier place among other post CMOS devices. Further, the aspiring logical operation when implemented by SET creates bigger panorama in future generation logic circuit. The same is attributed here in this letter.

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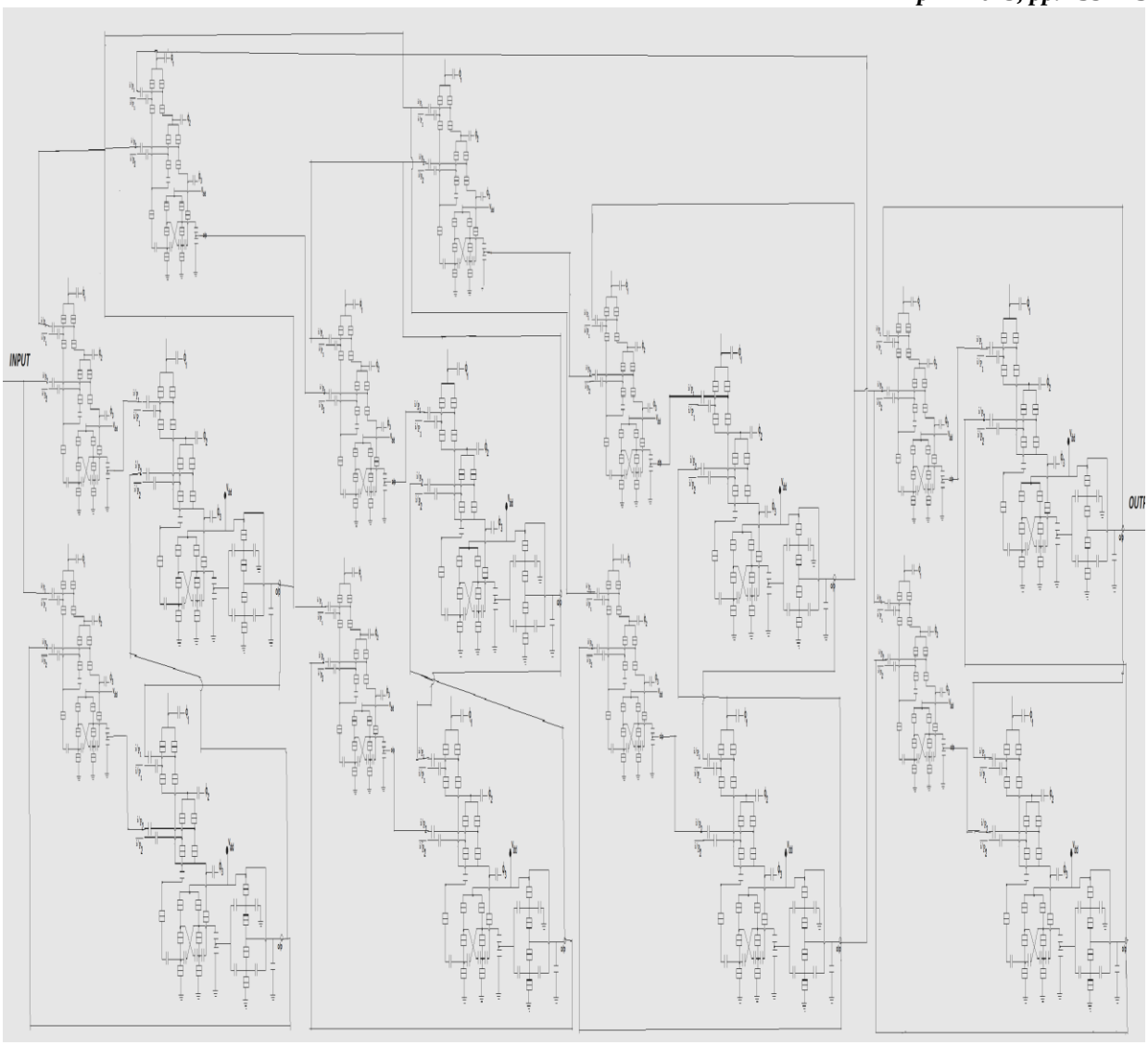

Fig. 4 Proposed Circuit Diagram of SET based Nano-Hybrid –Counter

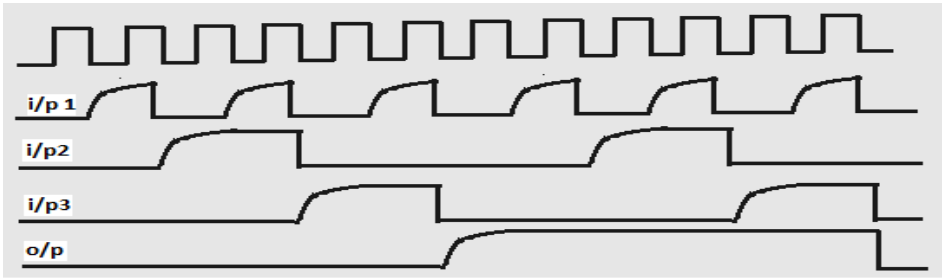

Fig. 5 Output Waveform of the operation of proposed SET based Nano-Hybrid -Counter

