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Design and Simulation of FPGA's Based Nuclear Spectroscopy using Single Channel Multiple Output Analyzer (SCMOA)

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Abstract : FPGA is popular for prototyping the digital circuits design. This paper describes the designing and simulation of FPGAs based Single Channel Multiple Output Analyzer (SCMOA) and compare with multiple channel analyzer used in nuclear spectroscopy. SCMOA circuits is designed by writing program in Very High Speed Integrated Circuit Hardware Description Language (VHDL). SCMOA was working on maximum frequency 121.536MHz. 51 Slices out of 3,584 and 41 Slice Flip Flops out of 7,168 were used. ModelSim SE 6.5 simulator is used for simulation and implemented on Xilinx Sparton-3 xc3s400-4pq208.

Keywords -Nuclear spectroscopy, Pulse Height Analysis, Multi-Channel Analyzer, Single Channel Multiple Output Analyzer, FPGAs, VHDL

I. INTRODUCTION

Spectroscopy system is used to measure radiation of the radiation source, by measuring the energy distribution of the particle [1]. According to the theory of Pulse Height Analysis in various books, by measuring the height of the pulse, we can measure the energy of the particle [7].

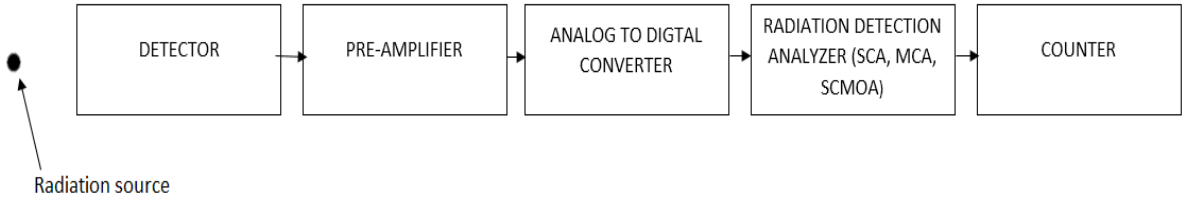

Figure.1: Block diagram of Nuclear Spectroscopy system

Each particle interact with the detector produces voltage pulse. This voltage pulse is in millivolt (mV). This pulse is transfer into preamplifier to amplify the signal and reduces sources of noise. Then amplified signal goes to the analog to digital converter, analog signal is converted into digital signal. Then radiation detection analyzer (e.g. SCA, MCA) is used to analyze the signal and scalar is used record the analyzed pulse [5].

With the rapid development of IC technology, the application of FPGA becomes more and more widely, more than 90% embedded system design engineers of the world are using the FPGA for a wide variety of designs. Field Programmable Gate Arrays (FPGAs) are especially popular for prototyping integrated circuits designs [6].

In this paper, we have proposed a new nuclear spectroscopy analyzers SCMOA and implemented on FPGA. Section II briefly describes the theoretical description of SCMOA and how it is different from the previous nuclear spectroscopy analyzer (SCA and MCA). In Section III we describe the algorithm of the SCMOA with the associated Datapath Unit and Control Unit. Section IV present the schematics, simulation results, device utilization summery and timing report of implemented SCMOA with various units. In Section V results of SCMOA is discussed and compared to MCA and in Section VI concludes the paper.

II. SINGLE CHANNEL MULTIPLE OUTPUT ANALYZER

We have proposed a model for analyzing nuclear spectroscopy signal called Single Channel Multiple Output Analyzer (SCMOA). SCMOA is quite different in functionality from the SCA and MCA. The Single Channel Analyzer (SCA) has only one threshold window, if the signal is lying in the threshold window then it will generate the pulse which will be stored in storage unit called channel [3]. Modified version of SCA is Multiple Channel Analyzer (MCA) [4]. MCA performs the same task with a number of threshold windows. The pulses generated by each threshold window individually are store in various channels counter as shown in figure.2.

In SCMOA, also have multiple windows similar to MCA, but it has only one channel through which data is send to demultiplexer. Demultiplexer will send the pulse to the desirable counter. Figure.3 shows the block diagram of a Single Channel Multiple Output Analyzer (SCMOA).

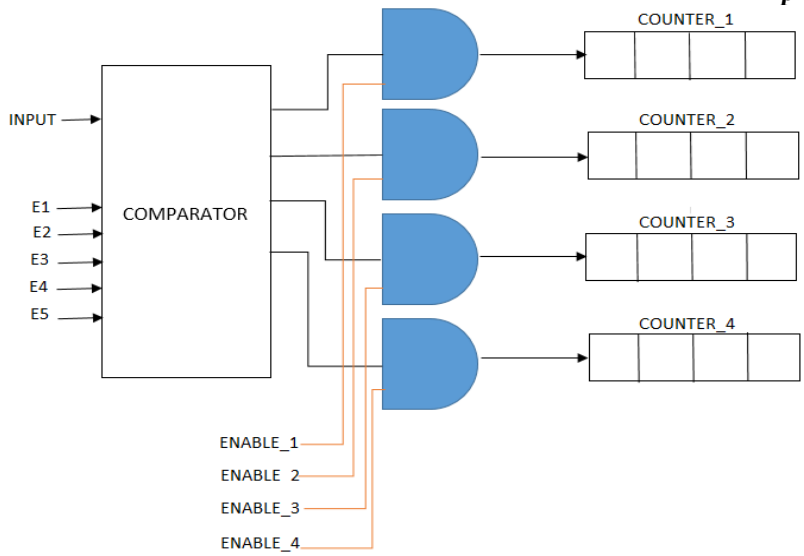

Figure.2: Block diagram of a MCA

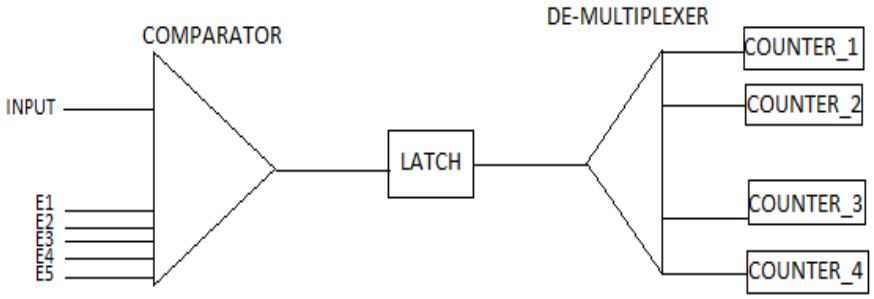

Figure.3: Block diagram of a Single Channel Multiple Output Analyzer

III. FPGAs BASED SCMOA

The detailed theory of Single Channel Multiple Output Analyzer (SCMOA) with suitable diagram is given in section II. In this section, we had manually designed the FPGA based SCMOA for counting the pulse which fall in between the ranges set by predefined energy level. Any digital system have two parts: Datapath unit and Control unit.

A. Algorithm of SCMOA

Following algorithm is used to analyze the data:

i. Analog to Digital Converter (ADC) converts the analog signal into digital signal.
ii. 8-bit data is compared with five predefined threshold value between which data lying and generate result 001,010,011 or 100.
iii. These pulses where transfer to the demultiplexer through latch.
iv. Demultiplexer will transfer the pulse to their respective counter respectively.
v. After counting the pulses by counters will display final results.

B. Components required for FPGAs based SCMOA

After analyzing the algorithm in section III-A, we conclude following functional unit are required for making the Datapath Unit and Control Unit.

i. One 8-bit ADC input unit
ii. One 8-bit comparator unit
iii. One 3-bit latch unit
iv. One 1:4 demultiplexer unit
v. Four 4bit counter unit

C. Datapath Unit of SCMOA

Schematic of component used in Datapath Unit of FPGAs based SCMOA is shown in figure.4. It have all the unit required for implementation of algorithm mentioned in subsection III-A. Datapath Unit of SCMOA consist of one 8-bit ADC Input Unit (UA) which interface ADC and comparator unit (UC), one 8-bit comparator unit (UC), one 3-bit latch unit (UL), one 1:4 demultiplexer unit (UD) and four 4bit counter unit (U01,U02,U03,U04).

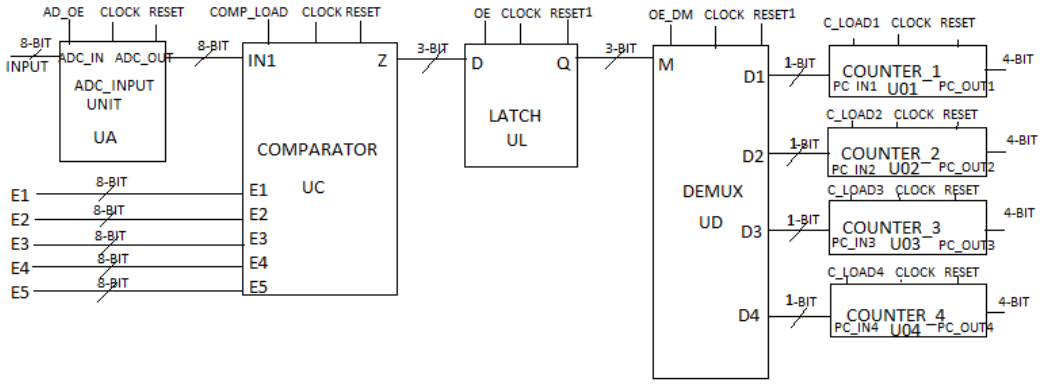

Figure.4: Schematic of component used in Datapath Unit of FPGAs based SCMOA

D. Control Unit of SCMOA

Finite State Machine (FSM) technique is used in control unit FPGAs based SCMOA. It had 7 states: ST0, ST1, ST2, ST3, ST4, ST5 and ST6.in these states various operations are performed such as comparison of data with predefined levels, generation of signals and pulses and counting. The State diagram for Control Unit of FPGAs based SCMOA is shown in figure.3.

i. During the state ST0, initialize the operations to be performed. Reset the system so that output of every unit must be zero.
ii. During the state ST1, asserting signal ADC_OE is high to enable ADC Input Unit for accepting data from the ADC.
iii. During the state ST2, asserting signal COMP_LOAD is high to enable comparator for accepting data from ADC and pass to comparator. Then the input data is compared with the predefined input and produce output.
iv. During the state ST3, asserting signal OE is high to enable latch for accepting data from output of comparator and transfer to the demultiplexer.
v. During the state ST4, asserting signal OE_DM is high to enable demultiplexer for accepting data from output of latch. Demultiplexer will transfer data to their respective counter.
vi. During the state ST5, asserting signal C_LOAD1, C_LOAD2, C_LOAD3 and C_LOAD4 is high to enable counter units for accepting data from demultiplexer.
vii. During the state ST6, reset latch and demultiplexer to make their previous output zero.
After ST6, transfer control signal to state ST1, unconditionally.

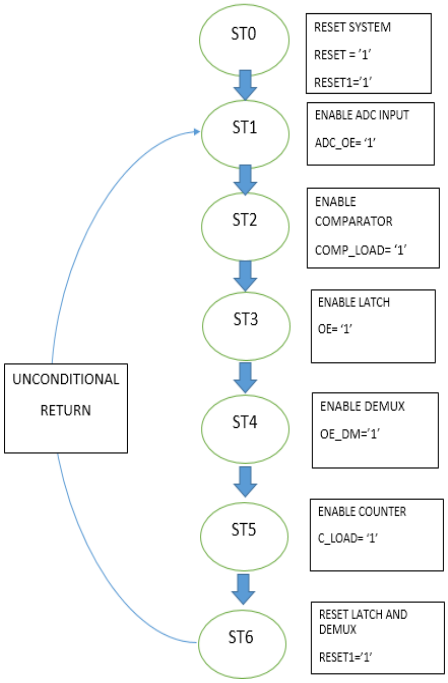

Figure.5: State diagram for Control Unit of FPGAs based SCMOA

IV. SIMULATION AND VERIFICATION

All the units of related to SCMOA is mentioned in section III with proper design and algorithm. These units: Datapath unit and control unit is designed by writing program in Very High Speed Integrated Circuit Hardware Description Language (VHDL). The functionality of each unit is verified by using Modelsim SE 6.5 simulator. SCMOA is synthesized by using synthesis tools provided in Xilinx ISE Webpack 13.4.

A. Datapath unit

The schematic of datapath unit is shown in figure.6 and 7. Table 2 represent device utilization summary report of datapath unit that estimate utilization of device during designing process. Table 3 represent the timing summary report of datapath unit. The maximum operational frequency of designed datapath unit is 121.536MHz.

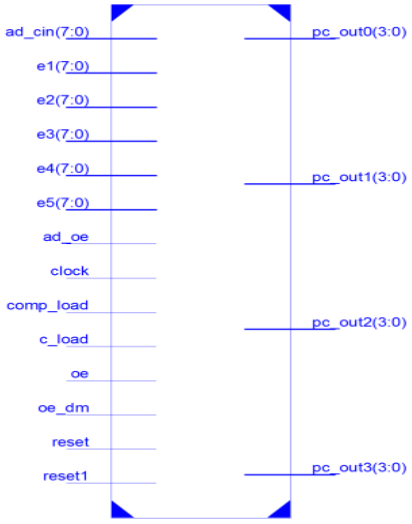

Figure.6: Schematic of Datapath Unit

Table 1 Device Utilization Summary Report Of Datapath Unit Of Fpga Based Scmoa

Selected Device: "3s400pq208-4".			
Number of Slice Flip Flops:	34 out of	7,168	1%
Number of 4 input LUTs:	66 out of	7,168	1%
Number of occupied Slices:	45 out of	3,584	1%
Total Number of 4 input LUTs:	66 out of	7,168	1%
Number of bonded IOBs:	72 out of	141	51%
Number of BUFGMUXs:	1 out of	8	12%

Table 2 Timing Summary Report Of Datapath Unit Of Fpga Based Scmoa

Speed Grade: -4
Minimum period: 8.228ns (Maximum Frequency: 121.536MHz)
Minimum input arrival time before clock: 8.353ns
Maximum output required time after clock: 7.285ns
Maximum combinational path delay: No path found

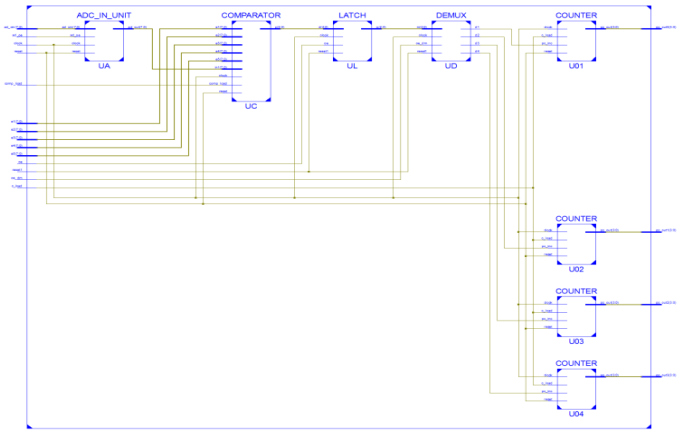

Figure7. Schematic of component used in Datapath Unit

B. Control Unit

The schematic of control unit is shown in figure.6. Table 4 represent device utilization summary report of control unit that estimate utilization of device during designing process. Table 5 represent the timing summary report of control unit. The maximum operational frequency of designed control unit is 382.555MHz.

Table 3 Device Utilization Summary Report Of Control Unit Of Fpga Based Scmoa

Selected Device:"3s400tq144-4".			
Number of Slice Flip Flops:	7 out of	7,168	1%
Number of 4 input LUTs:	4 out of	7,168	1%
Number of occupied Slices:	6 out of	3,584	1%
Total Number of 4 input LUTs:	4 out of	7,168	1%
Number of bonded IOBs:	52 out of	97	53%
Number of BUFGMUXs:	1 out of	8	12%

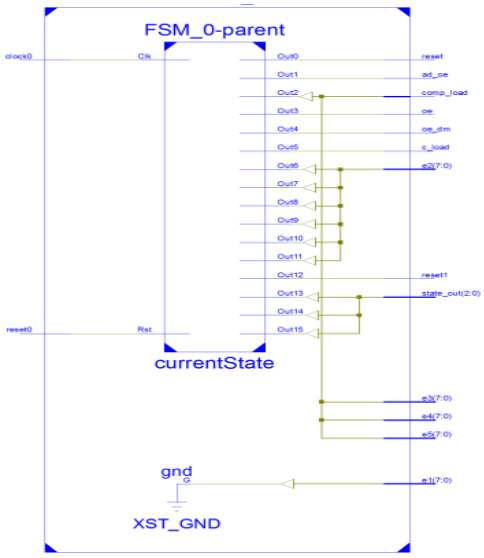

Figure.8: Schematic of Control Unit

Table 4 Timing Summary Report of Control Unit of Fpga Based Scmoa

Speed Grade: -4

Minimum period: 2.614ns (Maximum Frequency: 382.555MHz)

Minimum input arrival time before clock: No path found

Maximum output required time after clock: 9.243ns

Maximum combinational path delay: No path found

C. FPGAs Based SCMOA Unit

The schematic of FPGAs based SCMOA unit is shown in figure.9. Table 6 represent device utilization summary report of FPGAs based SCMOA unit that estimate utilization of device during designing process. Table 7 represent the timing summary report of FPGAs based SCMOA unit. The maximum operational frequency of designed FPGAs based SCMOA unit is 121.536MHz.

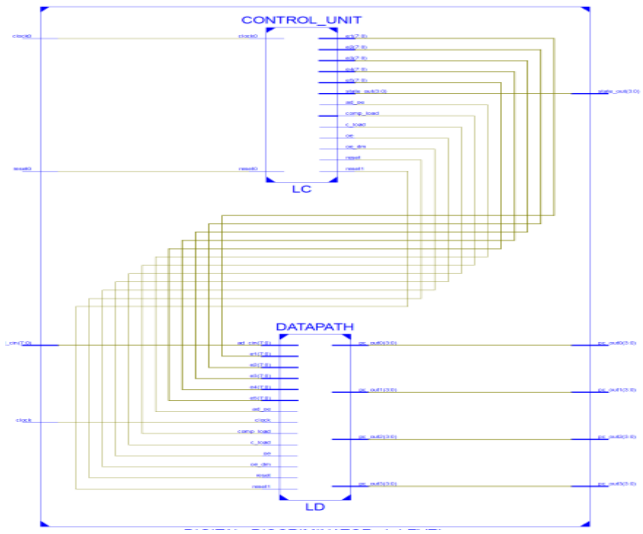

Figure.9: Schematic of FPGAs based SCMOA

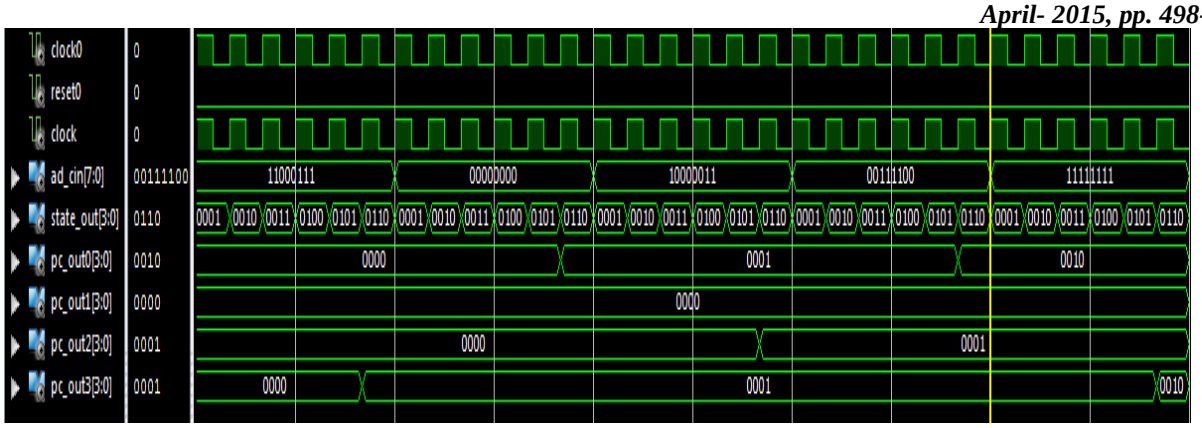

Figure.10. Simulation result of FPGAs based SCMOA

Table 5 Device Utilization Summary Report of Fpga Based Scmoa

Selected Device:"3s400pq208-4".			
Number of Slice Flip Flops:	41 out of	7,168	1%
Number of 4 input LUTs:	70 out of	7,168	1%
Number of occupied Slices:	47 out of	3,584	1%
Total Number of 4 input LUTs:	70 out of	7,168	1%
Number of bonded IOBs:	30 out of	141	21%
Number of BUFGMUXs:	2 out of	8	25%

Table 6 Timing Summary Report Of Fpga Based Scmoa

Speed Grade: -4
- Minimum period: 8.228ns (Maximum Frequency: 121.536MHz)
- Minimum input arrival time before clock: 1.825ns
- Maximum output required time after clock: 9.243ns
- Maximum combinational path delay: No path found

V. RESULTs AND DISCUSSION

In this paper we discussed the proposed model Single Channel Multiple Output Analyzer design (SCMOA) simulation and implementation. Designed SCMOA is made of Control Unit and Datapath Unit. Complete circuit is designed by using VHDL and verified in ModelSim SE 6.5 simulator. SCMOA is implemented on Xilinx Sparton-3 xc3s400-4pq208. Datapath Unit of SCMOA consist of one 8-bit ADC input unit, one 8-bit comparator unit, one 3-bit latch unit, one 1:4 demultiplexer unit and four 4bit counter unit. It maximum operational frequency 121.536MHz. 51 Slices out of 3,584 and 41 Slice Flip Flops out of 7,168 were used.

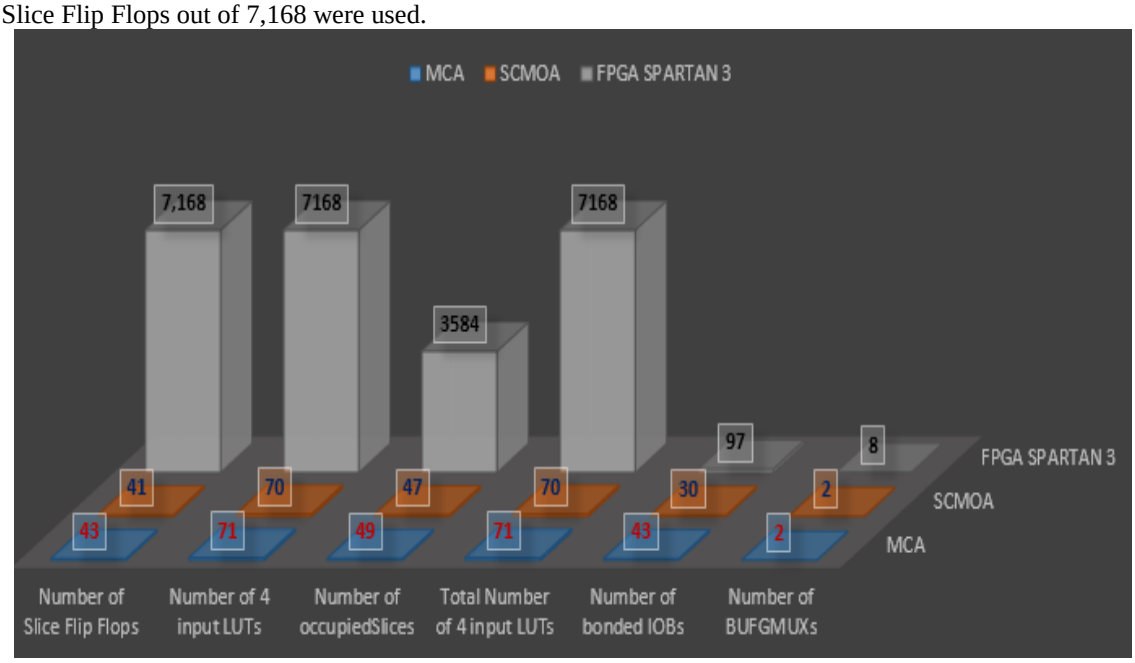

Figure.11: Device utilization summary report of FPGAs based MCA vs SCMOA

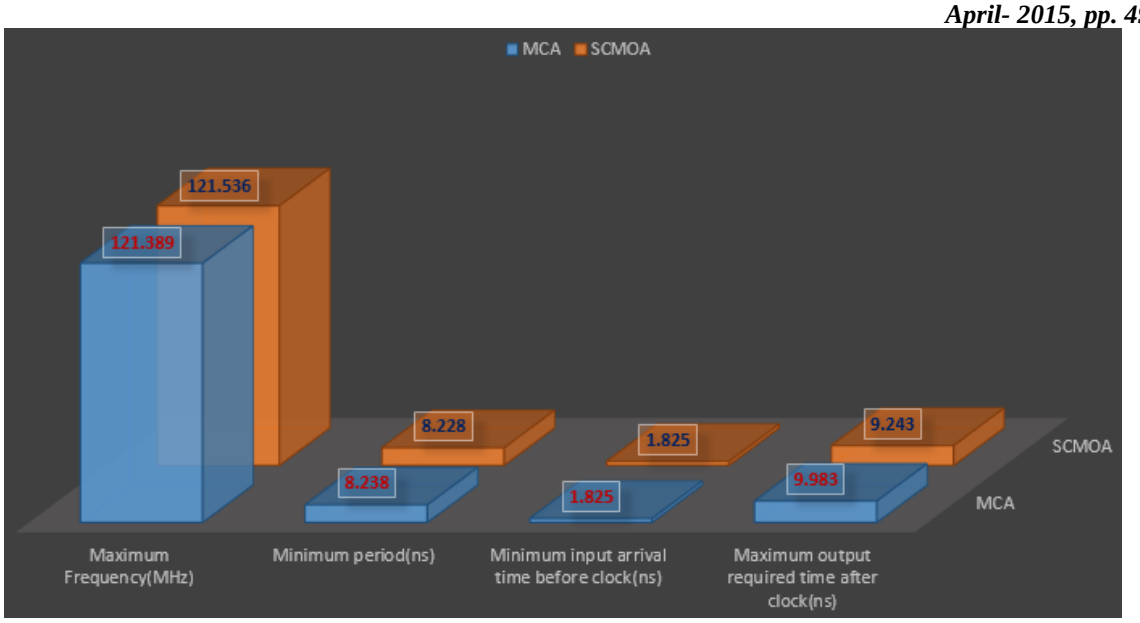

Figure.12: Time summary report of FPGAs based MCA vs SCMOA

Table 7 Device Utilization Summary Report of FPGAS Based MCA VS SCMOA

	MCA	SCMOA	FPGA SPARTAN 3
Number of Slice Flip Flops	43	41	7,168
Number of 4 input LUTs	71	70	7168
Number of occupied Slices	49	47	3584
Total Number of 4 input LUTs	71	70	7168
Number of bonded IOBs	43	30	97
Number of BUFGMUXs	2	2	8

Table 8 Time Summary Report of FPGAS Based MCA VS SCMOA

	MCA	SCMOA
Maximum Frequency(MHz)	121.389	121.536
Minimum period(ns)	8.238	8.228
Minimum input arrival time before clock(ns)	1.825	1.825
Maximum output required time after clock(ns)	9.983	9.243

VI. CONCLUSIONS

In this paper, we have improved the analyzer circuit used in the nuclear spectroscopy. The proposed model, single channel multiple output analyzer (SCMOA) is showing better performance than the traditional multi channel analyzer (MCA) circuit. It is using less component than MCA and cost is also reduced.

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