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A Comparitive Study of Binary Multiplier for The Efficient Implementation of Linear Convolution Using FPGA

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Abstract: Convolution is a mathematical way of combining two signals to form a third signalWhile convolving the two signals, multipliers are the most important and main component and generally they are the slowest component. Therefore we need to choose such multiplier which process faster than the other and will consume less area and power. Here in this paper we are designing the binary multiplier using Peasent algorithm on FPGA & comparing the results with Vedic multiplier for the efficient implementation of convolution which consumes less power ,require less area& good speed as compared with vedic multiplier.

Keywords: Linear Convolution, Binary multiplier, Peasent Algorithm,Vedic Multiplier,FPGA.

I. INTRODUCTION

Convolution is a powerful mathematical tool for the analysis of Linear time invariant system which operates on two signals or functions f & g to produce third function .The output produced is typically viewed as a modified version of one of the two original functions, giving the area overlap between the two functionsas a function of the amount that one of the original functions is translated.Many approaches have been attempted to reduce the convolution processing time using hardware andsoftware algorithms. But they are restricted to specific applications.This paper presentsthe methodology of reducing convolution processing time using hardware computing and implementations of discrete linear convolution of two finite length sequences .This implementation method is realized by simplifying the convolution building blocks.Multipliers are key components of many high performance systems such as FIR filters, microprocessors, digital signal processors, etc. Asystem's performance is generally determined by the performance of the multiplier because the multiplier is generally the slowest element in the system. Furthermore, it is generally the most area consuming. Hence, optimizing the speed and area of the multiplier is a major design issue. However, area and speed are usually conflicting constraints so that improving speed results mostly in larger areas. The purpose of this analysis is to prove the feasibility of an FPGA that performs a convolution of two aperiodic signals specially unsigned bits.The heart of system is the design of Binary multiplier. Here we have designed a binary multiplier using the Russian peasant algorithm which solves the problem of multiplication by quick multiplication of multiplicand & multiplier which is relatively quick & simpler than any other algorithm. The idea is to double the first number and halve the second number repeatedly till the second number doesn't become 1. In the process, whenever the second number become odd, we add the first number to result (result is initialized as 0).The same is implemented in VHDL .Thereby performing a comparative analysis with Vedic multiplier .The proposed implementation uses a change hierarchical design approach, which efficiently and accurately quickens computation; reduces power, hardware resources, and area considerably. The efficiency of the proposed convolution circuit is tested by embedding it during a prime level FPGA. In addition, the presented circuit uses less power.

This paper is organized as follows. Section II investigates the related convolution algorithm implementation. In section III, circuit implementations are presented. Section IV presents the verification of the proposed design. In section V, evaluation and comparison of the design are presented. Finally, the conclusion is obtained.

II. RELATED WORK

Low power consumption and smaller area are some of the most important criteria for the fabrication of DSP systems and high performance systems. Optimizing the speed and area of the multiplier is a major design issue. However, area and speed are usually conflicting constraints so that improving speed results mostly in larger areas. Here we try to determine the best solution to this problem by comparing a the multipliers by Peasent algorithm & Vedic Algorithm.Some approaches are listed below:

1.Existing digit serial multipliers have been Plagued by complicated switching systems and/or irregularities in design. Radix 2^n multipliers which operate on digits in a parallel fashion instead of bits bring the pipelining to the digit level and avoid most of'the above problems. They were introduced by M. K. Ibrahim in 1993. These structures are iterative and modular.

2. Presented a design for fast convolve for CDMA signals. This is based on avoiding complex operations such as FFT based convolves. They used substitution of the FFT for a Walsh which reduces the operations three times[2] because it uses only real additions but it requires more hardware like counters and RAM blocks which increases activity factor.The

pipelining done at the digit level brings the benefit of constant operation speed irrespective of the size of' the multiplier. The clock speed is only determined by the digit size which is already fixed before the design is implemented.

3. The main problem in implementing and computing convolution is speed, area and power which affect any DSP system. Speeding up convolution using a Hardware Description Language for design entry notonly increases (improves) the level of abstraction, but also opens new possibilities for using programmable devices [3].

4. Today, most DSPs suffer from limitations in available address space, or the ability to interface withsurrounding systems. The use of high speed FPGAs[5], together with DSPs, can often increase thesystem bandwidth, by providing additional functionality to the general purpose DSP.

III. PROPOSED WORK

Two four bit unsigned Input signals are selected, and the implementation for 4x4 was prepared in order to have short convolutions that will lead to the lowest implementation cost. The circuit deals with two signals having N values each. We selected N=4 in our implementations. We consider the two numbers like two arrays having four locations each to store values. Each array is fed into a quadruple 4X1 Mux separately. Hence we can have each signal value up to 4 bit. The selection of values is done by selection switches of each Mux. The selected values go into the Array Multiplier and from there they are routed into Parallel Load Registers through a 1X8 Demux. Afterwards the stored values are added to get the convolved Result [4]. The block diagram of the circuit is shown in figure 3.1.[1]

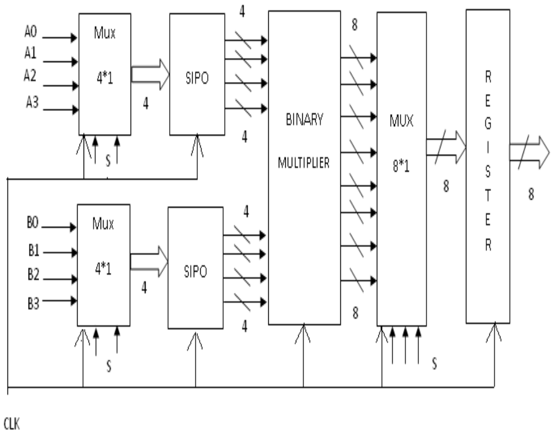
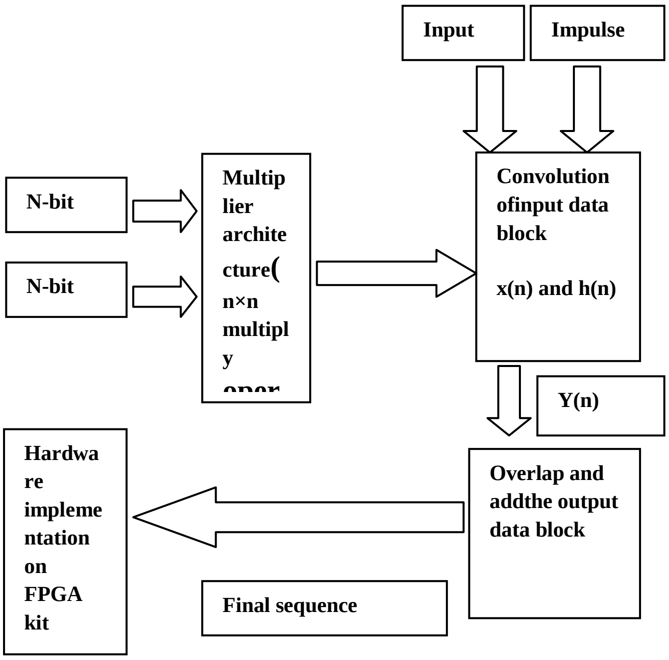


Fig.3.1 Proposed Block Diagram of Convolution Process.


Input
Impulse
N-bit
N-bit
Multiplier architecture(n×n multiply oper
Convolution ofinput data block
x(n) and h(n)
Y(n)
Overlap and addthe output data block
Hardware implementation on FPGA kit
Final sequence

Components used in convolution process

[A] MULTIPLEXER 4:1 & 8:1

A multiplexer is a device that selects one of several analog or digital input signals and forwards the selected input into a single line. A multiplexer of 2^n inputs has n select lines, which are used to select which input lines to send to the output. Multiplexers are mainly used to increase the amount of data that can be sent over the network within a certain amount of time and bandwidth. A multiplexer is also called a data selector.

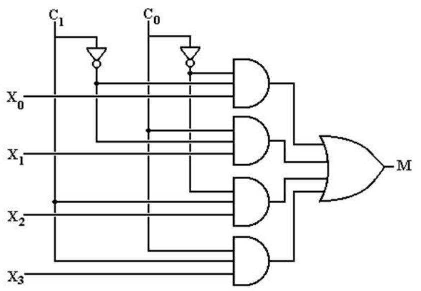


Fig.3.2 Mux 4:1

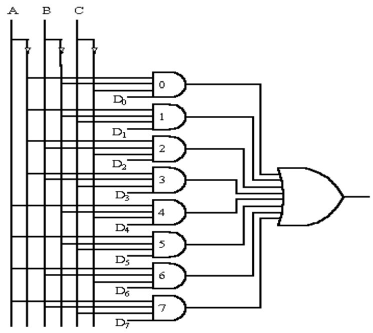


Fig.3.2 Mux 8:1

[B] SIPO

A shift register is a cascade of flip flops sharing the same clock, in which the output of each flip-flop is connected to the data input of the next flip-flop in the chain, resulting in a circuit that shifts by one position the bit array stored in it, shifting in the data present at its input and shifting out the last bit in the array, at each transition of the clock input. In digital circuits, a shift register is a cascade of flip flops, sharing the same clock, in which the output of each flip-flop is connected to the "data" input of the next flip-flop in the chain, resulting in a circuit that shifts by one position the bit array stored in it, shifting in the data present at its input and shifting out the last bit in the array, at each transition of the clock input.shift register.

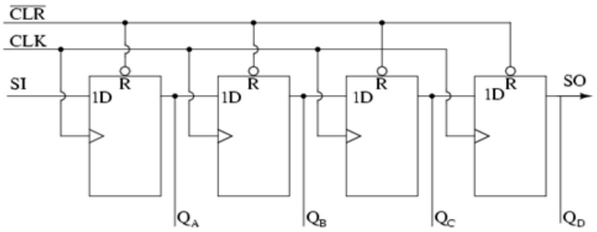


Fig.3.4.Serial in parallel out shift Register Details

[C] BINARY MULTIPLIER.

Binary multiplier we have studied by using Vedic Algorithm & Peasant Algorithm .

i) Peasent Algorithm

The multiplication algorithm discussed is commonly known as the *Russian Peasant Multiplication.* The algorithm in fact may have Egyptian roots. It is introduced as the *Ethiopian (Peasant) Multiplicatio*n)A high speed processor depends greatly on the multiplier as it is one of the key hardware blocks in most digital signal processing systems as well as in general processors. The most significant aspect of the proposed method is that, the developed multiplier architecture is based on peasant algorithm of Russian Mathematics. It generates all partial products and their sum in less time. This also gives chances for modular design where smaller block can be used to design the bigger one. So the design complexity gets reduced for inputs of larger no of bits and modularity gets increased.

The proposed Peasant multiplier is coded in VHDL (Very High Speed Integrated Circuits Hardware Description Language), synthesized and simulated using FPGA. Finally the results are compared with Conventional multipliers to show the significant improvement in its efficiency in terms of speed .The high speed processor requires high speed multipliers and the peasant Multiplication technique is very much suitable for this purpose.

The use of peasant algorithm mathematics lies in the fact that it reduces the typical calculations in conventional mathematics to very simple one. This is so because the peasant algorithm based on the natural principles on which the human mind works. Peasant Mathematics is a methodology of arithmetic rules that allow more efficient speed implementation. It also provides some effective algorithms which can be applied to various branches of engineering such as computing.

The algorithm Steps followed are as follows:

1] Make two column and write the two number you want to multiply.

2] Divide the first number by two till you get one and ignore the remainder.

3] Multiply the second number by two until there are the same amount of number as there in first column

Example of Peasant algorithm

The Russian peasant multiplication, also called the Russian peasant algorithm, uses a halving and doubling method to multiply whole numbers I will illustrate the method with two good examples that you should study carefully .When halving, disregard any remainder Just put the quotient in the halving column when the number in the halving column is 1, cross out all rows that have an even number in the halving column the answer is found by adding the remaining numbers in the doubling column

For example, to multiply 238 by 13:-

STEP 1:- the smaller of the numbers, to reduce the number of steps, 13, is written on the left and the larger on the right.

STEP 2:- The left number is progressively halved (discarding any remainder) and the right one doubled, until the left number is 1:

13		**238**
6	(remainder discarded)	**476**
3		**952**
1	(remainder discarded)	**1904**

STEP3 :-Lines with even numbers on the left column are struck out, and the remaining numbers on the right are added, giving the answer as 3094:

13	**238**
6	476
3	**952**
1	+ **1904**
	3094

The algorithm can be illustrated with the binary representation of the numbers:

1101	**(13)**	**11101110**	**(238)**
110	(6)	**11101110**0	(476)
11	**(3)**	**11101110**00	**(952)**
1	**(1)**	**11101110**000	**(1904)**

1 1 1 0 1 1 1 0 (238)

× **1 1 0 1 (13)**

1 1 1 0 1 1 1 0 (238)

0 0 0 0 0 0 0 0 0 **(0)**

1 1 1 0 1 1 1 0 0 0 **(952)**

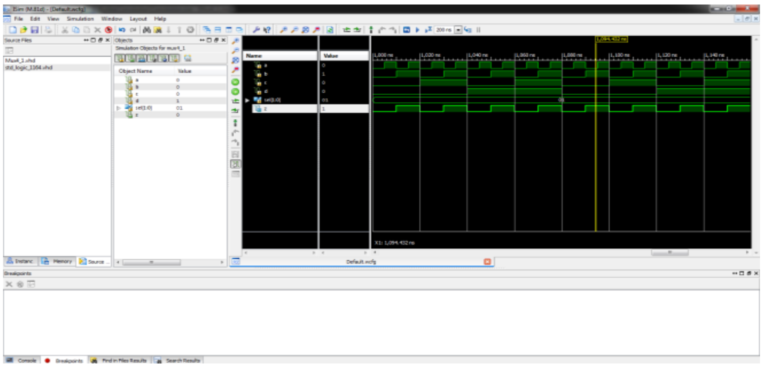
+ **1 1 1 0 1 1 1 0** 0 0 0 **(1904)**

1 1 0 0 0 0 0 1 0 1 1 0 (3094)

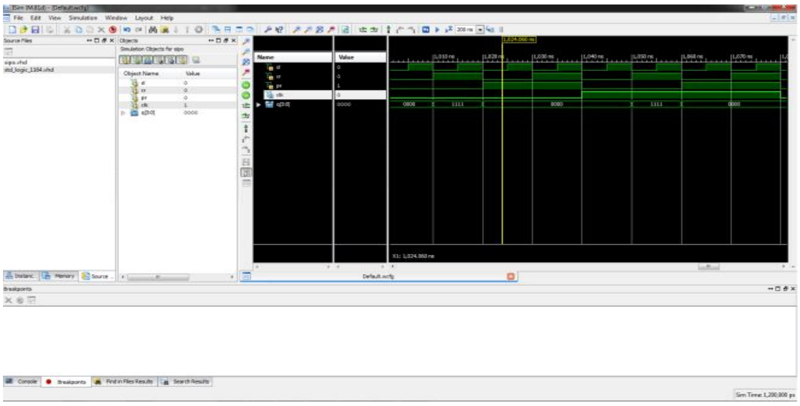
[D]SIMULATION RESULT & CONCLUSION:

The proposed different building blocks of convolution i.e .Mux 4:1,Mux 8:1, SIPO,Register & Binary multiplier using Peasant algorithm is coded in VHDL (Very High Speed Integrated Circuits Hardware Description Language), synthesized and simulated using FPGA. Finally the results are compared with Conventional multipliers e.g. Vedic multiplier to show the significant improvement in its efficiency in terms of speed .The high speed processor requires high speed multipliers and the peasant Multiplication technique is very much suitable for this purpose.Below are shown the simulation results .

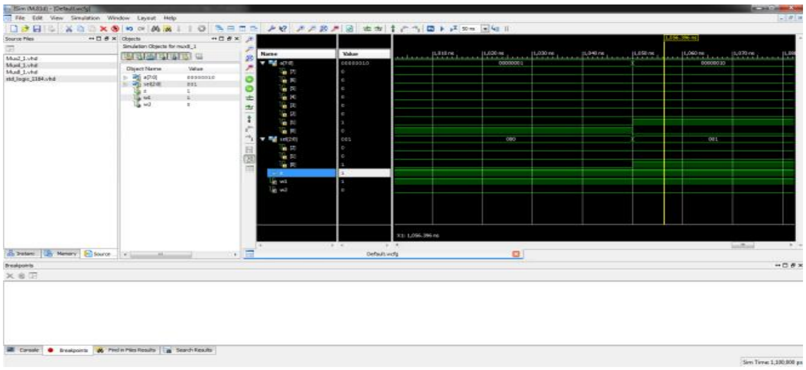
MUX 4:1



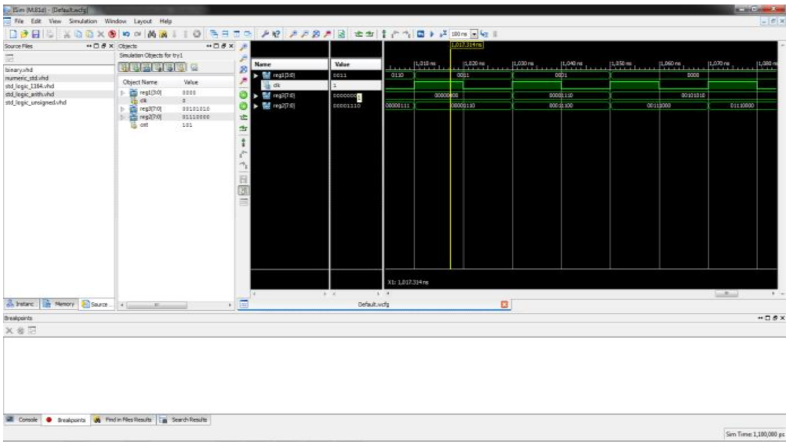
SIPO



REGISTER



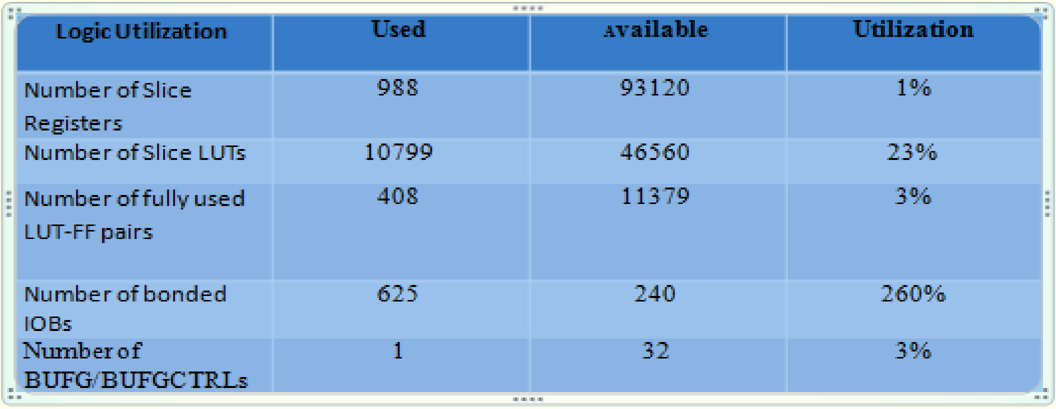
BINARY MULTIPLER USING PEASENT ALGORITHM



Comparison between Vedic multiplier and Peasant multiplier

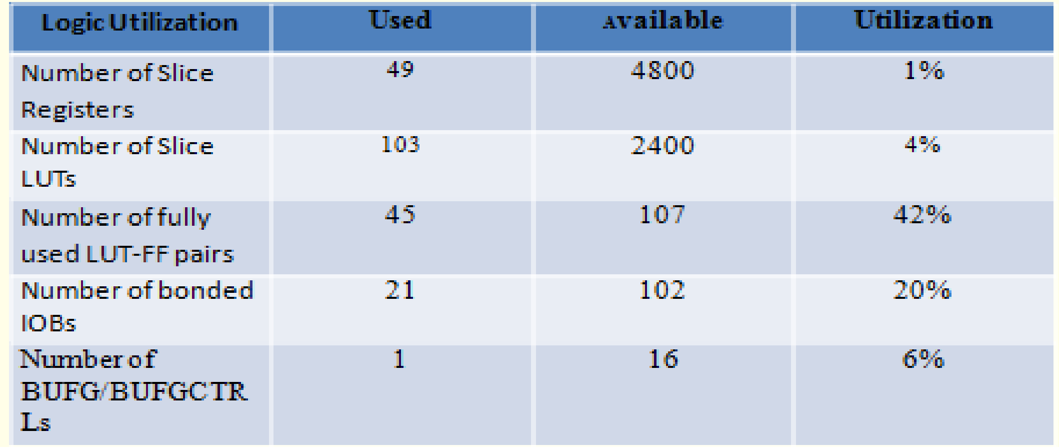
Device utilization summary of

1.Vedic multiplier



Logic Utilization	Used	Available	Utilization
Number of Slice Registers	988	93120	1%
Number of Slice LUTs	10799	46560	23%
Number of fully used LUT-FF pairs	408	11379	3%
Number of bonded IOBs	625	240	260%
Number of BUFG/BUFGCTRLs	1	32	3%

2. Peasant multiplier



Logic Utilization	Used	available	Utilization
Number of Slice Registers	49	4800	1%
Number of Slice LUTs	103	2400	4%
Number of fully used LUT-FF pairs	45	107	42%
Number of bonded IOBs	21	102	20%
Number of BUFG/BUFGCTRLs	1	16	6%

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