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Design and Synthesis of Low Cost Reversible Arithmetic and Logic Unit (ALU)

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Abstract – In low power circuit design, reversible computing has become one of the most efficient and prominent techniques in recent years. In this paper, Low Cost reversible Arithmetic and Logic Unit (ALU) is designed to show its major implications on the Central Processing Unit (CPU). In the proposed design, eight arithmetic and four logical operations are performed. In the proposed design, TSG Full Adder Gate (TSGFAG) is used in reversible ALU design. And proposed design are analysed and compared with the previous published design in terms of number of gates count and garbage output.

Keywords –Reversible Logic Gates, Reversible ALU design, Reversible full adder, Reversible TSG Gate, TSG Full adder Gate (TSGFAG), Proposed Reversible ALU design

I. INTRODUCTION

There are many problems occurs in conventional computing. The major problem in conventional computing is heat dissipation, which is the important issue in today's circuit development [1]. In VLSI design, the conventional logic circuits dissipate more power [2].

In the conventional logic circuits, every bit of information loss will generate kTlog2 joules of heat energy [3]. In the conventional logic circuit design, information loss occurs due to the total number of output signals is less than the total number of input signals applied to the logic circuit. and inputs cannot be generated from the outputs of the conventional circuits [4].

Reversible computing is an alternative method in low power dissipating circuit design for current technologies such as low power (CMOS) design, cryptography, optical information processing, quantum computing and nanotechnology.

Arithmetic and Logic Unit (ALU) is core part of the CPU of any computer architecture. ALU works as a data processing unit. ALU is a multi-functional circuit that performs one of a few possible functions on two operands and which depends on the control inputs [5]. Reversible logic can be implemented in designing ALU to reduce the power dissipation and propagation delay in the circuits [6].

In this paper, a new reversible ALU designs are proposed using TSG reversible full adder logic gate. In the proposed designs, eight arithmetic and four logical operations are performed. The proposed designs are analysed in terms of number of gates count and garbage output.

II. REVERSIBLE LOGIC GATES

A. Feynman Gate

Fig 1 shows a 2*2 Feynman gate [7]. The input vector is I(A, B) and the output vector is O(P,Q), the output vector are defined by P=A, Q= A ⊕ B [5].

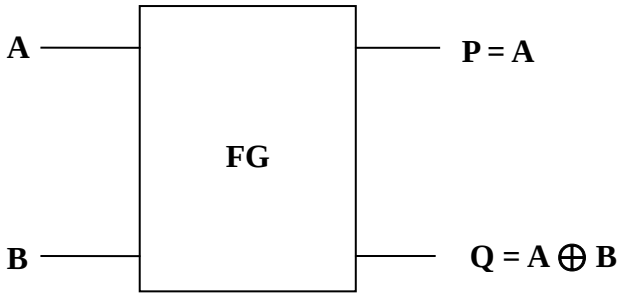

Fig.1 Feynman gate

B. Toffoli Gate

Fig 2 shows a 3*3 Toffoli gate [8][9]. The input vector is I(A, B, C) and the output vector is O(P, Q, R). The outputs are defined by P=A, Q=B, R=AB ⊕ C.

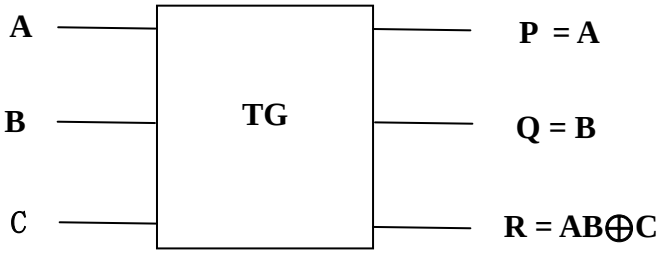

Fig.2 Toffoli gate

C. Peres Gate

Fig 3 shows a 3*3 peres Gate [10]. The input vector is I(A, B, C) and the output vector is O(P, Q, R). The output is defined by P=A, Q= A ⊕ B and R= AB ⊕ C.

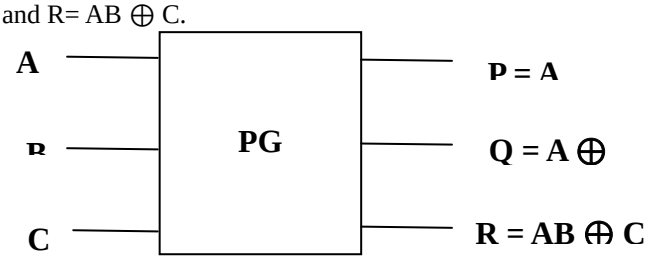

Fig.3 Peres gate

D. Reversible R-I Gate

R-I gate [11] is a reversible of 3*3 gate with three inputs and three outputs. The Fig. 4 shows the R-I reversible gate. The outputs are defined by P=B, Q= $A\bar{B}$ □ □ BC , R= AB□ C.

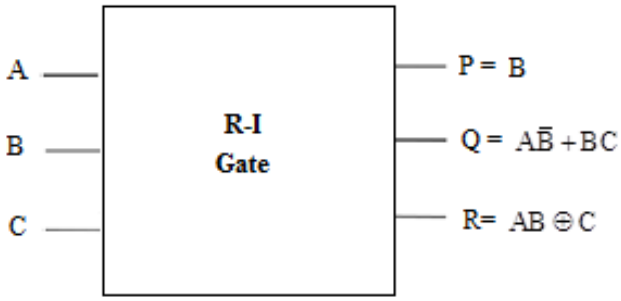

Fig.4 Reversible R-I gate

III. PROPOSED ALU DESIGN

As in previous section it is discussed that ALU works as a data processing components which is an important part in the central process unit (CPU). Besides, it is the main performer in any computing devices. ALU is a multi-functional circuit that performs one of a few possible functions on two operands of A and B which is depending on the control inputs.

A. Reversible ALU

The reversible ALU [11] is designed to produce the same function as conventional ALU. Fig. 5 is the block diagram of reversible ALU designs. It has two main logic circuit design, namely, control unit and reversible full adder and the design has five constants signals (e.g: Cinput1, Cinput2, Cinput3, Cinput4 and Cinput5) for realizing the eight arithmetic operations and four logic operations [11] .

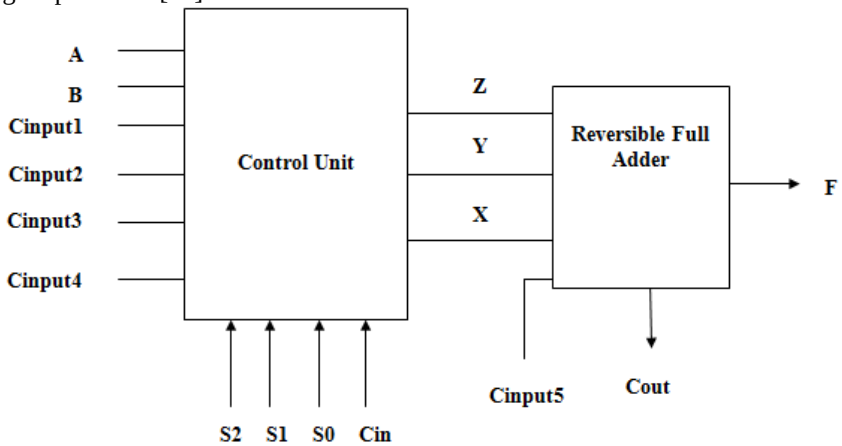

Fig.5 Block diagram of reversible ALU design

1.) Control Unit

Control unit [11] is a critical part in the reversible ALU design. Control unit performs the arithmetic operations inside the ALU. As shown in Fig.6, control unit design is made up from three Feynman gates, three R-I gates and one Fredkin gate. Four control variables S2, S1, S0 and Cin select twelve different operations in the reversible ALU design. The arithmetic and logic operations are differentiated using the variable input of S2. The control unit has four constant signals. There are eight garbage outputs in the proposed control unit logic circuit [11].

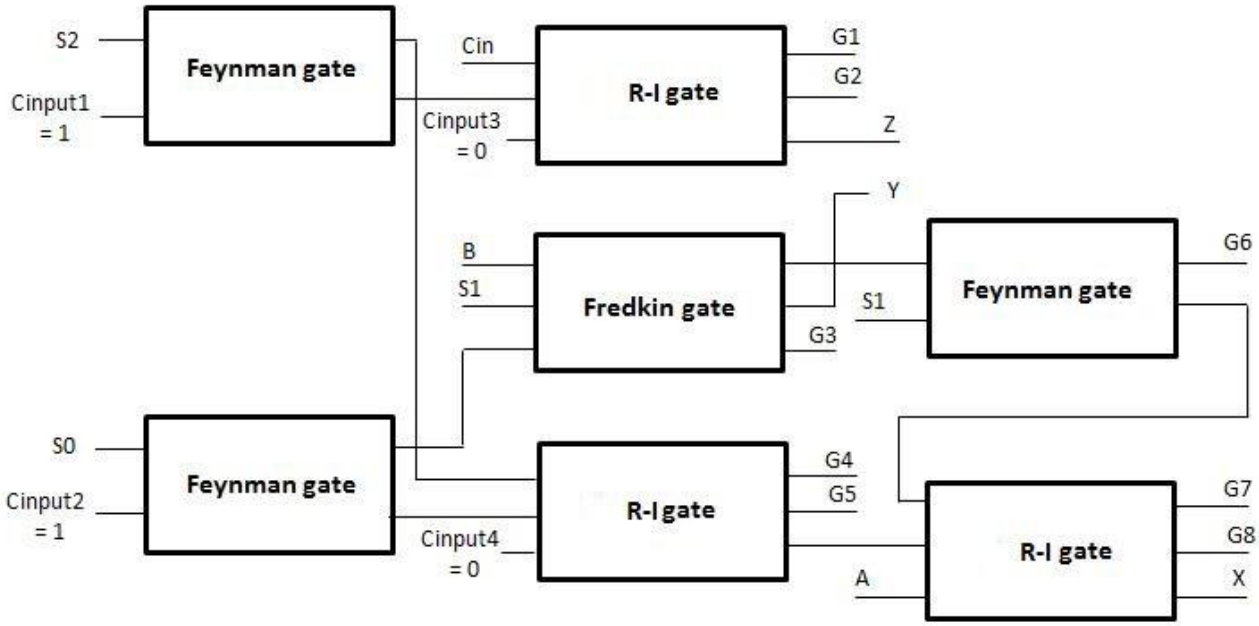

Fig.6 Block diagram of control unit

B. Reversible Full Adder

Full adder is the important building block in ALU unit. In reversible ALU, it is required to add reversible full adder circuit. Compatible reversible adder implementations is required in the anticipated paradigm shift logic compatible with the optical and quantum. The outputs of the reversible adder are given in the following equations:

Sum = A ⊕B ⊕Cin (1)

Cout = (A ⊕B) Cin ⊕AB (2)

C. Reversible TSG Gate

Fig 7 shows a 4*4 TSG gate [12]. The input vector is I (A, B, C, D) and the output vector is O (P, Q, R, S). The output is defined by P = A, Q = A'C' ⊕ B', R = (A'C' ⊕B') ⊕D and S = (A'C' ⊕ B').D ⊕(AB ⊕C)**.** The TSG gate [12] is capable of implementing all Boolean functions and can also work singly as a reversible Full adder as shown in figure

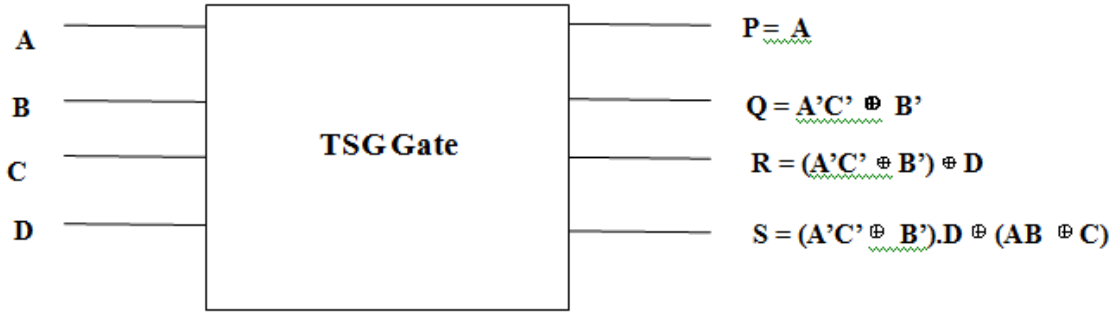

Fig.7 Reversible TSG Gate

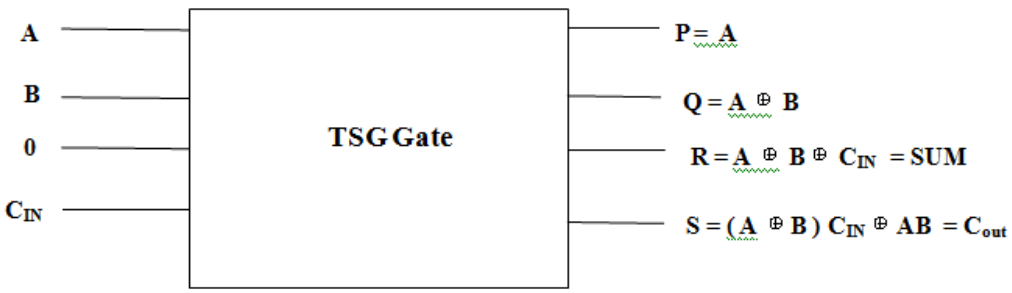

Fig.8 TSG Gate Working As Reversible Full Adder

D. Proposed Reversible ALU Design

Fig 9 shows the proposed Reversible ALU design using control unit and TSGFAG Gate. In which a control unit and a reversible TSG Full adder gate (TSGFAG) is used to design a reversible ALU.

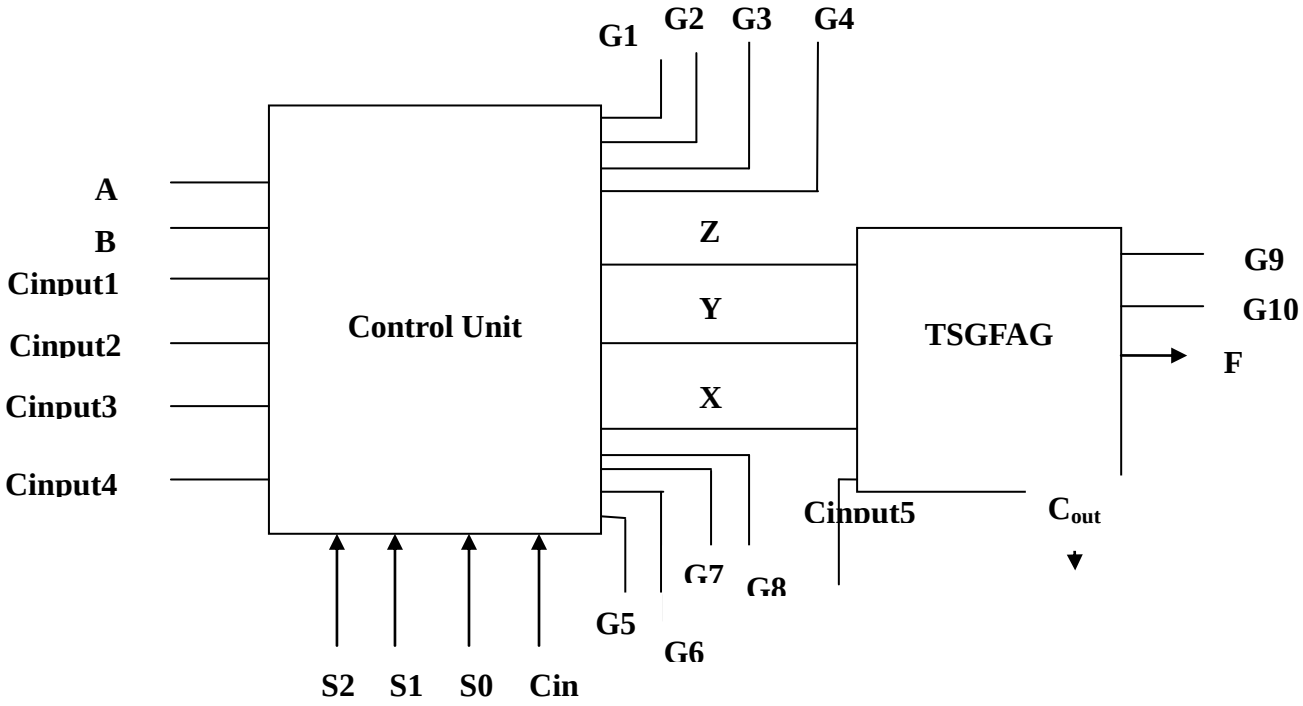

Fig.9 Block diagram of the proposed reversible ALU design.

IV. RESULTS

Table 1 shows the performance comparison of the ALU design (Control Unit + PFAG) published in [11] with the proposed reversible ALU design (Control Unit + TSGFAG). For comparison, number of gate count, garbage output are considered as the performance matrices.

Table I Comparison between proposed reversible ALU design and design published in [11]

ALU DESIGN	Gate Count	Garbage Output
Control Unit + TSGFAG	8	10
Control Unit + PFAG	9	10

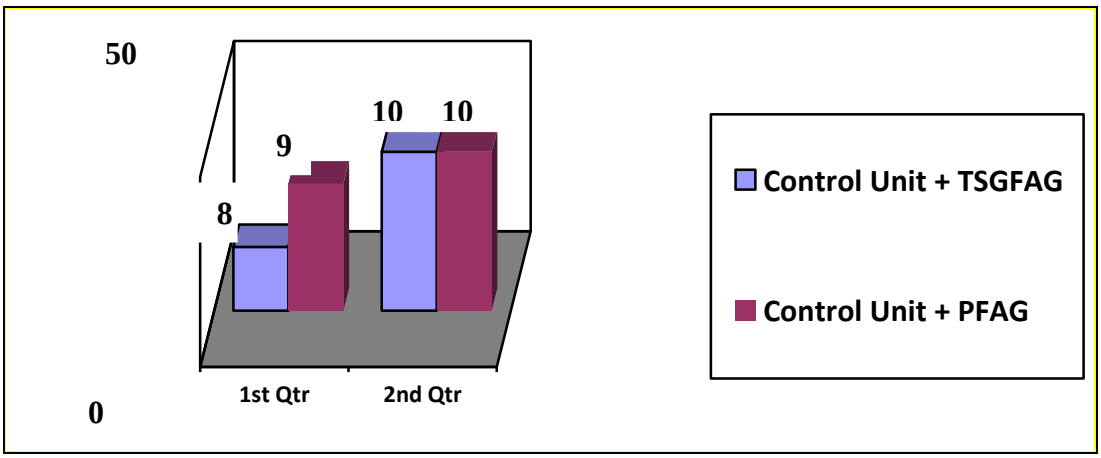

Fig.10 Comparison of proposed reversible ALU design with previous published [11] design based on two parameters

Fig. 10 shows that the proposed reversible ALU design (Control Unit + TSGFAG) is better than the reversible ALU design (Control Unit + PFAG) in terms of performance parameters like Gate Count and Garbage Output.

V. CONCLUSION

In this paper, the reversible ALU design is proposed with Control unit and TSG Full Adder Gate (TSGFAG). The proposed reversible ALU design are verified manually. The proposed design is analysed and compared with previous proposed design in terms of number of gates count, garbage output. The comparison shows that the proposed reversible ALU design outperforms the previous proposed reversible ALU design and conventional ALU design. In future more ALU designs can be proposed using new reversible logic gates based on new performance parameters.

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