



## Review of LP-TPG Using LP-LFSR for Switching Activities

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**Abstract**— *Test pattern generator (TPG) is more suitable for built in self test (BIST) structures used for testing of VLSI circuits. The objective of the BIST is to reduce power consumption, switching time and power dissipation without affecting the fault coverage. Low power linear feedback shift register (LPLFSR) is employed for TPG in order to reduce switching activities. This paper presents multiplier, LFSR, LP-TPG and BIST structure.*

**Index Terms**—*BIST, LFSR, TPG, Switching activity, CUT.*

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### I. INTRODUCTION

In system-on-chips (SoCs) design and test, power dissipation. Generally, power dissipation of a system in test mode is more than in normal mode [9]. This is because a significant correlation exists between consecutive vectors applied during the circuit's normal mode of operation, whereas this may not be necessarily true for applied test vectors in the test mode. Reduced correlation between the consecutive test vectors increases the switching activity and eventually the power dissipation in the circuit. The second reason for the increase in power dissipation during test is because the test engineers may test cores in parallel to reduce the test application time. This extra power (average or peak) can cause problems such as instantaneous power surge that causes circuit damage, difficulty in performance verification and decreased overall product yield and cost.

The main challenging areas in VLSI circuits are cost, performance, reliability, power, testing and area. The demand for portable computing devices and communication system are rapidly increasing. These applications require low power dissipation for VLSI circuits [2]. The ability to design, fabricate and test Application Specific Integrated Circuits (ASICs) as well as FPGAs with gate count of the order of a few tens of millions has led to the development of complex embedded SOC.

The rest of the paper is organized as follows. In Section II, literature survey relevant to power reduction are explained, which mainly concentrated to reduce the average and peak power. In section III, explains multiplier architecture, which is taken here as a circuit under test (CUT) to verify the effectiveness of the technique. In Section IV, the technique in the test pattern generator is described. Section V explains the common algorithm for the LP-LFSR. In section VI, implementation details are explained. At the end reviewed papers are presented and few conclusions are drawn.

### II. LITERATURE SURVEY

For test Pattern generation, Chakrabarty et al. proposed a deterministic built-in test pattern generation using twisted-ring counters (TRC). It embeds a precomputed deterministic test set for the circuit under test (CUT) in a short test sequence produced by TRC. The patterns derived from the seeds are applied testll-pre-clock to the circuit under test. This is a combination of BIST with external slow testers [4]. Y. Zorian et al. proposed a distributed BIST control scheme for complex VLSI circuits in which a generic BIST scheduling process and BIST control architecture is presented. The control architecture provides an autonomous BIST activation and a diagnostic capability to identify failed blocks [1].

Sybille Hellebrand et al. proposed pattern generation for a deterministic BIST scheme in which it targets test-per-scan architecture combining pseudo random and deterministic BIST. The amount of bits to be stored is reduced compared to others by 1-30% [2]. R.S. Katti et al. proposed a multiple output low power LFSR that produces the output of several clock cycles of a serial LFSR at once. This allows for a reduction in the power-supply voltage [7].

V. Kirthi, Dr. G. Mamatha Samson proposed that the LP LFSR architecture is carried by using Vedic Multiplier for the test pattern is faulty or not for better power reduction in BIST [15].

A better low power can be achieved by using single input change pattern generators. It is proposed that the combination of LFSR and scan shift register is used to generate random single input change sequences [3 & 8]. In [8 & 12], it is proposed that  $(2m-1)$  single input change test vectors can be inserted between two adjustment vectors generated by LFSR,  $m$  is length of LFSR. In [8], it is proposed that  $2m$  single input changing data is inserted between two neighbouring seeds. The average and peak power are reduced by using the above techniques. Still, the switching activities will be large when clock frequency is high.

### III. MULTILPLIER ARCHITECHTURE

Multpliers have large area, long latency and consume considerable power. Reduction of power consumption makes a device reliable. Therefore, low power multpliers with high clock frequencies play an important role in today's digital signal processing. Digital signal processing (DSP) is the technology at the heart of the next generation of personal mobile communication systems. Most DSP systems incorporate a multiplication unit to implement algorithms such as convolution and filtering.

Multpliers are classified by the format in which words are accessed namely:

1. Serial multplier
2. Parallel multplier
3. Serial-parallel multplier

1) Serial Multplier: It uses a successive addition algorithm .It has a simple structure because both the operands are entered in a serial form .Therefore the physical circuit requires minimum amount of area and less hardware.

2) Parallel Multplier: Most of the digital systems incorporate a parallel multiplication unit to carry-out high-speed operation due to the operands is entered in parallel which consumes less time.

3) Serial-Parallel Multplier: The serial parallel multplier serves as a good tradeoff between time consuming serial multplier and area consuming parallel multplier .These multpliers are used when there is a demand for both high speed and small area. In a device using serial-parallel multplier, one operand is entered serially and the other is stored in parallel with a fixed number of bits.

From the review the multpliers used for this technique are like array multpliers, booth multpliers, Vedic multpliers and Braun array multpliers.

We reported the ongoing multplier now is array multplier the block diagram of that is given below.

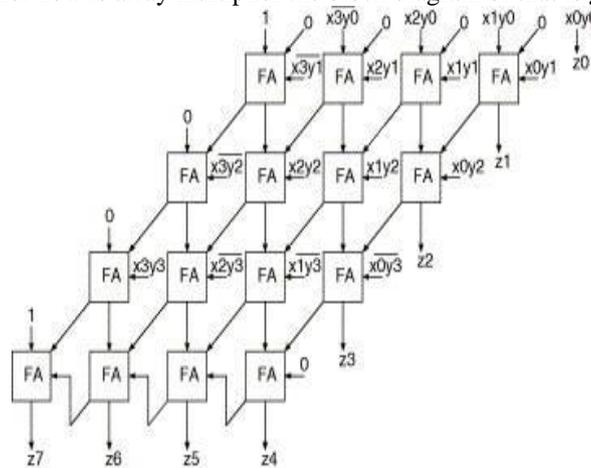


Fig1: array multplier

### IV. LOW POWER TEST PATTERN GENERATION

LP-TPG structure consists of modified low power linear feedback shift register (LPLFSR), m-bit counter; gray counter, NOR-gate structure and XOR-array. The m-bit counter is initialized with Zeros and which generates  $2^m$  test patterns in sequence. The m-bit counter and gray code generator are controlled by common clock signal [CLK].

The output of m-bit counter is applied as input to gray code generator and NOR-gate structure. When all the bits of counter output are Zero, the NOR-gate output is one. Only when the NOR-gate output is one, the clock signal is applied to activate the LP-LFSR which generates the next seed. The seed generated from LP-LFSR is Exclusive-ORed with the data generated from gray code generator. The patterns generated from the Exclusive-OR array are the final output patterns. [13]

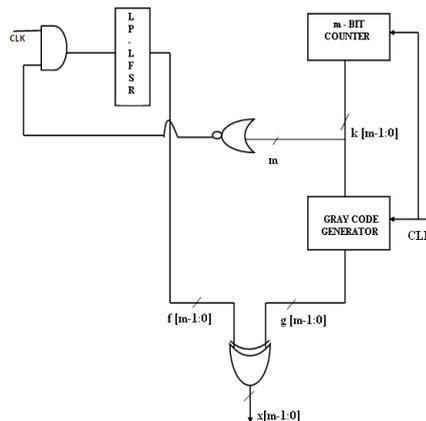


Fig2: LP-TPG



## VI. IMPLEMENTATION DETAILS

The final BIST architecture is [8], [12]. BIST is a design for testability (DFT) technique in which testing is carried out using built-in hardware features. Since testing is built into the hardware, it is faster and efficient. The BIST architecture shown in fig.3 needs three additional hardware blocks such as a pattern generator, a response analyzer and a test controller to a digital circuit. For pattern generators, we can use either a ROM with stored patterns, or a counter or a linear feedback shift register (LFSR). A response analyzer is a compactor with stored responses or an LFSR used as a signature analyzer. A controller provides a control signal to activate all the blocks. BIST has some major drawbacks where architecture is based on the linear feedback shift register[LFSR].The circuit introduces more switching activities in the circuit under test (CUT)during test than that during normal operation[9].It causes excessive power dissipation and results in delay penalty into the design[7].

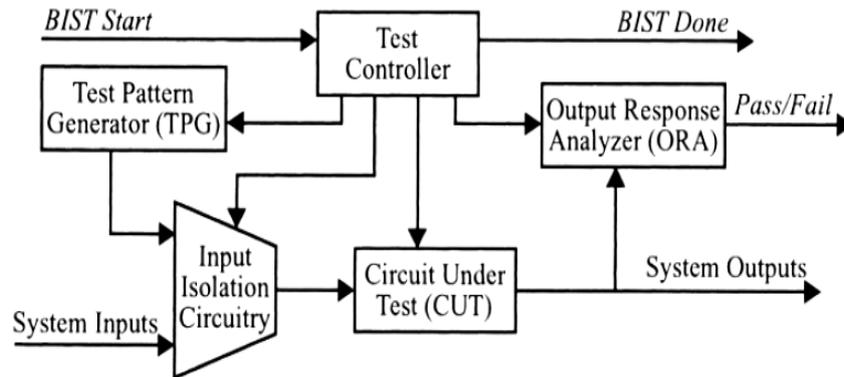


Fig4: BIST architecture

## VII. CONCLUSION AND FUTURE WORK

Using Low power test pattern generator, a circuit's performance can be increased and switching activities can be reduced so that power dissipation will be reduced during test mode. We are going to implement a LP-TPG using diff multiplier techniques so that the power will reduce compared to previous works and also switching rate will be reduced in future.

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