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An Extensive Literature Review on Reversible Logic Gates

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Abstract: Reversible logic is promising as it is able to compute with various applications in very low power like nano-computing for example quantum computing. Reversible circuits are like conventional circuits despite they are build from reversible gates. Reversible circuits, have single, one-to-one mapping between the input and output vectors.Thus all output vectors are permutations of input vectors. A concise review of reversible logic gates basics will be studied. The basic reversible logic gates need to be optimized in reversible logic design and synthesis. Reversible gates need steady inputs for configuration of gate functions and junk outputs that helps in keeping reversibility. Therefore, it is very important to lessen the parameters such as junk bytes, quantum cost and delay in the scheming of reversible circuits. As reversible circuits have tremendous applications in a vairety of emerging technologies such as quantum computing and quantum dot. Consequently this research work would also cover the promising nanotechnologies.

Key Words- Reversible Logic Gates.

I. INTRODUCTION

Reversible logic is a promising computing design paradigm which presents a method for constructing computers that produce no power dissipation. Reversible computing emerged as a result of the application of quantum mechanics principles towards the development of a universal computing machine. Specifically, the fundamentals of reversible computing are based on the relationship between entropy, heat transfer between molecules in a system, the probability of a quantum particle occupying a particular state at any given time, and the quantum electrodynamics between electrons when they are in close proximity. The basic principle of reversible computing is that a bijective device with an identical number of input and output lines will produce a computing environment where the electrodynamics of the system allow for prediction of all future states based on known past states, and the system reaches every possible state, resulting in no heat dissipation.

A circuit is reversible when their is a one-to-one mapping between sets of input and output values. Thus the values of input states can be always reconstructed from the values of output states. Bennett's theorem suggests that every future (binary) technology will have to use a kind of reversible gates in order to lower the power dissipation. They can also used in quantum dots and DNA circuit realization technologies. The input and output vector of an N-input and N-output reversible logic gate or N X N reversible logic gate can be represented as:

$$In = I1, I2, I3, \ldots, IN \quad (1.1)$$
$$On = O1, O2, O3, \ldots, ON \quad (1.2)$$

Here I_n and O_n represents the input and output vectors of a reversible logic gate. The conventional CMOS logic gates are irreversible in nature as the input vectors cannot be created by the output vectors. Thus erasing a bit or loss of information causes $kTln2$ joules of heat energy. However in reversible logic gates there exists a unique one to one mapping between the input and output vectors. An conventional XOR gate can be represented as shown in Fig. 1.1(a), where A,B are the inputs and outputs respectively. In the conventional XOR gate the inputs A, B are mapped to the output as output = A xor B, whereas in the reversible logic, a XOR gate can be represented as shown in Fig. 1.1(b), where X, Y and P, Q are the input and output vectors respectively. Here the mapping between the inputs and outputs can be represented as P = X and Q = Y $\otimes$ X and holds the property of unique input and output vector mapping property of reversibility. The reconstruction of input vectors from the output vectors can be seen in table 1.1(b). The table 1.1(a) shows the input and output vectors for a conventional xor gate. In the table 1.1(a) it can be seen that for the output P = 0 the input vectors are AB = 01, 10, whereas in the table 1.1(b) each output vector corresponds to a unique input vector. Quantum technology is inherently reversible and is one of the most promising technologies for future computing systems. In addition to reversibility, it has powerful properties such as quantum superposition,

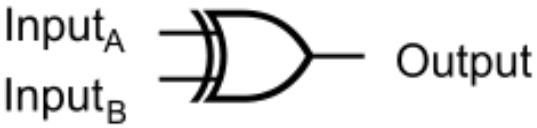


Fig 1.1 (a) Conventional XOR gate

Fig 1.1(b) Reversible XOR gate

Table 1.1(a). Truth table of conventional XOR gates

A	B	Output = A ⊗ B
0	0	0
0	1	1
1	0	1
1	1	0

Table 1.1(b). Truth table of reversible XOR gates

X	Y	P=X	Q=Y ⊗ X
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

quantum parallelism and quantum entanglement that allow for solving problems much more efficiently than in classical computing. For instance, while a classical algorithm needs *N* steps to search an unstructured database, a quantum algorithm proposed by Grover for the same problem needs only $\sqrt{N}$ steps where *N* is the number of elements in the searched unstructured space. It can be proved, moreover that there is no classical algorithm that would require fewer steps than O (N). (Observe that the quantum circuit is reversible when it calculates in Hilbert Space before the measurement. It is no longer reversible after measurement, since the probabilistic measurement cannot be reversed). Although only a few quantum algorithms are known in 2010, many problems can be reduced to some of these algorithms, for instance to the Quantum Fast Fourier Transform or to Grover's algorithm. Thus, any NP-hard problem can be reduced to Grover's algorithm to give a practically useful and substantial reduction in complexity for large values of N. This reduction is, however, not as high as in the case of the exponential speedup obtained by the famous Shor's quantum algorithm for integer factorization.

II. REVERSIBLE LOGIC GATES

In the existing literature, there are several reversible gates such as the Feynman gate and the Fredkin gate. The number of 1x1 and 2x2 reversible gates needed to design a 3x3 reversible gate from 1x1 and 2x2 reversible gates is called the quantum cost of that gate. The quantum cost of all 1x1 and 2x2 reversible gates are considered as unity. The 3x3 reversible gates are generally implemented using the 1x1 NOT gate and 2x2 reversible gates such as Controlled-V and Controlled-V^+ (V is a square-root of NOT gate and V^+ is its hermitian) and the Feynman gate also known as Controlled NOT gate (CNOT). The NOT gate is 1x1 gate represented as shown in Fig. 2.1. Since it is a 1x1 gate, its quantum cost is unity.

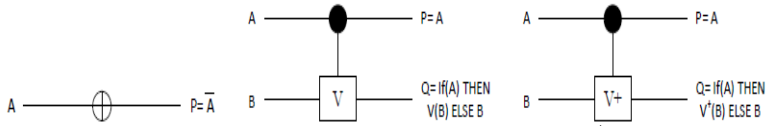


Fig 2.1. NOT, Controlled-V and Controlled-V^+ gates

Controlled-V and Controlled-V^+ gates:-

A controlled-V gate is shown in Fig. 3.1(b). In a controlled-V gate, when the control signal A=0 then the qubit B will pass through the controlled part unchanged, i.e., we will have Q = B. When the value of A=1 then the unitary operation

$$V = \frac{i+1}{2}\begin{pmatrix} 1 & -i \\ -i & 1 \end{pmatrix}$$

is applied to input B, i.e., Q=V(B). The controlled-V + gate is shown in Fig. 3.1(c). In the controlled- V^+ gate when the control signal A=0 then the qubit B will pass through the controlled part unchanged, i.e., we will have Q = B. When A=1 then the unitary operation $V^+ = V - 1$ is applied to the input B, i.e., Q=V^+ (B). The V and V^+ quantum gates have the following properties:

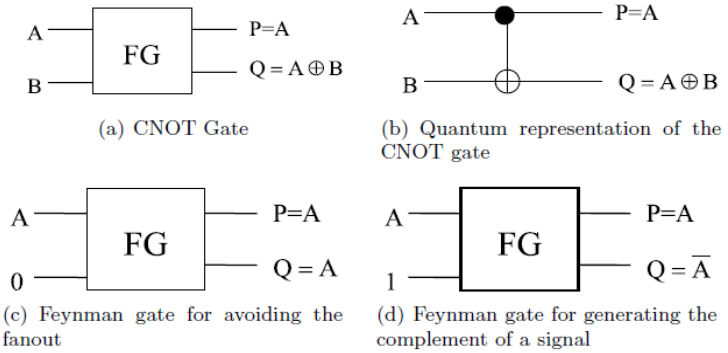
$$V \times V = NOT$$
$$V \times V^+ = V^+ \times V = I$$
$$V^+ \times V^+ = NOT$$

The property as shown above represents that when two V gates are in series they will behave as a NOT gate. Similarly two V^+ gate in series behaves as a NOT gate. A V gate in series with a V^+ gate and vice versa is an identity. The more details of V and V^+ gate can be found.

Feynman Gate (CNOT Gate)

The Feynman gate (FG) or the controlled-NOT gate (CNOT) is a 2-inputs and 2-outputs reversible gate with the mapping (A, B) to (P=A, Q=A⊕B). Here A is the controlling input and B is the controlled input; P, Q is the two outputs. Since the Feynman gate is a 2x2 reversible gate, it has a quantum cost of 1. Figure 2.2(a) and 2.2(b) shows the block diagram and the quantum representation of the Feynman gate.

Fan-out is not allowed in reversible logic. Feynman gate is helpful in this regard as it can be used for copying the signal thus avoiding the fan-out problem as shown in Fig. 2.2(c). It can also be used for generating the complement of a given input signal as shown in Fig. 2.2(d).



(a) CNOT Gate

(b) Quantum representation of the CNOT gate

(c) Feynman gate for avoiding the fanout

(d) Feynman gate for generating the complement of a signal

Fig 2.2. CNOT gate, its quantum implementation and its useful properties

III. LITERATURE REVIEW

Gopal, Lenin; Mohd Mahayadin and Nor Syahira [1] investigated the ALU designed to show its major implications on the Central Processing Unit (CPU).In this paper, two types of reversible ALU designs are proposed and verified using Altera Quartus II software. In the proposed designs, eight arithmetic and four logical operations are performed. In the proposed design 1, Peres Full Adder Gate (PFAG) is used in reversible ALU design and HNG gate is used as an adder logic circuit in the proposed ALU design 2. Both proposed designs are analysed and compared in terms of number of gates count, garbage output, quantum cost and propagation delay. The simulation results show that the proposed reversible ALU design 2 outperforms the proposed reversible ALU design 1 and conventional ALU design.

Kaur, T. and Singh, N.[6], In this research work, the basic concepts of reversible circuits are briefly discussed. Furthermore, an efficient & low cost fault tolerant reversible Arithmetic and logical unit (ALU) is designed and implemented. The results are then compared with the existing design. The large garbage outputs in the proposed design are compensated by the number of operations that it can perform. The Proposed design can perform almost all arithmetic and logical operations on the other hand existing design performs only four operations.

Rakshith, T.R. and Saligram, R. [7] estimated the power dissipation is an important design criterion during the VLSI process flow. Reversible logic is one of the promising fields having a wide range of applications starting from low power VLSI design, fault tolerant circuits, quantum computing to fields such as bio informatics. An ALU may be regarded as the processor's numerical calculator and logical operation evaluator. In this paper a fault tolerant reversible ALU design is proposed. Parity preserving logic gates are the main component in this design. A parity preserving gate is the one in which the parity of the input and the output vectors is the same. The proposed ALU can produce up to 16 logical and 16 arithmetic operations.

Syamala, Y. and Tilak, A.V.N., [8] researched on a function is reversible if each input vector produces a unique output vector. Reversible logic is of growing importance to many future computer technologies. In this paper, the design of a reversible Arithmetic Logic Unit (ALU) is presented making use of multiplexer unit as well as control signals. ALU is one of the most important components of CPU that can be part of a programmable reversible computing device such as a quantum computer. In multiplexer based ALU the operations are performed depending on the selection line. The control unit based ALU is developed with 9n elementary reversible gates for four basic arithmetic logical operations on two n-bit operands. The series of operations are performed on the same line depending on control signals, instead of selecting the desired result by a multiplexer. The later design is found to be advantageous over the former in terms of number of garbage outputs and constant inputs produced.

Morrison, M. and Ranganathan, N. [9] worked on reversible logic that is widely being considered as the potential logic design style for implementation in modern nanotechnology and quantum computing with minimal impact on physical entropy. Recent advances in reversible logic allow for improved quantum computer algorithms and schemes for corresponding computer architectures. Significant contributions have been made in the literature towards the design of reversible logic gate structures and arithmetic units, however, there are not many efforts directed towards the design of reversible ALUs. In this paper, we propose the design of two programmable reversible logic gate structures targeted at ALU implementation and their use in the realization of an efficient reversible ALU is demonstrated. The proposed ALU design is verified and its advantages over the only existing ALU design are quantitatively analyzed.

Morrison, M.; Lewandowski, M. and Meana, R. [10] analyzed the reversible logic is gaining significant consideration as the potential logic design style for implementation in modern nanotechnology and quantum computing with minimal impact on physical entropy. Recent advances in reversible logic allow schemes for computer architectures using improved quantum computer algorithms. Significant contributions have been made in the literature towards the design of

reversible logic gate structures and arithmetic units, however, there are not many efforts directed towards the design of reversible ALUs. In this work, a novel programmable reversible logic gate is presented and verified, and its implementation in the design of a reversible Arithmetic Logic Unit is demonstrated. Then, reversible implementations of ripple-carry, carry-select and Kogge-Stone carry look-ahead adders are analyzed and compared. Next, implementations of the Kogge-Stone adder with sparsity-4, 8 and 16 were designed, verified and compared. The enhanced sparsity-4 Kogge-Stone adder with ripple-carry adders was selected as the best design, and its implemented in the design of a 32-bit arithmetic logic unit is demonstrated.

The problem of a reversible logic structure is that it introduces new metrics for reversible logic design. This structure has high-cost and high-delay of 4*4 reversible logic gates was presented. The proposed method may achieve the good performance of reversible gates in terms of cost, delay and logical output calculations. The gates were implemented in reversible arithmetic logic units in the existing research work. These new ALU designs are advantageous to previously work in synthesis that can favor low delay and high parameter calculation output, which is highly desirable for the realization of a reversible logic processing unit. The area and delay performance of ALU using reversible gates should be as low as possible.

IV. PROPOSED METHODOLOGY

The designing of ALU using reversible gates depends on delay introduced by the architecture of design digital circuits. In this research work we have studied various logic gates in arder to improve the performance of delay of proposed ALU architecture the target board plays very significant role and different target boards introduce different delays in terms of nS. Therefore upgraded board must be selected for getting better system performance.

V. CONCLUSION AND FUTURE SCOPE

The programmable reversible gates have been studied in reversible arithmetic logic units. These new ALU designs are advantageous to previously published work in implementations that favor low delay and high logical calculation output, which is desirable for realization of a reversible central processing unit. The proposed designs can be integrated in the design of a novel reversible arithmetic logic unit. Two highly programmable, low-cost and low-delay 4*4 reversible logic gates has been investigated and studied. The ALU can be verified, and then compared to previous reversible ALU research. The proposed scheme for ALU design would provide a significant improvement in functionality over previously proposed reversible arithmetic logic units.

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