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High Speed Multiplier Using Vedic Mathematics Technique

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Abstract- The demand for the high speed at the time of process which undergoes in less time as fast as possible. A multiplier is needed due to its high speed processing ability. A multiplier is a major source of power dissipation and high delay. The delay can be reduced by using Vedic multiplying techniques .So which technique of Vedic multiplier used in the process so the delay is minimum. In our project we are using 4x4 bit Vedic Multiplier which consist vertical and crosswise methods. This process is done by using Xilinx software. And this process seems to have high performance in terms of speed.

Keywords:- Vedic multiplication, Half Adder, Full Adder, VHDL, hardware design.

I. INTRODUCTION

In the past, the parameters like high speed, small area and low cost where the major areas of concern, whereas power consideration are now gaining the attention of the scientific community associated the VLSI design. With the advance technology demand for high speed and portable digital signal processing system is increased. Multiplier is extensively used in digital signal processing due to its fastest growing technology. Now a day digital signal processing is present in every technical field. DSP helps to do fastest multiplication and addition operations.

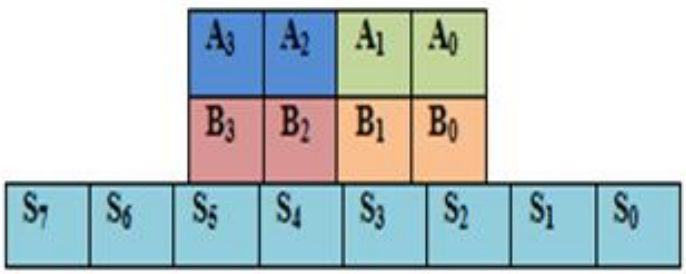
The ancient system of Vedicmathematics was rediscovered from the Vedas between the year 1911 and 1918 by Sri Bharati Krishna Tirthaji. This technique is totally based on 16 sutras in this paper we will discuss the architecture based on Urdhavatiryakbhyamin which vertically and crosswise mathematical operation is performed according to the sutra is presented.the paper presents the basic logic for 4x4 multiplier and the implementation of it with less hardware used.Multiplication having wide application in different areas of engineering technology and in digital systems booths algorithm and array algorithm are the most successful algorithm use for multiplication operations and the other methods include Vedic multipliers based on "urdhvatiryakbhyam".

Digital multipliers are the most commonly used components in any digital circuit design. They are very fast and efficient components that are used to implement. Based upon the arrangement of the modules, there are various types of multipliers exists. Suitable multiplier architecture is chosen for this application.

The Vedic mathematics is very simple, regular as well as logical. Its high degree of eminence is attributed to the aforementioned facts. It is these phenomenal characteristics, which made Vedic mathematics, become so popular and thus it has become one of the leading topics of research not only in India but abroad as well. Vedic mathematics' logics and steps can be directly applied to problems involving trigonometric functions, plane and sphere geometry, differential calculus, integral calculus and applied mathematics of various kind.

II. VEDIC MULTIPLICATION

The proposed Vedic Multiplier is based on"Urdhva Tiryakbhyam"Sutra(algorithm).These Sutra have been traditionally used for the multiplication of two numbers in the decimal number system.In this work,we apply the same ideas to the binary number system to make the proposed algorithm compatible with the digital hardware. Its general multiplication formula applicable to all cases of multiplication. It means vertical and crosswise. It is based on novel concept through which the generation of all partial products can be done with concern addition of this partial products.Multiplier consist of 4 inputs and its resultant output is of 8-bits.If the input is of maximum n-number of bits than its resultant output by multiplication is of maximum 2n-bits.The A3,A2,A1,A0 and B3,B2,B1,B0 are the two inputs taken in 4X4 multiplier.



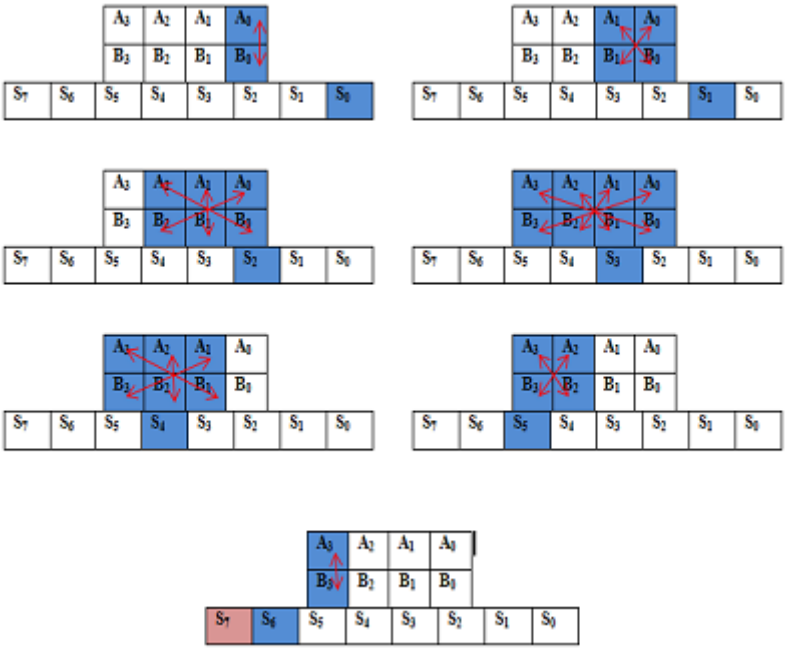


Fig-1. 4 bit Vedic multiplier

THE VEDIC SUTRAS WITH THEIR MEANINGS ARE
LISTED BELOW:
There are 16 Vedic sutras which are listed below with their meanings.
1. (Anurupye) Shunyamanyat –One of them is in ratio then other value is in ratio.
2. ChalanaKalanabyham -Differences and Similarities
3. EkadhikinaPurvena- The value is more than the previous one.
4. EkanyunenaPurvena –The value is less than the previous one.
5. Gunakasamuchyah-The factors of sum is equal to sum of factor.
6. Gunitasamuchyah-the product of sum is equal to sum of product.
7. NikhilamNavatashcaramamDashatah -The value from 9 and last from 10.
8. ParaavartyaYojayet-Transpose and adjust the values.
9. Puranapuranabyham - completion or noncompletion.
10. Sankalana- vyavakalanabhyam -By addition and by subtraction.
11. ShesanyankenaCharamena- The remainders by the last digit.
12. ShunyamSaamyasamuccaye -When the sum is equal then its sum is zero.
13. Sopaantyadvayamantyam -The ultimate and twice the penultimate.
14. Urdhva-tiryakbhyam -It performs vertically and crosswise operations.
15. Vyashtisamanstih -Part and Whole.
16. Yaavadunam- Whatever the extent of its deficiency.

This all are the 16 Vedic sutras. The Vedic multiplication technique is based on one of the sutra named as'Urdhva-tiryakbhyam'.The vertical product of bit A0 & B0 gives the output S0.The sum A0.B0 &A1.B0 gives the output S1 which is 10 bit of its previous sum S0.And the remaining multiplication is done with same method.Theposition of ten's and hundred bit are forward carry to the next addition performed. From the 10's bit S6 the answer of S7 bit will come in the multiplication process.
The multiplication process is shown in figure with different architectures.

III. URDHVA TIRYAKBHYAM SUTRA

Urdhva Triyakabhyam (vertical and crosswise)algorithm can be generalized for n x n bit number. This multiplier has the advantage that has the number increases, gate delay and area increases very slowly as compare to other multiplier. It is very efficient to time space and power .this architecture is demonstrated in the terms of silicon area or speed. Since the partial product .The multiplier has greater advantage that the no. And their sum is calculated in parallel and crosswise method, since the multiplier required same amount of time to calculate the product the multiplier is independent of clock frequency of the processor. By adopting the Vedic Multiplier, structure ,due to its regular structure, It can be easily layout in microprocessors and designers can easily circumvent this power of multiplier it can be easily be increased by increasing the input and output data bus widths since it has quite a regular problems to avoid catastrophic device faliour.The net advantage is that it reduces the need of microprocessor to operate at increasingly high clock frequencies.While at higher clock frequency generally results in increased processing power. Its only disadvantage is that power dissipation increases which result in higher device operating temperature.

IV. ADDER STRUCTURE

In this paper we use four bit full adder to implement the Vedic multiplier.

Four bit full adder-Four bit full adder consist of multiple full adder with carry ins and carry out chains together, where the carry bit ripples from 1 bit to the next bit .All four full adder are internally connected to each other.Whereas each full adder supplied with two inputs.

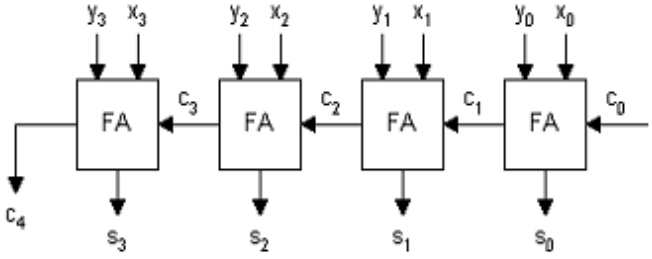


Fig-2. Four bit full adder

The two Boolean functions for the sum and carry are:

SUM = Ai ⊕Bi⊕Ci

Cout= Ci+1 = Ai · Bi + (Ai ⊕Bi) · Ci

Half Adder – A half adder is a logic circuit that performs one-digit addition.It has two inputs (the bits to be summed) and two outputs (the sum bit and the carry bit) and its associates block diagram is as shown. An example of a Boolean half adder is this circuit in figure

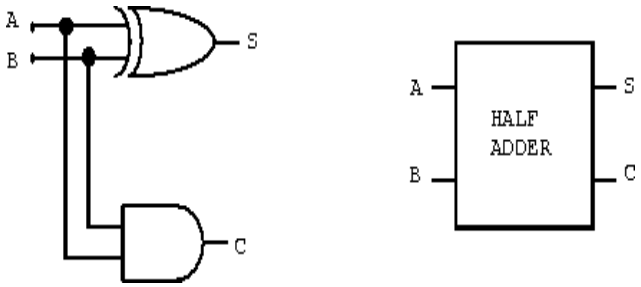


Fig.-3 Half adder

Boolean expression for half adder is -

$$S = \overline{A} \bullet B + A \bullet \overline{B}$$

$$C = A \bullet B$$

Boolean equation

V. BLOCK IMPLEMENTATION OF 4X4 VEDIC MULTIPLIER

The implementation of 4x4 Vedic multiplier using "Urdhva Tiryakbhyam" sutra is shown in the fig-4. The 4x4 multiplier is implemented using four 2x2 Vedic multiplier modules, 2 four bit full adders and half adder .Each 2 x2 multiplier consist of two inputs which are internally connected to each other.For the design of 4x4 block the first step is to grouping the two bit of each four bit input.This groupin pair will form vertical and crosswise product. The partial product shown represent the vertical and crosswise product terms.

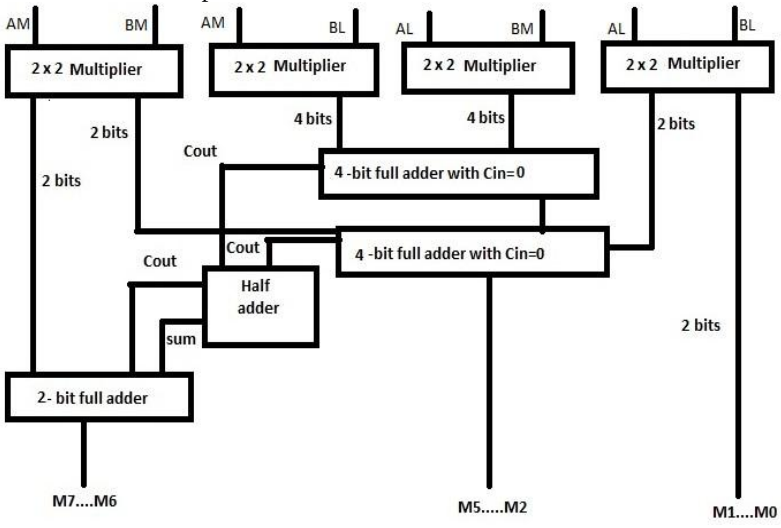


Fig-4. Block diagram of 4bit Urdhva multiplier with 4 bit full adder

VI. SIMULATION OF 4X4 MULTIPLIER

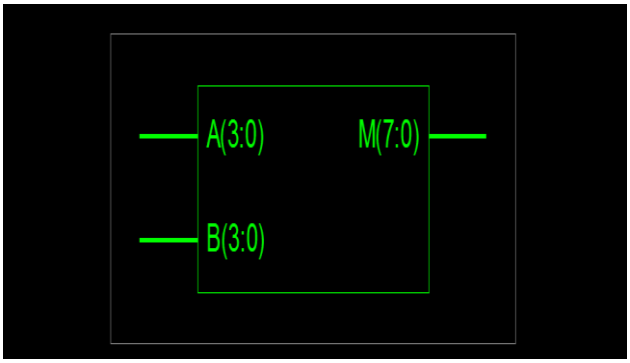


Fig.6:- block view of 4bit Urdhva Multiplier

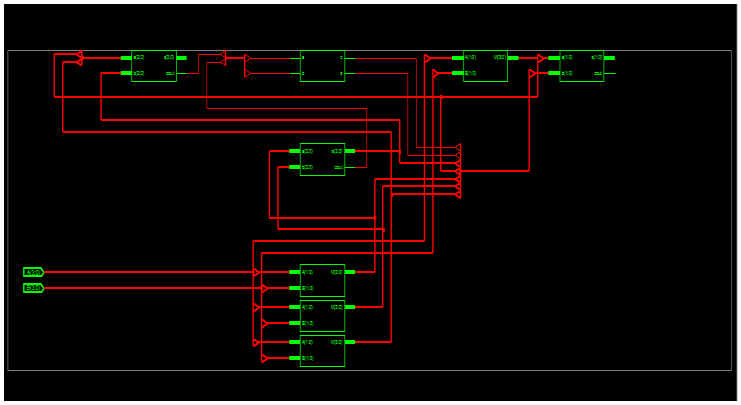


Fig.7:- RTL view 4bit Urdhva multiplier

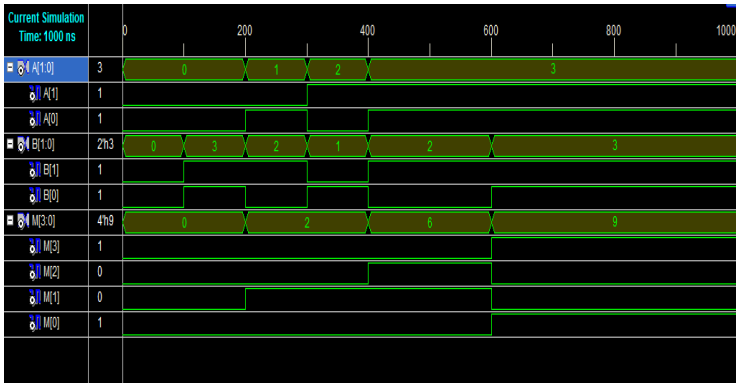


Fig.8:-simulation result of 4bit multiplier

VII. RESULT ANALYSIS

Table 1:- comparison of multiplier in the terms of delays

Types of multiplier (4 bit)	Delay(ns)
Urdhva multiplier with ripple carry adder	16.236
Traditional booth multiplier	25.52ns

This paper shows the comparison between 4bit multiplier with ripple carry adder, half adder,two bit adder Uradhvatiryakbhyam sutra the coding of 4x4 multiplier is done in VHDL,and it is synthesized and simulated using Xilinx ISE14.2.Software.

The result shows that 4x4 Vedic multiplier with ripple carry adder having less delay or we conclude that 4x4 Vedic multiplier is faster than 4bit traditional booths multiplier. And it acquire less area on the circuit and it take less power as compare to any other multiplier.

VIII. CONCLUSION

The high speed multiplier is used to design efficient full adders such as high performance and less delay significantly achieves high optimization. the efficient full adder design is implant in Vedic multiplier. Array and booth multiplier are not efficient than Vedic multiplier.Hence Urdhava Tiryakbhyam multiplier is the best multiplier compared to booth multiplier when compared to delay and power calculations.

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