Volume 5, Issue 1, January 2015 ISSN: 2277 128X
International Journal of Advanced Research in Computer Science and Software Engineering
Research Paper
Available online at: www.ijarcsse.com

Low Power Implementation of Rate 1-By-3 Viterbi Decoder on FPGA

Doli Vyas*, Shraddha Shrivastav, Rita Jain
Department of ECE, LNCT
RGPV Bhopal, India

Abstract— In high speed communication technology, hardware and software are crucial in field of electronics whereas decoding and encoding of any data, the VLSI based FPGA devices are used which provide high speed [1], low power features ,less area, high speed network connectivity, hardware portability, data error removal capability and complex algorithm realization etc. A high communication hardware rate decoder which is very commonly and effectively used in present scenario is Viterbi decoder. In this Trellis coded modulation (TCM) is involved for decoding of data. In comparison with normal decoders the Viterbi decoder not only offers reduced power and speed but it also provides reduced cost. In this paper the data error identification probability is improved with the design of Viterbi decoder used in low power operational performance in communication systems. The proposed design is implemented on a field programmable gate array (FPGA) device with a single bit error identification a correction ability of the conventionally proposed algorithm. The architecture of the decoder plays an important role in hardware complexity and high speed decoding among other various functional blocks on Viterbi decoder. The pipelined architecture design approach is used to implement the proposed decoder in this work. A single bit error if introduced in the transmitted data of the encoded bits during communication channel, can be effectively corrected by the proposed decoder design. The Proposed algorithm design is synthesized and simulated successfully on Xilinx ISE Tool [2] on Xilinx Spartan 3E FPGA for a rate 1/3 convolutional design architecture.

Keywords— Convolutional Code , Error correction code, error detection code, FPGA, Low Power, Trace Back, Trellis Diagram, Viterbi Decoder, Xilinx ISE.

I. INTRODUCTION

In the communication of data, the errors caused in the communication channel are very important to identify and rectify. Among the various error detection and correction (EDAC) techniques, Viterbi Decoder is very commonly implemented technique. In this technique of decoding of data, a trace back approach is used to recover the data bits that are encoded and transmitted in the system. Sometimes complex hardware architecture is utilized in the implementation of such architectures for a high data and high speed application. Use of rate-3/4 convolutional code is proposed for trellis coded modulation system for deep space communications in [3]. M-algorithm for Viterbi decoding implementation is shown in [4] and T-algorithm based design is shown in [5, 6]. Viterbi decoder design based on over-scaling supply voltage is proposed in [7]. Reduced-state sequence decoding based approach for Viterbi Decoder implementation is proposed in [8]. Power efficient Viterbi Decoder implementation using T-algorithm has been already proposed in [9, 10]. Pseudo NMOS and Dynamic logic based design of Viterbi Decoder circuit are proposed in [11]. An asynchronous design implementation based on Gate Diffusion Input is proposed in [12]. A high-rate convolutional code suffers from a decrease in bit-error-rate performance due to inherent drifting error between the estimated the accurate path matric during the trellis generation and the optimal path matric calculation. The design performance is highly dependent on the decoding latency of the circuit, overhead bits in the used algorithm, availability of memory elements, etc. The computational complexity and overhead are the main factors that affect the power consumption of the circuit. In this work, we analyzed the conventional Viterbi decoder algorithm and the proposed Viterbi decoder design algorithm for a rate 1/3 code. The remainder of this paper is organized as follows. Section II gives the gives the description of the proposed designs of Encoder, State Diagram of Encoding algorithm, Encoding Circuit Functional Diagram description and the Decoder Flow Diagram. The simulation and synthesis results are given in Section IV. Conclusion based on the proposed design is provided in Section V.

II. PROPOSED VITERBI ENCODER-DECODER DESIGN

This The current input and current state of an encoder is the output function of a Viterbi encoder. One or more logic gates and shift registers are realized as hardware circuit of a Viterbi decoder. XOR gate is generally used in circuit realization. To determine the interconnections of the registers and logic gate an empirical approach is used. The minimum hamming distance is determined by the hardware interconnection and number of memory element also it is used to determine the maximum number of error bits which the decoder corrects. The ratio of number of input bit(s) to the number of encoded output bit(s) is specified as the conversion rate for a Viterbi decoder. I.e. for a decoder with ‘n’ number of input bits and ‘m’ number of corresponding encoded bits is called as rate “n/m” encoder. Viterbi encoder`s simple block diagram is shown in Fig 3.

© 2015, IJARCSSE All Rights Reserved

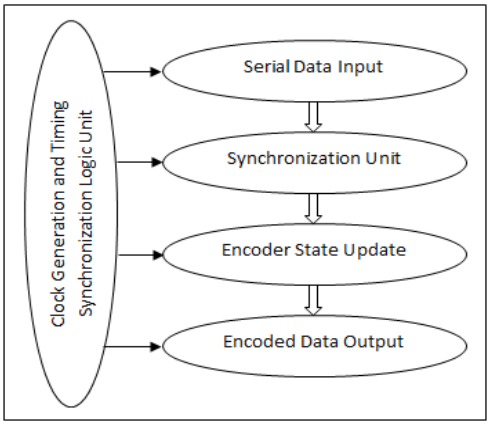

Fig. 1: Block Diagram of Implemented Viterbi Encoder

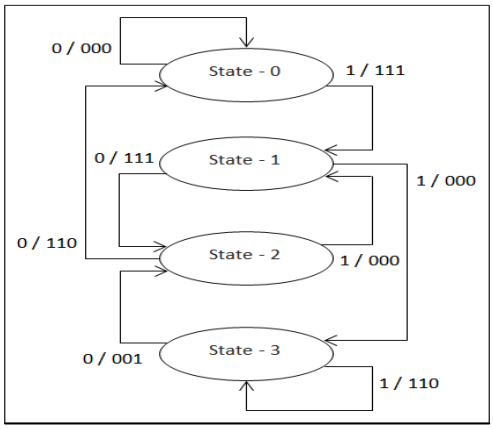

Fig. 2: State Flow Diagram of a Rate 1/3 Viterbi Encoder with 2-Memory Elements

The operation of a convolutional encoder and its encoding algorithm can be easily understood with the help of its state diagram. For example, Fig-6 represents the state diagram of the rate 1/3 Viterbi encoder. In this state model, there are 4-states of the decoder so it is realized using 2-Registers (Memory Elements). These four states are represented as State-0, State-1, Srate-2 and State-3. The encoded output is generated using the state information and the current input bit value. For generation of an encoded value, from any current state, there can be two possible transitions corresponding to logic-'0' input bit and logic-'1' input bit. For each of the transition from every state a specific output is generated. This output of state is also the output of the encoder against the input bit. A sequence of continuous logic '0' will move the current state to the initial state.

The proposed Viterbi encoder has four memory elements leading to a total of 16-states of the encoded data bit. The functional block of the proposed Viterbi encoder is shown in Fig-7. This functional diagram represents the encoding operation of the encoder logic circuit with the following logic state conventional equations:

$S0 = S_{in}$ xor M2 xor M0 … (i)

$S1 = S_{in}$ xor M3 xor M1 xor M0 … (ii)

$S2 = S_{in}$ xor M3 xor M2 xor M1 xor M0 … (iii)

Where, S_{in} is the serial input data bit,

M0 M1, M2, M3 are states of the memory elements.

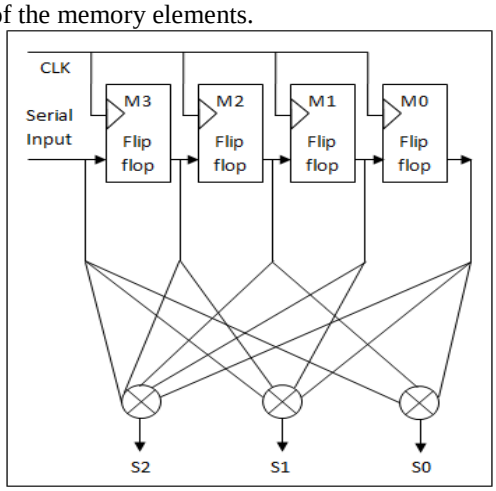

Fig. 3: Functional Diagram of Implemented Rate-1/3 Viterbi Decoder with 4-Memory Elements

© 2015, IJARCSSE All Rights Reserved

The 3-bit encoded output is generated using XOR Logic operation between the combination of Sin, M0, M1, M2 or M3 as mentioned in the equations (i), (ii) and (iii).

The serially received bits are first synchronized by the indentification of start and end of data packet with boundaries of the received symbol in viterbi decoder. The bits are processed for computing branch metric in synchronization with encoded symbol. Hamming distance between the corresponding received code symbol and the estimated actual bit code symbol is represented by branch metric. Accumulation of branch metric along the path is known as "path metric" and a state of computation at path metric at initial computation state is known as "State metric". State metric and branch metric values are updated at every state of computation in registers. The trace back method is used to generate the actual data bits from computed data with the help of complete receiving of symbol packet of a trellis. During the tracing of data, the path is selected with the help of decision hardware with a smaller path metric value. The data bits are decoded among the selected data bits along the trace back path. A viterbi decoder`s flow diagram is shown in fig-4.

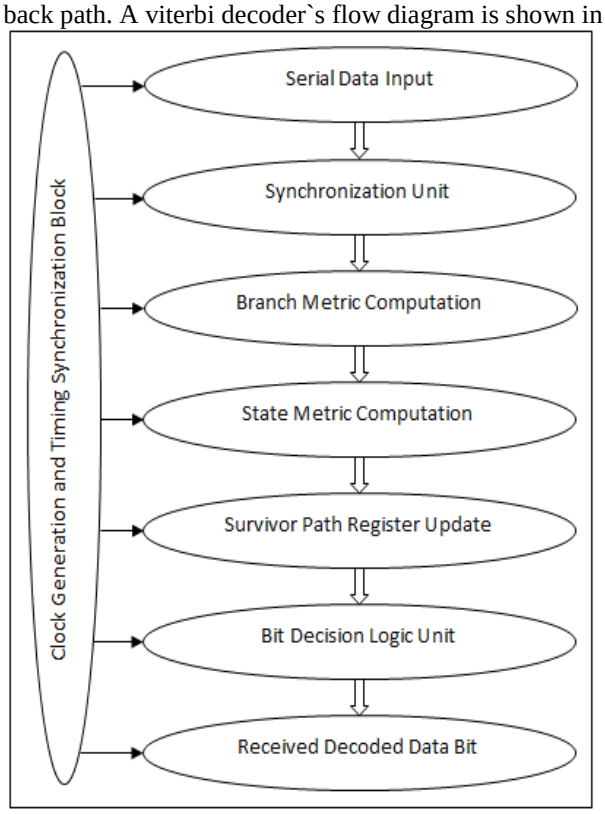

Fig. 4: Block Diagram of Implemented Viterbi Decoder

III. SIMULATION AND RESULT

The proposed design is simulated using Xilinx Tool on Xilinx Spartan-3E and Virtex-6 FPGA Devices. The waveform results of the functional Simulation of the proposed Encoder design is shown in Fig-7. The 16-bit input data that is used to encode using the proposed encoder design is:

Input 16-bit - 0110010101010011

The encoded output of the proposed encoder is:

Encoder Output (Binary) – 011 110 001 010 000 101 000 101 000 010 001 110 011 011 001 111

Encoder Output (Octal) – 3612050502163317

The simulation output of proposed encoder is decoded back using the proposed decoder design to get the actual data.

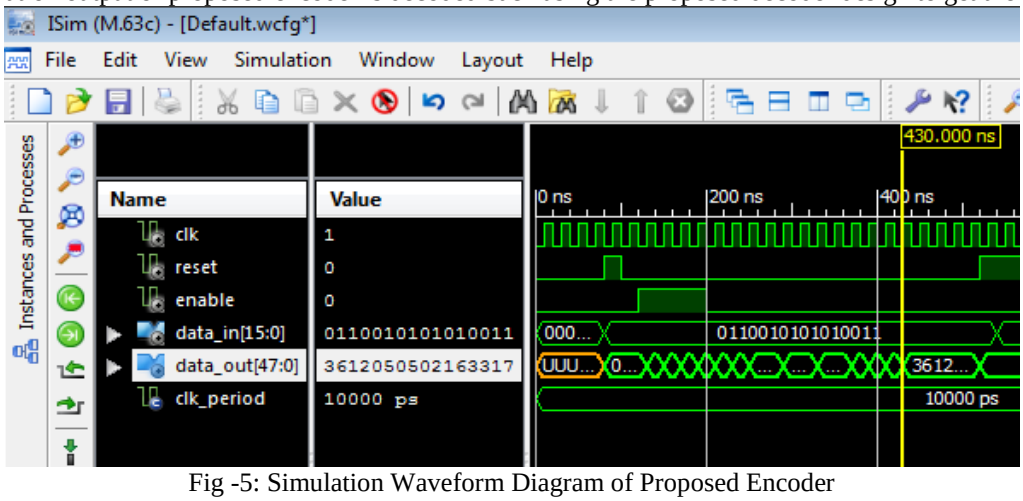

Fig -5: Simulation Waveform Diagram of Proposed Encoder

© 2015, IJARCSSE All Rights Reserved

The Hardware Utilization summary is presented in Table-I. The operational clock frequency vs dynamic power consumption summary of the proposed design is shown in Table-2.

TABLE I DESIGN HARDWARE UTILIZATION

Virtex-6 XC6VLX75T-1FF484	**Total**	**Encoder**		**Decoder**	
		Used	**%**	**Used**	**%**
Slices Reg	93120	238	1	364	0
LUTs	46560	448	1	423	0
LUT-FF Pair	-	153 out of 532	28	208 out of 490	42

a) Device Virtex-6 XC6VLX75T-1FF484

Spartan-3E XC3S500E-4PQ208	**Total**	**Encoder**		**Decoder**	
		Used	**%**	**Used**	**%**
Slices	4656	153	3	437	9
Flipflops	9312	102	1	362	3
LUTs	9312	200	2	623	6

b) Device Spartan-3E XC3S500E-4PQ208

TABLE III OPERATIONAL CLOCK FREQUENCY VS DYNAMIC POWER CONSUMPTION OF PROPOSED DESIGN

Device	**Frequency (MHz)**	**Dynamic Power Consumption**	
		Encoder	**Decoder**
Virtex-6 XC6VLX75T-1FF484	1000	0.168	0.082
	500	0.086	0.041
	250	0.043	0.021
Spartan-3E XC3S500E-4PQ208	1000	0.103	0.161
	500	0.053	0.082
	250	0.027	0.041

IV. CONCLUSIONS

A Viterbi Decoder is the most effective algorithm to identify single bit error during communication and also to recover the actual data from a single-bit error affected data. The presented design is an attempt to propose a low power design option of the Viterbi Decoder using a field programmable gate array device. The proposed design introduces only redundant bit overhead and effectively allows the proposed design to identify and correct a single bit change in the data. The proposed concept can be effectively introduced with large data packets while maintaining the same error identification and correction ability of the design.

ACKNOWLEDGMENT

The authors wish to convey special thanks to Mrs. Rita Jain (HOD, Department of Electronics and Communication Engineering, Laxmi Narain College of Technology, Bhopal, India) and Piyush Jain (Director Innovative Technology Design and Training Centre, Bhopal, India) for sharing ideas in line with the proposed work.

REFERENCES

[1] D. Chakraborty, P. Raha, A. Bhattacharya, R. Dutta, "Speed Optimization of a FPGA based modified Viterbi Decoder", *IEEE International Conference on Computer Communication and Informatics* (ICCCI-2013), January 2013.

[2] www.xilinx.com

[3] "Bandwidth-efficient modulations", *Consultative Committee For Space Data System*, Matera, Italy, CCSDS 401(3.3.6) Green Book, Issue 1, Apr. 2003.

[4] C. F. Lin and J. B. Anderson, "M-algorithm decoding of channel convolutional codes", presented at the *Princeton Conf. Info. Sci. Syst.*, Princeton, NJ, Mar. 1986.

© 2015, IJARCSSE All Rights Reserved

[5] S. J. Simmons, "Breadth-first trellis decoding with adaptive effort", *IEEE Trans. Commun.*, vol. 38, no. 1, pp. 3–12, Jan. 1990.

[6] F. Chan and D. Haccoun, "Adaptive viterbi decoding of convolutional codes over memory less channels", *IEEE Trans. Commun.*, vol. 45, no. 11, pp. 1389–1400, Nov. 1997.

[7] R. A. Abdallah and N. R. Shanbhag, "Error-resilient low-power Viterbi decoder architectures," *IEEE Trans. Signal Process.*, vol. 57, no. 12, pp. 4906–4917, Dec. 2009.

[8] J. B. Anderson and E. Offer, "Reduced-state sequence detection with convolutional codes," *IEEE Trans. Inf. Theory*, vol. 40, no. 3, pp. 965–972, May 1994.

[9] J. Jin and C.-Y. Tsui, "Low-power limited-search parallel state Viterbi decoder implementation based on scarece state transition," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 15, no. 11, pp. 1172–1176, Oct. 2007.

[10] F. Sun and T. Zhang, "Low power state-parallel relaxed adaptive Viterbi decoder design and implementation," in *Proc. IEEE ISCAS*, May 2006, pp. 4811–4814.

[11] Mohammad K.Akbari and Ali Jahanian, 2004, "Area efficient, Low Power and Robust design for Add Compare and Select Units", *Proceedings of the IEEE Conferecne on EUROMICRO Systems on Digital System Design* (DSD '04).

[12] Arkadiy Morgenshtein, M Moreinis and R Ginosar, 2004, "Asynchronous Gate-Diffusion-Input (GDI) Circuits", *IEEE Transactions on VLSI Systems*, 12, pp.847-856.

© 2015, IJARCSSE All Rights Reserved