Volume 5, Issue 1, January 2015 ISSN: 2277 128X
International Journal of Advanced Research in Computer Science and Software Engineering
Research Paper
Available online at: www.ijarcsse.com

Real Time, High Performance, RCE-NN Based Face Recognition System Using FPGA

Ramya .Rani .R
E&C & DBIT
Bangalore, India

Tejaswini .M .L
Assistant Professor, E&C, DBIT
Bangalore, India

Abstract—Faces represent complex multidimensional meaningful visual stimuli and developing a computational model for* face recognition is difficult.*This paper presents hardware implementation of a real-time, highly accurate face recognition system (FRS). Face image is captured from a camera connected to Field Programmable Gate Array (FPGA) based reconfigurable hardware board. Then the image is passed to contrast limited adaptive histogram equalization (CLAHE) unit which is used for image contrast enhancement which in turn increases the accuracy of the system, then image is passed on to discrete wavelet transform (DWT)unit to remove variable illumination & principal component analysis (PCA) is used to extract the features with 35 principal components which is optimized for performance and speed. Finally, Restricted Coulomb Energy (RCE) based neural network (NN) classifier is used for face recognition. The RCE based NN will be implemented using FPGA and thus the inherent parallelism is utilized effectively which is not possible with NN software implementation.

Keywords— FRS, CLAHE, DWT, principal components, FPGA.

I. INTRODUCTION

Face recognition is one of the conventional biometric authentication technique which is popular because it is non-intrusive and economic with low cost cameras and embedded systems. Over the past few years, extensive research works on various aspects of face recognition by human and machines have been conducted by psychophysicists, neuroscientist and engineering scientists. Face recognition plays a important role in user authentication. Automatic face recognition by embedded platform can be divided into two main approaches i.e. content-based and face based. In content-based approach, recognition depends on the relationship between human facial features such as eyes, mouth, nose, profile silhouettes and face boundary.

In proposed system we focus on hardware implementation of face recognition system(FRS) to attain greater accuracy and faster recognition time. The software based FRS takes longer time to recognize a person's face accurately due to sequential nature of processing. Hence, the proposed hardware based FRS .We have used CLAHE for adaptive local contrast enhancement for improving the local contrast of input image. Restricted Coulomb Energy (RCE) can be used for a wide range of applications primarily because it can learn any regular pattern and its training is faster than that of traditional multi-layer perceptron network. The faster learning is because the neurons are connected in parallel. The feature vectors are classified using RCE based classifier implemented in FPGA. In this case, the recognition time is independent of the number of neurons. FPGAs have turned out to be the best option in flexible digital signal processing hardware where they were often applied as configurable logic cells.

II. EXISTING METHODS

A. Frs based on proximal support vector machine

With the development science and technology, many industries urgently require the identification of the person's identity. Fingerprints and iris recognition technology has been good using, but the fingerprints and iris recognition has its own inadequacies. For example, the iris recognition needs to scan the iris of the human eye, so it may be hurt to human eye. Face extraction of face recognition possess of simplicity hidden and non-contact, so many scholars have been studying. Now, face recognition method have many types, one of method is support vector machine, it has been widely study by people. In recent years, support vector machine has breakthrough progress in theoretical research and algorithm realization, become a powerful means which overcome the "dimension disaster" and "over learning". Support vector machine is a compromise of empirical risk and generalization ability. The traditional support vector machine has many disadvantage, it is solving a quadratic programming problem. Its algorithm need to iterative, so the cost of time is very large, then, many of the requirements of real-time problem is not suitable for the use of the traditional support vector machine. To overcome this shortcoming, proximal support vector machine is used. It is an effective, simple, fast approximate support vector machine. The efficiency of its identification with support vector machine is slightly low, but reduce much time in training. In particular, it has better improve of training time when its dimension is not high and have a larger number of samples. Some areas of face recognition require real-time, however, traditional support vector machine cannot meet this requirement. PSVM have some characteristics that it meet the recognition rate of certain conditions and meet the requirement of real-time at the same time. PSVM has a wide application prospect in the field of face recognition .This PSVM method has poor discriminatory power and takes longer time to recognize persons face .

B. Frs based on combination of wavelet,pca and ann

A wavelet-based PCA method is developed so as to overcome the limitation of the original PCA method; furthermore, a neural network is utilized in order to carry out the classification of faces. A multilayer perceptron architecture is developed which is fed by the reduced input units, feature vectors generated by combination of wavelet. Here the usage of a particular frequency band of a face image for PCA is used to solve the first problem of PCA. The disadvantage of this method is that it had less recognition accuracy.

III. PROPOSED FACE RECOGNITION SYSTEM

The system consists of a CMOS sensor camera which has a resolution of 1Mps.An inbuilt FPGA based Real-time image processing module is present in the camera for image pre-processing and is used for face detection .The 1024x1024 image from the CMOS sensor is resized to 128x128 resolution image and passed on to the Reconfigurable Embedded Hardware Platform through the CamLink interface. This 128X128 resolution image obtained after cropping and resizing is known as frontal face image which is then given to CLAHE, the image pre-processing module. This module increases the performance accuracy of the system by enhancing the contrast of the image.

After that Daubechies-4 two dimensional DWT is performed for multi resolution analysis of the face images, remove variable illumination and select appropriate features/sub-band of the face images. Then PCA is performed for dimension reduction and feature extraction of the face images. This block gives us the feature vectors which is fed to the NN classifier for training, testing and recognition. NN is in the form of Register Transfer Logic (RTL) core implemented in Spartan-6 FPGA.

The final facial verification logic is carried out in the FPGA and the results of the analysis are passed to the on-chip MicroBlaze processor. The results are then captured by the Graphical User Interface (GUI) on host system for presentation to the user through the Ethernet port.

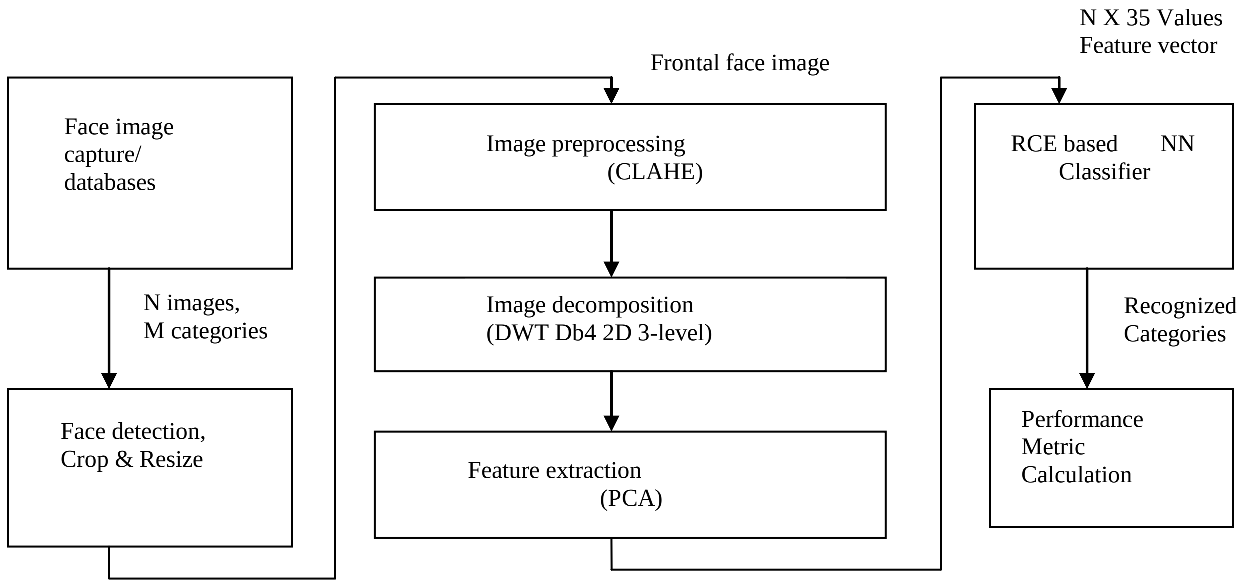

Fig 2.1. System overview block diagram

The GUI also provides interface to the embedded processor functions and diagnostics supported by the embedded firmware. In addition to supporting the above image processing modules the Hardware platform uses MicroBlaze processor of Spartan-6 FPGA to run a monitor program and firmware to support board diagnosis, embedded processor functions, bitstream Configuration and Control of the various sub-modules on the board.

The image from the CMOS sensor is resized using on camera processing and passed on to the reconfigurable Embedded Hardware Platform through the CamLink interface. The Serial data on the CamLink is de-serialized using a de-serializer and fed to Spartan-6 FPGA. The FPGA hosts the image processing pipeline which includes the contrast enhancement, image decomposition and projection to the eigen-space. The eigen-face projection vector is then passed to face recognition classifier. The outputs from the classifiers are then presented in the GUI along with the input face via on board 10/100/1000 mbps Ethernet interface. The board is populated with 512Mbit of FPGA NOR memory to store the configuration images of the on-board FPGA and another 512Mbit memory to store the MicroBlaze firmware image. The smart camera module, which is used to captures the face in steady state, feature a start-up or control switch to select the recognition. It is interfaced with the embedded hardware platform through 10 meter Camlink cable with both end terminated by 26 pin Mini D Ribbon (MDR) plug connector. CamLink consists of a transmitter, a receiver and is used to transfer digital data at a clock speed of 85 MHz.

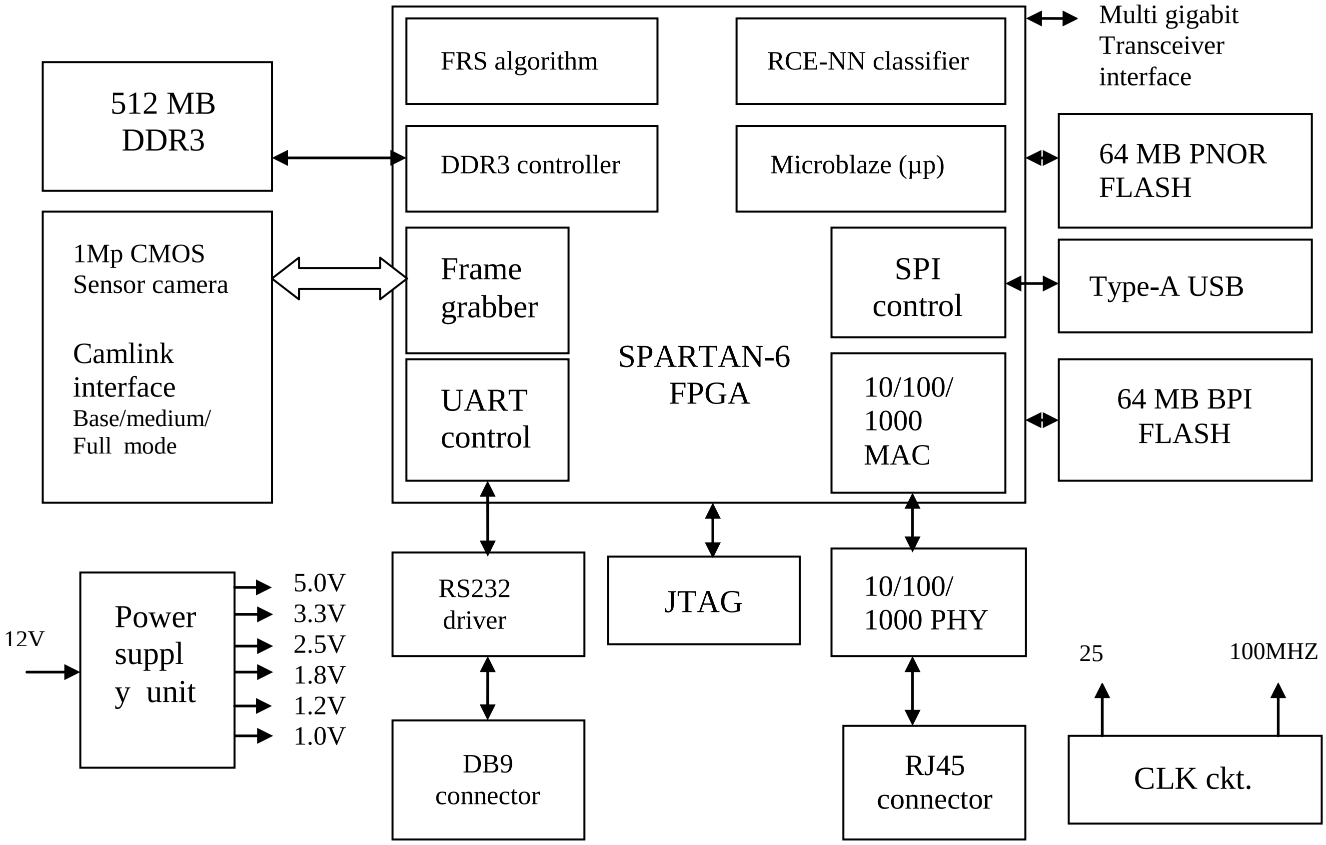

Fig 2.2. System hardware architecture block diagram

The transmitter converts 28 bits of CMOS/TTL data into four linear variable differential signal (LVDS) data streams. The data is sampled and transmitted with every cycle of the transmit clock. The receiver converts the LVDS data streams back into 28 bits of CMOS/TTL data. Using the transmit clock, 28 bits of TTL data is transmitted at 595 Mbps per LVDS channel. With four LVDS data channels the total data throughput is 2.04Gbit/s. It supports Basic, Medium, and Full CamLink specification, thus allowing up to approximately 800-900 MB/sec transfers at 85 MHz.

IV. RESULTS

Face image capture and face detection, crop and resize, CLAHE and DWT block, simulation results as done in MATLAB. Have implemented these blocks using MATLAB and have verified it, further the same block will be implemented on FPGA and facial features will be extracted and will be recognized using RCE-NN. The image resized to 128x128 in face detection, crop and resize unit is passed on to CLAHE block because this module increases the performance accuracy of the system by contrast enhancing the original images. After that Daubechies-4 two dimensional DWT is performed for multi resolution analysis of the face images, remove variable illumination and select appropriate features/sub-band of the face images. Then PCA is performed for dimension reduction and feature extraction of the face images. This block gives us the feature vectors which is fed to the NN classifier for training, testing and recognition.

The results are then captured by the Graphical User Interface (GUI) on host system for presentation to the user through the Ethernet port. The GUI also provides interface to the embedded processor functions and diagnostics supported by the embedded firmware.

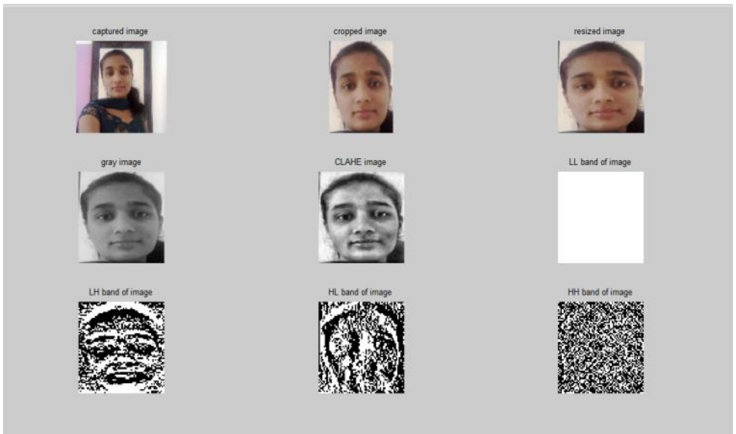

Fig 3.1. Simulation result of face detection, crop resize, CLAHE and DWT unit

V. CONCLUSIONS

Real-time, improved face recognition system design & its implementation on FPGA based embedded platform is presented in this paper. The face images are captured using CMOS sensor camera connected to FPGA board via CamLink. Image pre-processing techniques namely CLAHE, DWT & PCA are implemented for local contrast enhancement, image decomposition & dimensionality reduction respectively. The 35 feature vectors derived from PCA module are used to categorize and recognize the face using RCE based classifier. We have fully utilized the parallelism of the NN architecture by implementing this RCE based NN in FPGA itself.

ACKNOWLEDGMENT

Wishes to acknowledge Mrs.Tejaswini.M.L who has helped me in the preparation of this paper .

REFERENCES

[1] Santu Sardar & K. Ananda Babu, "*Hardware Implementation of Real-Time, High Performance,* RCE-NN based Face Recognition System" IEEE,2014 27th International Conference on VLSI Design and 2014 13th International Conference on Embedded system.

[2] Santu Sardar, Gaurav Tewari, K. A. Babu, "*A Hardware/Software Co-design model for Face Recognition using Cognimem Neural Network chip* " 2011 International Conference on Image Information Processing (ICIIP 2011).

[3] N. Kouda and N. Matsui, "On the function approximation in restricted coulomb energy neural network with gaussian radial basis function," 2011.

[4] Chao Sui, Ngai Ming Kwok, Tianran Ren, "*A Restricted Coulomb Energy (RCE) Neural Network System for Hand Image Segmentation*" 2011 Canadian Conference on Computer and Robot Vision.

[5] G. Tewari, S. Sardar, and K. A. Babu, "*High-speed & memory efficient 2-d dwt on xilinx spartan3a dsp using scalable polyphase structure with da for jpeg2000 standard*," 3rd International Conference on Electronics Computer Technology (ICECT 2011), Kanyakumari, India, 2011.

[6] C.-S. Fahn and Y.-T. Lin, "*Real-time face recognition techniques used for the interaction between humans and robots*," in Computer Symposium (ICS), 2010 International, 2010, pp. 234–239.

[7] L. Lang, F. Xia, and X. Wang, "*Study of face recognition algorithm based on support support vector machine*," in Intelligent Computation Technology and Automation,2009. ICICTA '09. Second International Conference on, vol. 1, 2009,pp. 702–705.

[8] M. Mazloom and S. Ayat, "*Combinational method for face recognition: Wavelet, pca and ann*," IEEE Computer Society, 2008.

[9] P. Sinha, B. Balas, Y. Ostrovsky, and R. Russell, "*Face recognition by humans: Nineteen results all computer vision researchers should know about*," Proceedings of the IEEE, vol. 94, no. 11, 2006.

[10] X. MuMehmet, A. Paul, W. Mohamad, and H. Hassoun, "*An rce-based associative memory with application to human face recognition*," Neural Processing Letters, 2006.

