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Review on Low Power Pulse Triggered Flip-Flops

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Abstract*— *In digital CMOS design, power consumption has been a major concern for the past several years. Advanced IC fabrication technology allows the use of nano-scaled devices; so the power dissipation becomes the major problem. Flip-flops are widely used in many sequential logic circuits such as registers, memory elements, counters, etc. These circuits are widely used in the implementation of VLSI chips. Therefore the power consumption of such circuits should be improved, without deteriorating other characteristics.

Pulse-triggered FF has a simple circuit which lowers the power consumption of the clock tree system. A P-FF consists of a pulse generator for strobe signals and a latch for data storage. If the triggering pulses are narrow, then the latch acts like an edge-triggered FF. P-FF gives a higher toggle rate for high-speed operations.

Keywords*— *Flip-Flop, latch, power, pulse triggered, high-speed.

I. INTRODUCTION

A flip flop or latch is a circuit that has two stable states and can be used to store state information. The difference between latches and flip-flops is that for latches, their outputs are constantly affected by their inputs as long as the enable signal is asserted i.e., in latches when they are enabled, their content changes immediately when their input change [2]. Flip-flops are fundamental building blocks of electronics system used in computers, communications and many other systems. They are used for storage of states (0 or 1). When used for infinite storage machines the output and the next state depends not only on current inputs, but also on current state, it can be used for counting pulses. A flip flop generally consists of two inputs, a clock generator or a clocking signal and two outputs. One being the normal value of the output and the other is complement value of bit stored in it. The output of flip flop is either logic 0 or logic 1.

Flip-flops (FFs) are used as the basic storage elements used in all kinds of digital designs. Most of the power applied to the chip is been accommodated by the flip flop. Flip-flop is one of the most power consumption components. It is important to reduce the power dissipation in both clock distribution networks and flip-flops. The power delay is mainly due to the clock delays [1] [2]. It is estimated that the power consumption of the clock system, which consists of clock distribution networks and storage elements, is 50% more than the total system power. On the other hand Flip-flops can change their content only either at the rising or falling edge of the enable signal. This enable signal is usually the clock signal. After the rising or falling edge of the clock, the flip-flop content remains constant even [2].

Master-slave flip-flops, sense amplifier based flip-flops and pulsed-triggered flip-flops are used in many existing microprocessors. Master-slave flip-flops consist of two stages, one is master and another one is slave and they are characterized by their hard-edge property [7] [10]. Examples of master-slave flip-flops are transmission gate based POWERPC 603, push–pull D-type-flip-flop (DFF), and true single phase clocked (TSPC) flip-flop [7]. Master-slave flip-flops and sense amplifier based flip-flop are characterized by positive setup time, causing large D-to-Q delays. On the other side, pulse-triggered flip-flops reduces the above two stages into one stage and is characterized by the soft edge property and a negative setup time, resulting in small D-Q delay [7] [10]. Pulse-triggered flip-flops can be classified into different types of flip-flops. Based on the pulse generators used, pulse-triggered flip-flops can be categorized into two types as: implicit-pulsed and explicit-pulsed. Pulse triggered flip-flops can be static, or semi-static, or dynamic, or semi-dynamic. And pulse-triggered flip-flops can also be classified into single-edge triggered flip-flops and double-edge triggered flip-flops. In implicit-pulse triggered flip-flops (ip-FF), the pulse is generated inside the flip-flop, example, hybrid latch flip-flip (HLFF), semi-dynamic flip-flop (SDFF), and implicit-pulsed data-close-to-output flip-flop (ip-DCO). Whereas, in explicit-pulse triggered flip-flops (ep-FF), the pulse is externally generated, for example, explicit-pulse data-close-to-output flip-flop (ep-DCO) [7] [10] [1].

II. LITERATURE REVIEW

Jin-Fa Lin has proposed external type pulse low power flip-flop and modified true single phase clock latch using 90 nm CMOS technology which is based on a signal feed-through scheme. In this paper first they have compared and discussed about some existing pulse triggered flip-flops such as ep-DCO, CDFF, Static-CDFF, MHLFF. Drawbacks of this flip-flop were long discharging path problem, longer delay and larger switching power dissipation.

He proposed a low-power P-FF design based on a signal feed-through scheme consisting of a pass transistor and pseudo-nMOS logic. His design managed to reduce the delay in latching the data “1” and “0,” and also reduced the longer delay by feeding the input signal directly to an internal node of the latch design which speeds up the data transition [1].

Saranya. L et al. have designed Low-Power Pulse-Triggered flip-flops. They studied and designed three different kinds of conventional pulse-triggered flip-flops. The implicit Pulsed Data-Close to output (ip-DCO) pulse-triggered flip-flop, the Modified Version of Hybrid latch flip-flop (MHLFF) and the Single-ended Conditional Capturing Energy Recovery (SCCER) flip-flop. Their design carried out comparison of low power pulse triggered flip-flops between SAL, SVL logics and they obtained the best power -delay-performance [2].

Ip-DCO is implicit kind of flip-flop where the pulse is generated inside the flip-flop itself. DCP mans that the input node is kept closer to the output node so it gives less data to output delay. The Hybrid Latch Flip-Flop reduces the complexity of the locking mechanism results in small delay and small area. The Modified Version of Hybrid Latch Flip-Flop uses less number of transistors and also less power consumption. SCCER circuit achieves low energy dissipation by restricting current flow across the device with low voltage drop and by recycling the energy stored on their capacitors by using an AC type supply voltage.

Tania Gupta et al. paper have designed dual edge triggered flip flop. They compared three existing designs of dual edge triggered flip-flop such as EP_CDFF, EP_CPFF and DET-SAFF with the proposed design of the dual edge triggered flip-flop (DET-FF). In EP_CDFF type of design included pulse generator and conditional discharge. The pulse generator is used to produce the dual pulse which is active at both rising and falling edge of the clock. Conditional discharge technique is used to reduce the unnecessary charging and discharging of the internal major nodes when the input is same for the long time, which leads to the power consumption. In EP_CPFF type of design includes conditional pre-charge technique for removing the redundant transitions of the flip-flop to reduce the power dissipation. In DET-SAFF type of design sense amplifier is used for flip-flop design.

The dual edge triggered flip-flop design eliminates the redundant transitions of internal nodes when current data is same for long time and also disables the clock when the input invokes no output changes in a control circuit. This flip flop design significantly reduces the power dissipation [3].

Sayed Alireza Sadrossadat et al. have proposed a statistical design of the flip-flops circuits to achieve a high yield, to meet the performance, leakage power, switching power, and layout area design specifications using 45 nm CMOS technology. Their proposed design provides solution for design parameters such as width and length of the flip-flop transistors, which provide maximum immunity to the process variations in the transistor dimensions and threshold voltage. The proposed design showed that for a given flip-flop design specifications, the flip-flops have to be designed using statistical sizing tools to improve the timing yield [5].

Massimo Alioto et al. have compared a large number of FFs i.e., 19 topologies belonging to four different classes in 65-nm CMOS technology. The comparison has been performed on the basis of whole energy-delay-area design space. The other parameters considered for comparison were layout parasitic, leakage in both standby and active mode, wide load and switching activity.

According to their analysis, the fastest topology is the STFF, the best low-energy FFs are the DETTGLM and TGFF, whereas the most energy-efficient TGPL [6].

Chen Kong et al. have designed the D-flip-flop, known as adaptive-coupling flip-flop (ACFF), which has a reduced transistor count as compared to other low-power flip-flops, and also 2 fewer transistors than the transmission-gate flip-flop (TGFF) using 40 nm CMOS technology. ACFF uses a single-phase clocking structure, with no local clock buffer and no pre-charging stage, which is more energy efficient than TGFF. This type of flip-flop saves up to 77% energy at 0% data activity. ACFF has a smaller standard deviation of delay times, especially at 0.8V with 18ps as compared to 34ps of σ for TGFF. ACFF design replaces about 84% of the FFs which shows that the more number of FFs meet the timing constraints despite ACFF having a larger setup time than TGFF [4].

Elio Consoli et al. have proposed a complete design methodology for nanometer flip flops using 65 nm CMOS technology. This design methodology permits to optimize FFs and also proposed appropriate metrics with physical meaning and various properties. These appropriate design metrics and the exploitation of their properties allows to widely explore the design space with a reduced computational effort [8].

Massimo Alioto et al. have analyzed various types of flip flops to check the influence of the clock slope on the speed and the overall energy dissipation of both FFs and clock domain buffers using 65 nm CMOS technology. Their analysis showed that an optimum clock slope minimizes the energy spent in a clock domain. Their results showed that 30/40 %energy savings with minimum the clock slope requirement can be relaxed with respect to traditional assumptions. They discussed various points as effectiveness of the clock slope optimization and optimization in terms of additive skew and jitter contributions for the existing classes of FFs.

Their analysis has revealed that, the speed performance of FFs is unaffected by the clock slope, whereas the FF energy dissipation is more heavily influenced. Analysis of the energy contributions in a clock domain has shown that a smoother clock slope increases the FF energy, and decreases the energy dissipated by the local clock buffer [9].

DAI Yan-yun et al. have designed a flip-flop design method using transmission voltage-switch theory using 0.18μm CMOS technology. This design is suitable for all kinds of pulse-triggered flip-flops and no extra work is required for eliminating the switching activities of internal nodes. Based on the proposed structure and design technique, two pulsed flip-flops were implemented and simulated. Using transmission voltage-switch theory technique they designed two pulsed flip-flops (D and JK Flip-flops).

In this design the proposed pulsed D flip-flop outperforms the conventional D flip-flop by 17.2% in delay and 30.1% in power-delay-product (PDP). Their results showed that the proposed pulsed JK flip-flop has low power and small PDP as compared to pulsed D flip-flops and proposed pulsed D flip-flops [10].

Peiyi Zhao et al. have proposed level conversion flip-flop (CPN-LCFF) using a Clustered voltage scaling technique using 0.18µm CMOS technology. Clustered voltage scaling (CVS) is an effective way to decrease power dissipation. In the CVS scheme, by using low supply voltage (VDDL) in speed insensitive paths and using high supply voltage (VDDH) in speed sensitive paths, the whole system power consumption can be reduced without disturbing the performance.

In this paper the author has investigated various level-shifting flip-flop topologies as: differential style, n-type metal–oxide–semiconductor (NMOS) pass-transistor style, and precharged style. The author proposed the clocked-pseudo-NMOS (CPN-LCFF) flip-flop, which combines the conditional discharge technique and pseudo-NMOS technique. Here the new CPN-LCFF outperforms the previous LCFF in terms of power and delay by 8% and 15.6%, respectively. Hence, CPN-LCFF is suitable for low-power high-performance systems [11].

Hamid Mahmoodi et al. have proposed four novel energy recovery clocked flip-flops as SAER, SDER, SCCER, and DCCER using TSMC 0.25- m CMOS technology which uses energy recovery from the clock network, resulting in significant energy savings. In this flip-flop design, the author implemented 4 proposed energy recovery clocked flip-flops through an H-tree clock network driven by a resonant clock-generator to generate a sinusoidal clock.

In this paper, author has used energy recovery techniques to the clock network which is capacitive signal in a chip. The proposed energy recovery clocking scheme recycles the energy from this capacitance in each cycle of the clock. Here the clock gating solutions are proposed for the energy recover clock. Here they applied clock gating to energy recovery clocked flip-flops in which power got reduced by amount of (1000X) during the sleep mode. Their results showed a power reduction of 71% on the clock-tree and 39% on flip-flops, resulting in an overall power savings of 25% for the multiplier chip [12].

S.H. Rasouli et al. have presented a paper on low-power flip-flops using 0.18 nm CMOS technology. Here they have proposed a design for modified hybrid latch flip-flop and double edge-triggered modified hybrid latch flip-flop. The single-edge-triggered flip-flop, called the MHLFF (modified hybrid latch flip-flop), is used instead of HLFF to reduce the power dissipation of the HLFF (hybrid latch flip-flop) by avoiding unnecessary node transitions. To reduce the power consumption of the flip-flop further, the double edge- triggered modified hybrid latch flip-flop (DMHLFF) is also proposed.

Their results showed that the MHLFF outperforms the SDFF by 21% in the power delay product. The double edge-triggered flip-flop (DMHLFF) was also proposed to reduce the power consumption further. The improvement in the power delay product for DMHLFF was up to 21% compared to LSDFF [13].

M. W. Phyu et al. have proposed a Low-Power Static Dual Edge-Triggered Flip-Flop design using 0.18-µm CMOS technology. This new static dual edge-triggered flip-flop that incorporates the benefit that it has no pre-charging and uses conditional discharging, which efficiently reduces the switching activity at the internal node and also reduces power dissipation. Such improvement is achieved by the concept of fan in concept. Here they have studied other flip-flops as ep-DCO, ep-SFF and CDFF and compared with the proposed -Power Static Dual Edge-Triggered Flip-Flop.

Their results showed that the SCDFF achieves a gain of 18.9% as compared to ep-DCO in terms of PDP, but reduces to 13.2% when compared to CDFF [8]. Also they have achieved the gain of 13% improvement in total gate area as compared to the best ep-SFF for minimum power-delay product (PDP) [14].

Peiyi Zhao et al. have proposed a High-Performance and Low-Power Conditional Discharge Flip-Flop design using 0.18µm CMOS technology. This paper is organized in two sections as follows: Firstly they described different techniques used to reduce the switching activity inside the flip-flops based on two categories: the conditional precharge and the conditional capture technologies. Secondly they introduced the new technique for low-power and high-speed designs.

A new flip-flop is introduced is based on a technology, known as the conditional discharge technology. This design CDFF reduces the internal switching activities, and also generates less glitch at the output, maintaining the negative setup time and small D-to-Q delay characteristics. The proposed flip-flop can save up to 39% of the energy as compared to the fastest pulsed flip-flops having a data-switching activity of 37.5% [7].

Nikola Nedovic et al. have proposed a dual edge triggered flip flop based on Conditional Pre-Charge Techniques using 0.18µ m CMOS technology. A new dual edge-triggered flip-flop saves power by inhibiting transitions of the nodes. This dual edge-triggered flip-flop saves power by reducing the internal switching activity as well as the clock period. The main advantage of DETFF is that they operate at half the frequency of the conventional single-edge clock, obtaining the same data throughput. Thus, power consumption of the clock generation and clock distribution system is halved.

The proposed DETFF outperforms other dual edge triggered storage elements by 12% and l0%, in terms of delay and EDP improvement respectively. The proposed DETFF allows substantial saving in clock distribution network by reducing clock power [15].

Vojin G. Oklobdzija et al. has presented a review of some of the techniques of high performance and low-power designs. He presented an overview of clocking and design of clocked storage element. Systematic design of different low power flip-flops such as conditional capture flip-flop, conditional discharge flip-flop is explained. The issues related to power consumption and low-power design are presented [16].

James Tschanz et al. have presented an analysis of delay and energy for Single Edge- Triggered & Dual Edge-Triggered Pulsed Flip-Flops. The paper described the use of flip-flop optimization which is used to determine the transistor sizes in the various flip-flop topologies and minimize total energy per cycle (E) for different values of data-to-Q (D-Q) delay.

In next part they compared several types of single edge-triggered flip-flops such as Implicit-pulsed semi-dynamic flip-flops, Implicit-pulsed static flip-flops and Explicit-pulsed flip-flops and also several types of dual edge-triggered flip-flops such as Conventional DET flip-flops, Explicit-pulsed DET flip-flop. There results showed that ip-DCO has the fastest delay. ep- FF is the most energy-efficient due to its static design and its low transistor count [17].

Bai-Sun Kong et al. have proposed Conditional-Capture Flip-Flop using 0.35 nanometer CMOS technology. This proposed design statistically achieves power reduction by eliminating redundant transitions of internal nodes. These flip-flops have negative setup time and hence provide small data-to-output latency. They presented the analysis of conventional high-performance flip-flops such as transmission-gate flip-flops (TGFFs), hybrid latch-flip-flops (HLFFs), semi-dynamic flip-flops (SDFFs), and sense amplifier-based flip-flops (SAFFs) and drawbacks of these flip-flops due to more power consumption. Their simulation results showed that the proposed Conditional-Capture flip-flop achieves power savings up to 61% while the single-ended structure provides the power savings up to 67%, as compared to conventional flip-flops. With a typical switching activity of 0.33, the power consumption is reduced by 23–30% with comparable minimum data-to-output latency [18].

III. CONCLUSIONS

In this paper the different types of low power flip-flops are compared and analyzed and also different techniques for designing of low power pulse triggered flip-flops are studied.

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