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# Design of a Three Lead ECG Amplifier System

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***Abstract - In this paper we present the design and development of a three lead ECG amplifier system. This circuit is capable of achieving, amplifying and filtering the low amplitude, desired ECG signals. The system has been designed at 33Hz to reject the power line frequency of 50Hz, so as to protect the circuit from the major noise interference which is the power line frequency. The system has been designed to use a combination of passive and active filters so as to achieve effective filtering of the noise and process the required ECG signals.***

***Keywords – ECG pre-amplifier, amplifier design, filter design, simulation, circuit implementation***

## I. INTRODUCTION

Low power consumption and low cost are the main issues in personal biomedical instruments. The performance of any personal biomedical system depends on the effectiveness in extraction and amplification of low-level bio-potential signals effectively from a noisy environment. To reduce the cost as well as the power consumption, compact design of personal medical instruments is desirable [1]. In this paper, we present a simple, low cost circuit design of an ECG amplifier system. The system is designed at a frequency of 33Hz, well below the power line frequency to avoid its interference which is the major problem with the commercial ECG systems.

## II. BLOCK DIAGRAM OF THE AMPLIFIER SYSTEM

The ECG amplifier system block is as shown as in figure 1. The preamplifier was designed using IC LM 324 and the ECG amplifier was designed using IC LM 386. Two output options are provided one at the output of the pre-amplifier and the other at the output of the ECG amplifier.

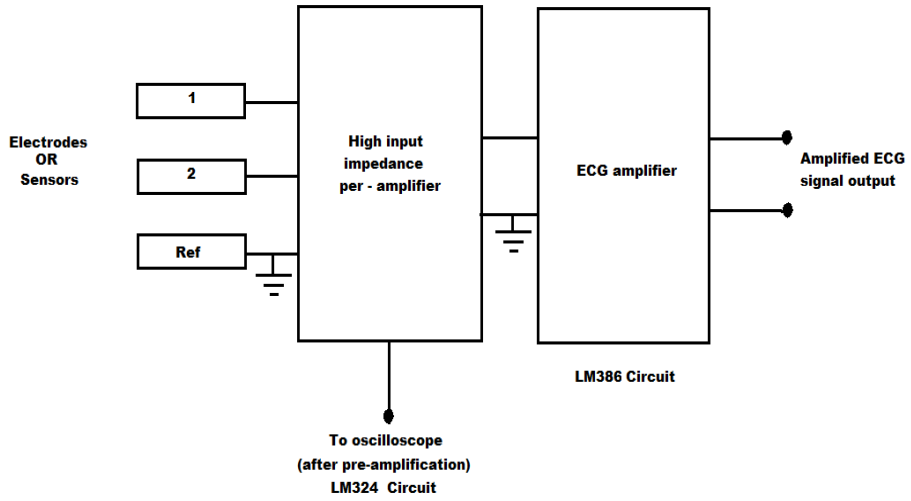



Figure 1. Block diagram of ECG amplifier

**Sensors**: Since the proposed work is to develop a three lead ECG system, three sensors, Sensor 1, Sensor 2 and the reference sensors were used. These developed sensors were connected to the Op-Amp amplifier inputs.

**Pre-amplifier block:** This block is constructed to amplify the low amplitude, low frequency sensor output and to present the same for further power level enhancement process.

To get the required characteristics of high input impedance and high CMRR, an Instrumentation Amplifier with Op-Amps is usually used as the first stage of a bio-potential amplifier. The architectures of an Instrumentation Amplifier can be either the 3 Op-Amps system or the current-feedback type [2, 3]. The three Op-Amps system is easy to construct while the current feed type has inherent higher CMRR. Both types can be constructed using commercial available integrated-circuit (IC) form.

**ECG amplifier block:** This block is constructed to enhance the power levels of the pre-amplified signal. The output of the pre-amplifier feeds the input of this block. This block uses a low voltage audio power amplifier in the IC form. The output of this block is the amplified ECG signal, ready to be transmitted.

## III. CIRCUIT DESIGN

**Pre-amplifier designing**

This section deals with the design and development of the amplifier and the filter required to process the ECG signal for display and further transmission. The inputs for this section are derived from three sensors, developed using Titanium dioxide as the base material. The circuit is designed to amplify the signals and at the same time eliminate as much noise as possible. The high frequency noise and the common mode noise both have to be addressed to, in designing the circuit.

The first stage of the circuit is the preamplifier stage which is a very crucial stage which has to produce high gain and should provide a good Common Mode Rejection. The input level shifter circuit shifts the signal level required for the digitizing of the signal at a later stage [4, 5]. The buffer amplifier ensures that the resistive loading is avoided and also provides high input impedance.

The voltage difference between the two electrodes serves as the signal input that is amplified through the Op-Amp circuits. These signals are then differentially amplified and passed through a low pass filter whose cut-off frequency is around 33Hz. The next stage is a second order low, Sallen-Key, pass filter which is used for anti-aliasing.

To nullify any wandering DC effects, a simple RC high pass filter with a very low cut off frequency has been implemented. The cut-off frequency has been chosen to be 1.6Hz and the capacitor value is chosen to be 10μF.

Since $f = 1/(2\pi RC)$, R = 9.9522k Ω, which has been taken to be 10kΩ.

To reject the noise frequency at 50Hz from the power mains, the acquired signal requires low pass filtering below 50Hz. The cut-off frequency has been selected to 33Hz to reject the power line frequency.

Let R = 100kΩ, $f = 1/(2\pi RC)$ and $f = 33$Hz, hence C = 47nF = 47kpF

The two signals are added and passed through an anti-aliasing Low Pass Filter which also provides a gain of 100 as shown in figure 2.

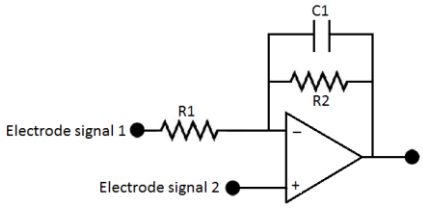
Gain $A = -R_2/R_1$ and the required gain is 100

Chose $R_1 = 100k\Omega$, then $R_2 = 10M\Omega$

$f = 1/(2\pi R_2 C_1)$ and f = 33Hz

Then $C_1$ = 483pF and hence chosen to be 470pF

Circuit simulation has been carried out with the help of 5spice Analysis software, version 1.67. 5Spice provides Spice specific schematic entry, the ability to define and save an unlimited number of analyses, and integrated graphing of simulation results.



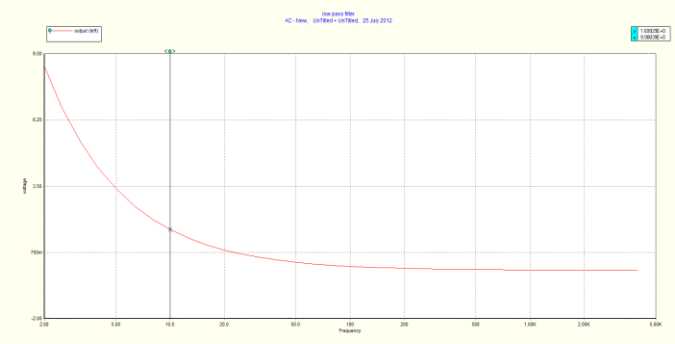
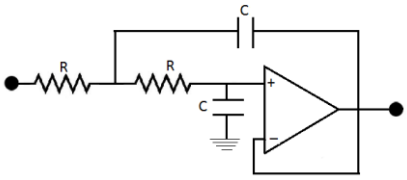



Figure 2. Anti-Aliasing low pass filter and the simulation result of the circuit with 5spice

This signal is passed through a Second order Sallen-key, unity gain low pass filter to get a narrow bandwidth of about 15.31 Hz as shown in figure 3.

$f = 1/\sqrt{(2\pi R_1 C_1 R_2 C_2)}$; when $R_1 = R_2 =$ R and $C_1 = C_2 = C$; then $f = 1/(2\pi RC)$

Let R = 100kΩ, then C = 106.15nF. Hence C is chosen to be 104kpF



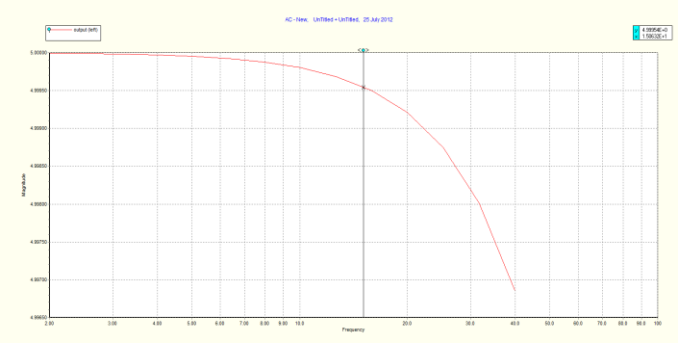



Figure 3. Second order Sallen-key, unity gain, low pass filter with its simulation result

The output of this filter is fed to two stages of passive filters for step wise elimination of noise. These two stages of passive LPFs give a second order response with a roll-off rate of -40 dB/ decade as shown in figure 4. The two step attenuation of the signal is compensated by providing an equivalent gain by the non-inventing amplifier.

$f = 1/(2\pi RC)$; f = 15.31Hz,

Let R = 100kΩ, then C = 106.15nF. Hence C is chosen to be 104kpF

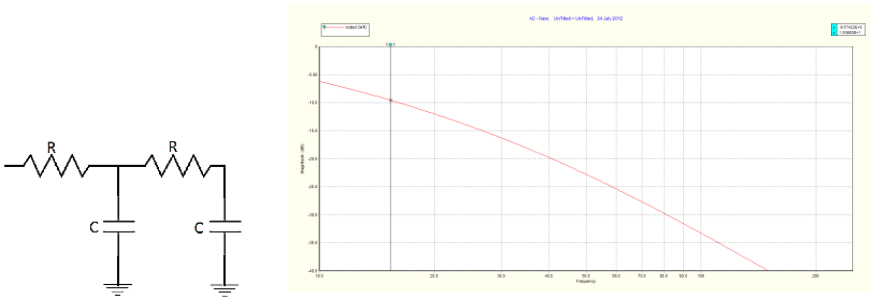



Figure 4. Two stages of Passive RC low pass filters with its simulation result

The final output is ready to be connected to the CRO, and is fed to the ECG amplifier. The same output is fed to an LED through a transistor switch to indicate the pulsing of the heart as shown in figure 5.

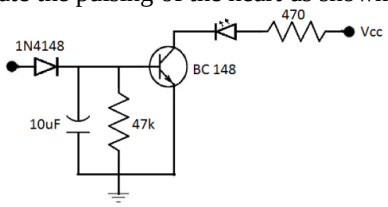



Figure 5. Final output stage of the pre-amplifier

**ECG amplifier designing:**

Figure 6 shows the circuit diagram of the ECG amplifier constructed using IC LM386. The LM386 is a power amplifier designed for use in low voltage consumer applications. The gain is internally set to 20 to keep external part count low, but the addition of an external resistor and capacitor between pins 1 and 8 will increase the gain to any value up to 200. The capacitor also maintains the DC bias levels in the gain adjustment circuit. The unused input is grounded to keep the DC offset voltages low [6]. Also, when using LM386 with higher gains, it is necessary to bypass the unused inputs, preventing degradation of gain and possible instabilities. The capacitor connected between pins 2 and 6, provides power supply decoupling. The RC circuit between the output point and ground acts as a high frequency load to provide stability. The potentiometer at the input pin provides adjustable input level attenuation.

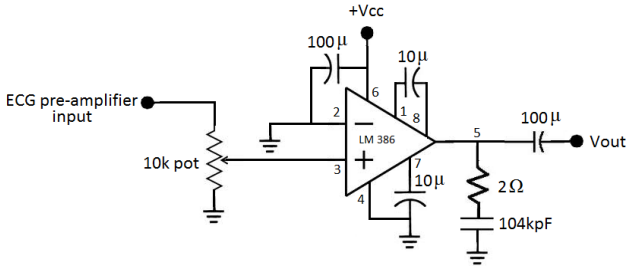



Figure 6. Circuit diagram of the ECG amplifier constructed using IC LM386

## IV. CIRCUIT DIAGRAM OF THE ECG AMPLIFIER STAGE

Figure 7 shows the complete circuit diagram of the ECG amplifier stage. The circuit shows the pre-amplifier and the ECG amplifier.

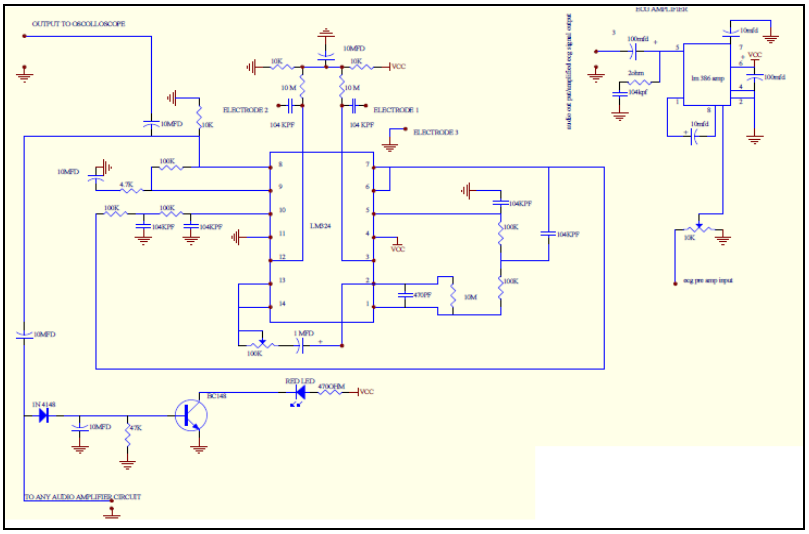


Figure 7. Circuit diagram of the ECG amplifier system

## V. RESULTS AND DISCUSSION

A prototype that incorporates all the above capabilities has been built on a printed circuit board as shown in figure 8. Conventional pre-gelled ECG sensors were used to achieve the ECG signals from the subject. These sensor outputs were connected to the circuit shown and the circuit output was connected to a digital oscilloscope.

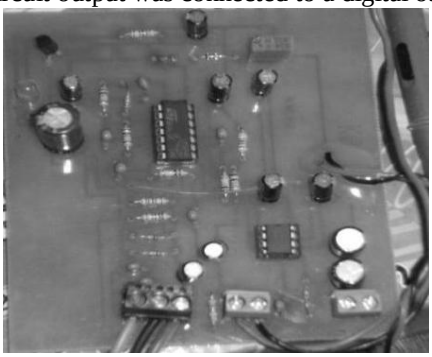


Figure 8. Assembled circuit on a Printed circuit board

Figure 9 shows the ECG signals achieved by the circuit, displayed on the digital oscilloscope. The achieved signals were compared with the signals displayed by commercially available three lead ECG machine of BPL make. The signals of our developed circuitry were found to be on par with the commercially available system.

Figure 9. ECG signals achieved by the circuit as displayed on the digital oscilloscope

## VI. CONCLUSION

The electrocardiogram is a very important clinical diagnostic tool. To measure the ECG signals on the body's surface successfully with all the undesirable signals like the common-mode voltage and noise requires very stable design. The power line interference is a major problem with the commercially available ECG systems. With the proposed design, it is possible to achieve good, noise free ECG signals with a low cost, easy to develop circuit.

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