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Design of Low Power STT - RAM Using Magnetic Tunnel Junction Structure

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Abstract—Spin-torque transfer RAM (STT-RAM), a promising alternative to static RAM (SRAM) for reducing leakage power consumption, has been widely studied to diminish the impact of its asymmetrically long write latency. STT-RAM offers advantages over current memory technologies with its virtually unlimited endurance, low current draw, and small cell size. Additionally, STT-RAM is prone to writing errors due to the relationship between an MTJ's operating temperature and its thermal stability. However, realizing the potential of STT-RAM could lead to a new period of instant-ON technologies, as well as great improvements to battery live and computational speed of current devices.

Index Terms—STT-RAM, MTJ, Spintronics , Non –volatile memory.

I. INTRODUCTION

Memory is one of the most important defining components used in every computer system, storage solution, and mobile device in existence today. Performance, scalability, reliability, and the cost of memory are major criteria in determining the economic success or failure of each system product brought to market.

STT- RAM, however, is well suited for many mainstream applications, particularly as a storage technology, since it delivers the high performance of DRAM and SRAM, has the low power and low cost of flash memory, scales well below 10nm, and leverages existing CMOS manufacturing techniques and processes. Since it is non-volatile, STT-RAM will also retain its data indefinitely when the power is lost or completely turned off.

STT-RAM is an evolution in magnetic storage from hard disk drives to solid-state semiconductor memory. Uses spin-polarized current ("spintronics") to write magnetic bits. Non-volatile, random-access memory with no moving parts and the key building block is the magnetic tunnel junction (MTJ).

Previous conventional wisdom for spin-torque transfer RAM (STT-RAM) is that writes are slower and require more power than their conventional static RAM (SRAM) counterparts. Several architectural solutions, such as hybrid caches with fast and slow writing memory components[2], various methods for preempting, avoiding, and bypassing writes[3] , and leveraging the asymmetry of writing different logic values[4], have been proposed to mitigate the write performance problem. However, due to scaling effects, performance and reliability of STT-RAM reads, not writes, will become the ultimate bottleneck at technologies of 45 nm and below. Read performance, the dominant operation in caches[5], suffers from increased sense amplifier delays for detecting increasingly small sense margins and higher read error rates. In contrast, due to reduced energy barriers at smaller technology nodes, writes will become faster at lower energy, although this leads to higher susceptibility to read disturbance (inadvertent writes from applying a read current).

The primary contribution of this brief is to identify, for the first time, the emerging read performance and stability issue of STT-RAM as the technology node scales. We provide a detailed study on the impact of scaling from 65 to 22 nm, demonstrating a widening performance gap between standard and differential sensing. Furthermore, we present a configurable STT-RAM memory circuit with differential sensing that can selectively operate either in standard mode (S-mode) with a standard slower read performance or in extreme access mode (X-mode) with improved performance and reliability. We demonstrate through a case study that using X-mode in STT-RAM caches can achieve more than 10% improvement in raw performance as well as performance per watt over a design without read optimizations at 22-nm technology.

II. TECHNOLOGY OF STT-RAM

Spin-Transfer Torque RAM (STT-RAM) is an emerging non-volatile memory technology with the potential to be used as universal memory. STT-RAM with a storage-class data retention time is superior as it ensures that all user data will be reliably stored without restriction. Similarly, researchers have proposed using PCM to significantly increase the capacity of main memory, but the schemes have required a large DRAM cache to mitigate the limited write endurance. As for storage devices, using STT-RAM to build this cache would eliminate this limitation. At the other end of the memory hierarchy, the high-performance caches of the microprocessor certainly benefit from the improved density and reduced leakage of STT-RAM. However, performance is reduced when using storage-class STT-RAM, as it requires a large amount of energy to perform writes. By leveraging the fact that the data in the microprocessor caches generally

has a short lifetime, it is possible to mitigate this by using reduced retention-time STT-RAM. Though this may reduce the retention time to one second or less, it can mitigate the write performance and energy penalty associated with STT-RAM caches. The use of a non-volatile memory (NVM) with high performance and endurance, such as STT-RAM, makes it possible to enable a memory hierarchy that has some degree of nonvolatility at each level. This opens new opportunities for optimizing both the performance and energy-efficiency of the system.

A. Overview of Magneto resistive Memory Technologies

STT-RAM is a new, more efficient variant of magneto resistive RAM (MRAM) in which a single bit of data is stored in the magnetic orientation of the free layer of a magnetic tunnel junction (MTJ). MTJs consist of at least two ferromagnetic layers with an oxide barrier (insulator layer) between them, as shown in Figure 1. One of the two magnetic layers is called the hard, pinned, or fixed layer and has its magnetic orientation permanently set during fabrication the other is called the soft or free layer and has a weak magnetic orientation that can be changed dynamically. MRAM and STT-RAM are non-volatile because the free layer does not need an electric current to maintain its orientation.

MRAM never gained significant traction in the memory market due to its extremely high write energy requirements, caused by the use of rotating electric fields to change the 6 free layer state. STT-RAM instead uses the spin-transfer torque effect to switch the free layer, which only requires passing a large electric current directly through the MTJ.

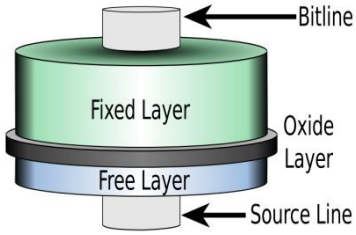

Fig.1 Structure of MTJ

This switching effect behaves according to a thermally-controlled stochastic process, and will be described in more detail in Section B. To minimize the impact of this randomness, the currents used are larger than strictly necessary to ensure reliable operation. Despite this, the write energy and circuit complexity is significantly reduced over MRAM. The presence of the oxide barrier between the ferromagnetic layers creates a noticeable resistance to electric current, dependent on the free layer orientation. When the two layers are oriented in the same direction, the MTJ is in the parallel (P) state and exhibits a low resistance (RP) [Fig. 2(a)]., and when the two layers are oriented in opposite directions, it is in the anti-parallel (AP) state and exhibits a high resistance (RAP) [Fig. 2(b)]. Figures and graphically demonstrate the two free layer states. Reading the state of the MTJ is accomplished by using a small current through the MTJ to estimate the resistance value. Performing a write requires holding the write current for a sufficient amount of time, which is called either the write pulse width or the MTJ write time, to ensure the free layer has changed state.

The low and high MTJ resistances can be used to represent logic values. In a typical 1T1J STT-RAM cell shown in Fig. 2(c), one MTJ is connected with one nMOS transistor, which serves as access controller. This nMOS transistor is typically 1.5 times the size of each of the six transistors that comprise an SRAM cell, leading to the four times density improvement assumed in SRAM replacements with STT-RAM [7].

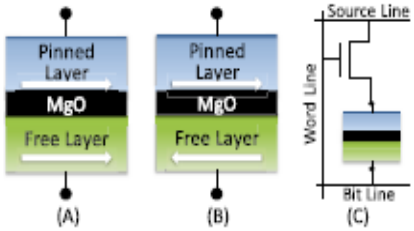

Fig. 2. Illustration of an MTJ and STT-RAM cell.

B. Characteristics of STT-RAM MTJs

When considering the use of MTJs to build STT-RAM memory devices, the most important characteristics are:

(i) The retention time,
(ii) The write latency, and
(iii) The write energy.

All three of these characteristics are interrelated, and it is difficult to change one without affecting the other two. This sectionS provides a foundation for understanding how they interact.

III. READ OPTIMIZATION USING X- MODE

The sensing performance and reliability can be further improved by a better SA design. The sense amplifier was tuned for best possible performance (i.e., the sensing latency). Differential sensing has two main drawbacks [1]. The area required to store a value is doubled, and the dynamic power of write access is also effectively doubled. To efficiently

leverage differential sensing and to minimize these side effects, we propose a configurable differential cell shown in Fig.3. Through a MUX and transmission gate, the cell can be configured into standard high-density mode (S-mode) by comparing the selected cell with *V*ref or in situations where read performance is critical to use extreme performance mode (X-mode) by sensing the voltage difference between adjacent cells[1]. Note that the transmission gate (*Mi*) is shared by multiple bitlines. The direct overhead of each bitline is only four transistors, which is negligible in the STT-RAM design incurring very minimum area overhead in our design. Although such a scheme will increasing the probability of read disturbance, since the read disturbance error is exponential related to the reading current as we mentioned, a small reduction of reading current could significantly reduce the disturbance error. Since this scheme can largely reduce the sensing error, with a smaller reading current, it can also reduced the read disturbance error without sacrificing the sensing error.

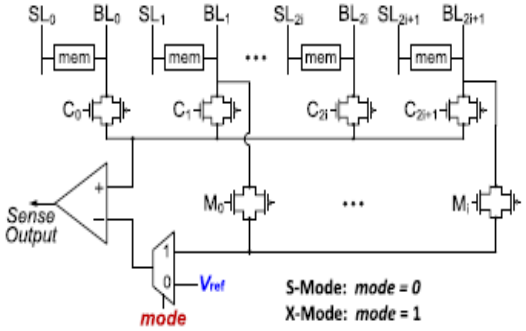

Fig. 3. Reconfigurable extreme mode (X-mode) memory circuit.

IV. SIMULATION RESULTS

In this section the simulation of reconfigurable extreme mode (X-mode)memory circuit using STT RAM is carried out. The resulting waveform for fig.3. is shown below and the power results of this memory is shown in table 1.

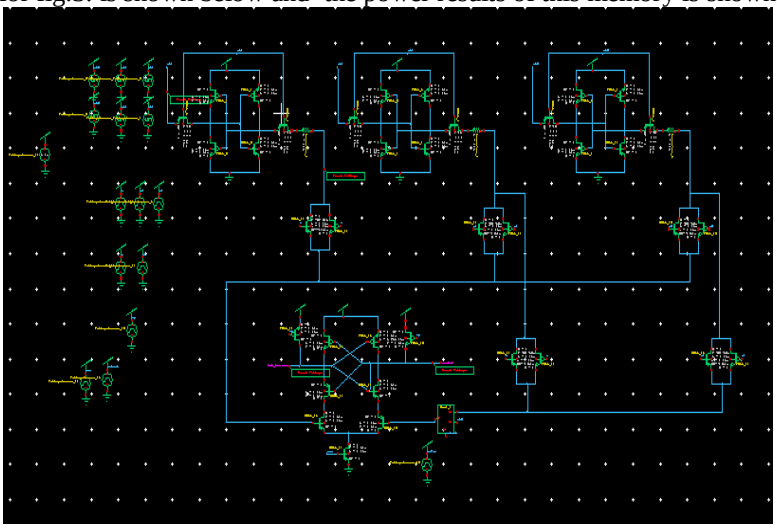

Fig. 4. Reconfigurable extreme mode (X-mode) memory circuit.

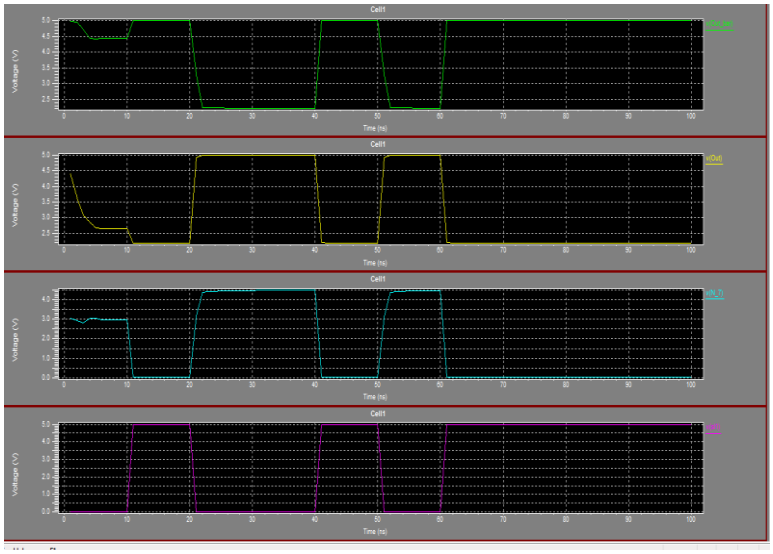

Fig. 5. Simulation results of Reconfigurable extreme mode (X-mode) memory circuit.

Table 1. Power Results

Average power consumed	1.898675e-002 watts
Max power	4.367759e-002
Min power	1.198141e-002

V. CONCLUSION

STT-RAM is a promising type of non-volatile memory, and has potential applications in instant ON technology and data-center power optimization. It has almost unlimited endurance in contrast to flash memory that can only be written a certain number of times before becoming unreliable. Additionally, as no charge moves in an STT-RAM cell, it takes very little power to "write" and "read" information. However, STT-RAM is currently not in production due to persistent challenges. Minute changes in the environment or in the production of a STT-RAM cell can cause large changes in the MTJ resistance as discussed. Additionally, as these cells are exceedingly small, they must be able to withstand ambient thermal disturbances, while allowing cells to accept "write" signals accurately. Ultimately, STT-RAM is extremely versatile as it can be treated as both SRAM and DRAM depending on the logic design. If the "write" current and production issues can be solved, it has the potential to introduce great changes in the present mobile industry and in other consumer electronics by enabling faster logic and longer battery life.

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