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A CMOS VCO for WiMAX Applications

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Abstract —In this study, a current reused voltage-controlled model including one PMOS, one NMOS and one extra NMOS cross coupled pair transistors is presented. When a voltage source ranging from -0.2 to 1.2V is applied to the proposed model, the output frequency varies from 3.78 GHz to 4.57 GHz. The VCO model is designed with 0.18µm CMOS process. The oscillator core consumes 0.83mW for a 1.2V supply. The phase noise at 1 MHz offset with respect to the center frequency is -120 dBc/Hz. The figure of merit for the proposed model isabout -192.35dBc/Hz.

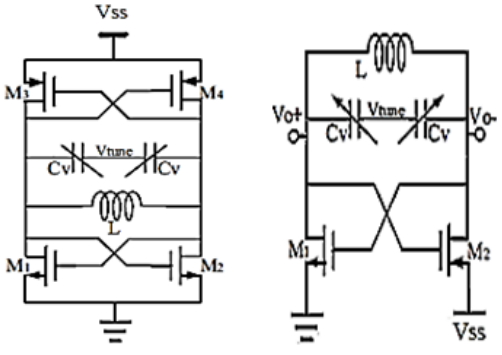
Keywords—Voltage Controlled Oscillator (VCO), Phase noise, Power consumption.

I. INTRODUTION

The WiMAX (mobile word wide interoperability for microwave access) is a wireless communications standard, which is designed for IEEE802.11a WLAN. WiMAX support mobile, nomadic and fixed wireless applications. With the increasing demand for low cost and high integration of wireless transceiver building blocks, a low power and low noise design are of great importance for radio frequency integrated circuit (RFIC) designers. Among the building blocks of the transceiver, the voltage controlled oscillator (VCO) is an important block [1].

Recently VCO using a couple of NMOS and PMOS transistors in the cross-connected pair as a negative conductance generator has been presented [2]. The series stack of N-and PMOSETs allow supply current to be reduced by half that of the conventional LC-VCO [1],[2]. In this study, both a conventional current-reuse model and a conventional current-reuse model integrated with NMOS cross-coupled pair are studied. As well, two resistors are added to drain and source to the latter model to improve the magnitude symmetry of output signal [3]. Finally, for noise reduction, three capacitors are paralleled with the two resistors and the NMOS transistor. In addition, a modified current LC-VCO comprising cross-connected pair transistors M1, M2 and LC-tank is proposed where there is only one DC path for supply current. Fig. 1(a) shows a conventional complementary cross-couple LC VCO, which uses four active device M1~M4 to provide negative conductance for LC tank loss compensation. During the first half period of oscillation, M1,M4 are on and M2,M3 are off, and during the second half period M2,M3 are on and M1,M2 are off and currentflows intheLC tank [2].However, as shown in Fig. 1(b), a current reuse VCO is introduced in which a negative conductance is created by the cross-connected pairs of transistors PMOS and NMOS to compensate for the losses in the LC tanks. NMOS and PMOS transistors allow current consumption to be reduced by half compared to that of the conventional cross coupled VCO shown in Fig. 1(a).

The rest of the study is organized as follows. Section II presents the design method for the proposed current-reuse VCO. Circuit simulation results are illustrated in section III. Finally, the conclusion is provided in section IV.

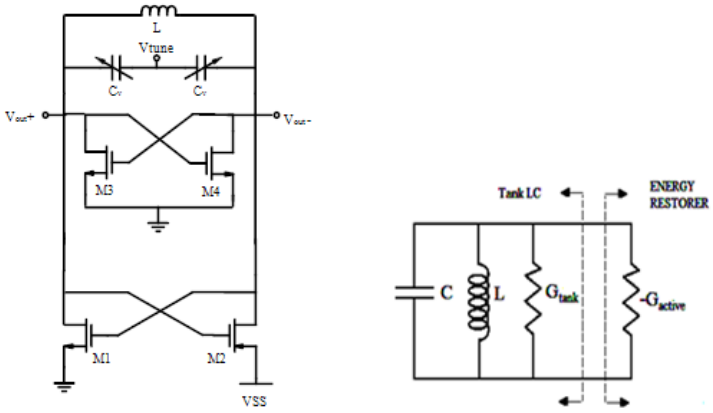


(a) (b)

Fig. 1 (a) Conventional cross- coupled VCOand (b) Conventional current reuse VCO [1].

II. CIRCUIT DESIGN

The circuit schematic of the proposed current-reuse VCO is shown in Fig. 2(a) As can be seen, the topology consists of two mainly transistors PMOS and NMOS with an additional NMOS cross-couple pair (compared to Fig.1 (a)) that causes an increase in the conductivity of the circuit resulting in smaller current consumption compared to the one in conventional current-reuse VCO [4]. As well, it compensates for the passive element loss of the LC tank and improves oscillator stability.



(a) (b)

Fig. 2 (a) Conventional Current Reuse VCOwith additional NMOS cross coupled , (b) Generic LC –VCO

The general concept of an LC oscillator is shown in Fig. 2 (b), where G_{active} and G_{tank} are the admittances of energy restorer and tank, respectively. The tank filters the non-sinusoidal current signal coming from the active circuit and delivers a sinusoidal voltage in its terminals. The oscillation occurs when conductance of the LC tank is compensated by that of the active circuit transistors. For similar M3 and M4 transistors sizes, the circuit conductance is as follows:

$$G_{m(active)} = -\left(\frac{g_{m,3}}{2} + \frac{g_{m,n}.g_{m,p}}{g_{m,n}+g_{m,p}}\right) \quad (1)$$

Quality factor Q is an important parameter in a LC-tank. The tank circuit consists of a spiral inductor and varactor components. The overall Q-factor of the LC-tank is given by:

$$\frac{1}{Q_T} = \frac{1}{Q_L} + \frac{1}{Q_C} \quad (2)$$

In most cases the quality factor of a varactor much higher than that of a spiral inductor, hence it can be neglected and Eq.(2) can be rewritten as :

$$Q_T \approx Q_L = \frac{R_{L,par}}{2\pi f L} \quad (3)$$

The conductance of an LC-tank can be determined by:

$$G_{tank} \approx G_{L,par} = \frac{1}{2\pi f Q_L R_{L,par}} \quad (4)$$

Consequently, the start-up condition for oscillation can be expressed by:

$$G_{m(tank)} + G_{m(active)} \le 0 \quad (5)$$

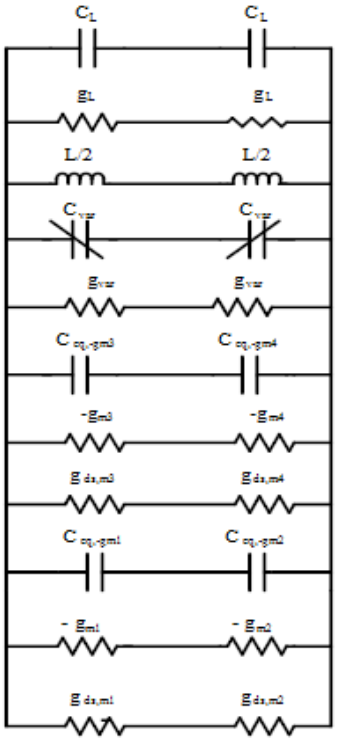


Fig. 3 Equivalentcircuitofthe current-reuse VCO core circuit.

The proposed model of the VCO topology including a current-reuse block, parasitic varactors, and a inductor is shown in Fig. 3. Usually the conductances g_{ds} and g_{var} are low as compared to g_L and can be neglected. Theoscillation frequency can be given by:

$$f_{osc} = \frac{1}{2\pi\sqrt{L\,C_{total}}} \quad (6)$$

Therefore, the total equivalent capacitance of the Fig. 3 is as follows:

$$C_{total} = \frac{C_{var}}{2} + \frac{C_L}{2} + \frac{C_{eq,-gm3}}{2} + \frac{C_{eq,-gm1}\,.\,C_{eq,-gm2}}{C_{eq,-gm1} + C_{eq,-gm2}} \quad (7)$$

The circuit structure shown in Fig. 2(a) is asymmetrical, and this may result in different power consumptions and high phase-noise in the differential output parts. To solve these problems, additional resistors [1] (r_1 and r_2 as shown in Fig. 4) are employed and M5 and M6 are biased in the triode region. The sizes of M5, M6 determined so that a symmetrical oscillation waveform can be achieved is given by:

$$V_{out}^{+} = V_{out}^{-} \quad (8)$$

$$g_{m1}(Z_{OUTN} \parallel Z_{tank}) = g_{m2}(Z_{OUTP} \parallel Z_{tank}) \quad (9)$$

Voltages supplied to M5 and M6 are V_1=1 and V_2=0.1, respectively.

Capacitances C1, C2 and C3 are parallel-connected with M3, M4, M6 to reduce the effects of the resistances, to adjust the load impedances of the output ports, and to improve the performance of the oscillator. Fig. 5 shows the effect of the capacitors C1, C2 for further lowering of the phase noise. Their sizes are calculated by:

$$Z_{in} = \frac{-2}{g_m - (C+C_{gs})\,jw} = \frac{-2g_m}{g_m^{\,2} + (C+C_{gs})^2 w^2} + j\,\frac{-2w(C+C_{gs})}{g_m^{\,2} + (C+C_{gs})^2 w^2} \quad (10)$$

The Q of proposed VCO is as following:

$$Q \approx \frac{1}{G_{total}}\sqrt{\frac{C_{total}}{L}} \quad (11)$$

and

$$G_{total} \approx G_{loss} + G_p - G_{m,active} \quad (12)$$

where G_{loss} , G_p are the parasitic losses conductance of inductor L and transistors, respectively.

In Eq.10 the input impedance (Real Part) is reduced by added capacitors and therefore, the negative conductance of oscillator increases. Therefore according toEq.12 G_{total} is reduced. As well, LC tank quality factor (Eq.11) increases which will lead to the improved phase noise.

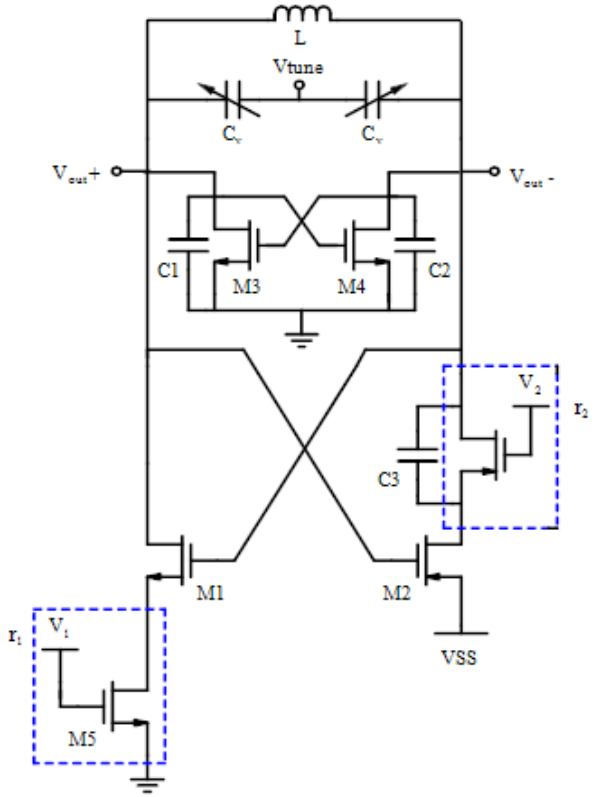


Fig. 4 Proposed current- reused VCO.

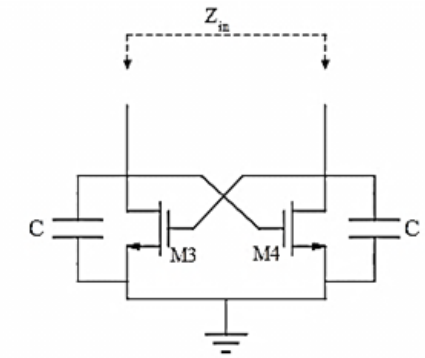


Fig. 5 NMOS core with additional capacitors.

III. SIMULSTIONRESULTS

The proposed VCO was designed using the TSMC 0.18µm technology and simulated by Advance Design System (ADS). The power consumption of the VCO core is 0.83 mW for a 1.2V supply voltage. Fig 6(a) and 6(b) show the positiveandnegativeoutput waveformsand thedifferentialoutputs. The MOS varactor capacitance, over the tuning voltage is shown in Fig 7. Fig 8 shows the simulation tuning range, the VCObands are adjusted by a controlled voltage supply ranging from -0.2v to 1.2v and frequency band are from 3.78 to 4.57GHz.

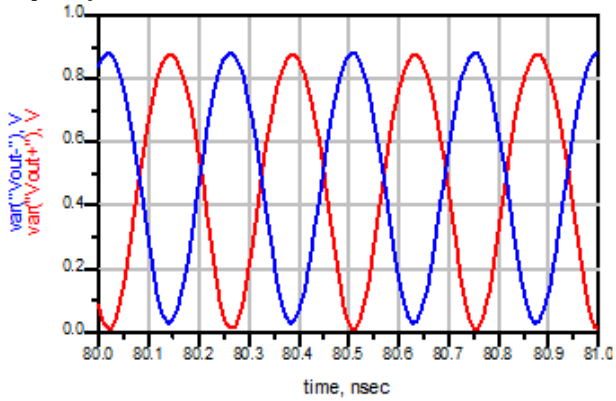


Fig. 6 (a) Output waveform V_{out}^{+} and V_{out}^{-} .

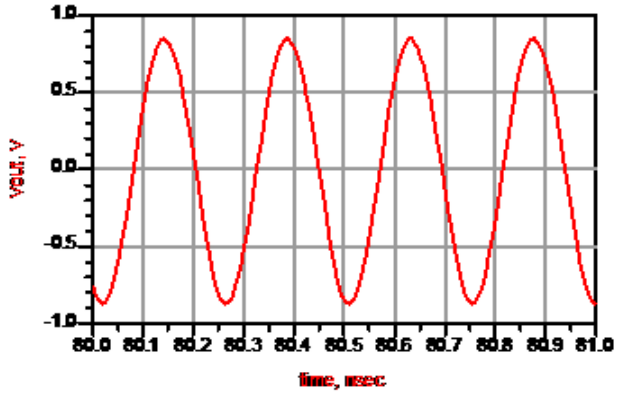


Fig. 6 (b) Output waveform differential.

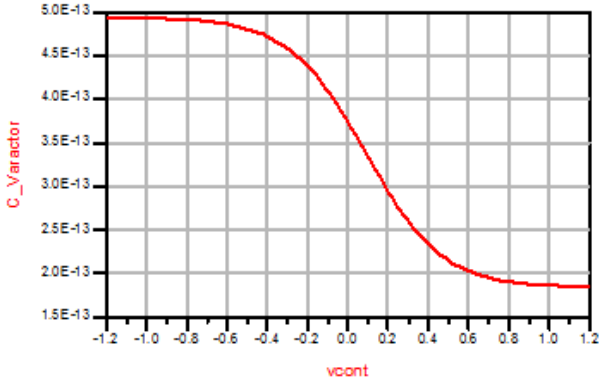


Fig. 7 Capacitance variation versus tuning voltage.

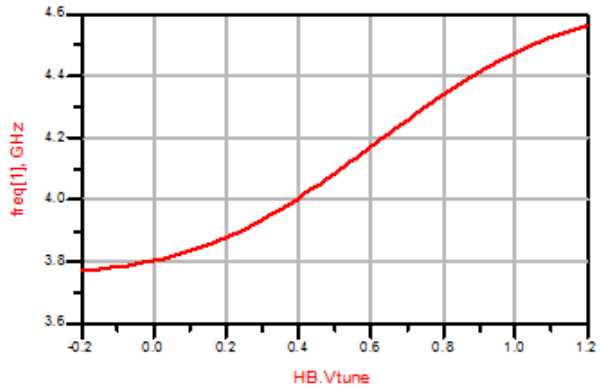


Fig. 8 Simulation result for output frequency versus tuning voltage.

Fig 9 depicts the simulation result for phase noise for the proposed VCO, which is about -99 to -120 dBc/Hz at 100KHz to 1MHz offset frequency. The measure used for comparing different VCOs is figure of merit that is defined by [5],[6]:

$$FOM = L(f_c) - 20\log\left(\frac{f_o}{f_c}\right) + 10\log\left(\frac{p_{dc}}{1mw}\right) \quad (13)$$

where $L(f_c)$ is the phase noise, f_c is the offset frequency, f_o is the oscillating frequency and p_{dc} is power consumption. According to Eq. 10, the FOM of the proposed VCO is -192.35dBc/Hz. Table I presents the performance of the proposed VCO and other references.

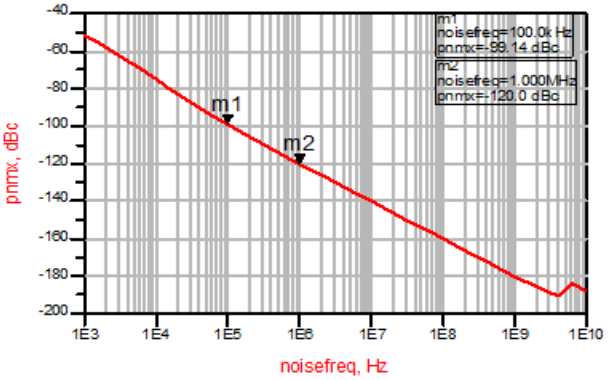


Fig. 9 Simulation result forphase noise of the VCO.

IV. CONCLUSION

The proposed VCO is designed in TSMC 0.18 µm CMOS technology. It allows the current consumption to be reduced by half, therefore power consumption will be reduced in comparison with conventional cross-coupled and previously studied current- reuse VCOsas presented in Table 1. To solvethe asymmetryoutput waveform problem, tworesistances are added to the drainsandsources of transistors. Simulation results yield the phase noise -120 dBc/Hz at 1 MHz offset from center frequency. The power consumption of the oscillator for a 1.2V supply is 0.83mW .The output frequencies range from 3.78 GHz to 4.57 GHz. The phase noise at 1 MHz offset with respect to the center frequency is -120 dBc/Hz. The studied model's figure of merit is about -192.35 dBc/Hz.

TABLE I COMPARISON PERFORMANCES OF PROPOSED VCO WITH PERVIOUS WORKS

Ref.	Process	Supply voltage (V)	Freq. (GHz)	Tuning Range	Core Power (mW)	Phase Noise@1MHz (dBc/Hz)	FOM@1MHz (dBc/Hz)
[1]	0.18-µm CMOS	1.4	5	14.7%	2.5	-118	-188.6
[4]	0.18-µm CMOS	1.6	10	7.1%	11.53	-106.9	-182.4
[7]	0.18-µm CMOS	1.2	5.6	10.6%	2.4	-119.13	-190.29
[8]	0.18-µm CMOS	1.4	5.8	15.8%	0.99	-115.88	-191
[9]	0.18-µm CMOS	1	5.5	15.31%	5.6	-105.83	-173.21
This Work	**0.18-µm CMOS**	**1.2**	**4.17**	**19%**	**0.83**	**-120**	**-192.35**

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