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Analysis of Shift Registers Using Pulsed Latch

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Abstract--In the world of Integrated Circuits, Complementary Metal–Oxide–Semiconductor (CMOS) has lost its credentiality during scaling beyond 32nm. Scaling causes severe Short Channel Effects (SCE) which are difficult to suppress. As a result of such effects, many alternate devices have been studied. Some of the major contestants include Multi Gate Field Effect Transistor (MuGFET) like FinFET, Nano tubes, Nano wires etc. Among these, Carbon Nanotube play a vital role in modern electronic design. In this paper, the CMOS transistors present in the single edge triggered D Flip Flop based shift registers is replaced by CNTFETs and the performance of shift registers built by 32nm CNTFET technology is compared with CMOS based shift registers at 32nm technology using HSPICE simulation tool.

Keywords: CNTFET, D Flip flop,FinFET, MuGFET, SCE, shift registers.

I. INTRODUCTION

Flip flops are the basic storage elements used extensively in all kinds of digital designs. As the feature size of CMOS technology process scaled down according to Moore's Law, designers are able to integrate many numbers of transistors onto the same die. The more transistors there will be more switching and more power dissipated in the form of heat or radiation. Heat is one of the phenomenon packaging challenges in this epoch, it is one of the main challenges of low power design methodologies and practices. Another driver of low power research is the reliability of the integrated circuit. More switching implies higher average current is expelled and therefore the probability of reliability issues occurring rises. We are moving from laptops to tablets and even smaller computing digital systems. With this profound trend continuing and without a match trending in battery life expectancy, the more low power issues will have to be addressed. The current trends will eventually mandate low power design automation on a very large scale to match the trends of power consumption of today's and future integrated chips[3]. Power]consumption of Very Large Scale Integrated design is given by generalized relation, $P = CV^2f$ [1]. Since power is proportional to the square of the voltage as per the relation, voltage scaling is the most prominent way to reduce power dissipation. However, voltage scaling is results in threshold voltage scaling which bows to the exponential increase in leakage power. Though several contributions have been made to the art of single edge triggered flip-flops, a need evidently occurs for a design that further improves the performance of single edge triggered flip-flops[2].

The flip flops are cascaded to form the shift register which shares the same clock, the output of each flip-flop is given as the "data" input to the next flip-flop due to which bit shifting take place. More generally, A shift register may be multidimensional, where data in and data out are in the form of bit array. Several shift register of same length are connected to form this bit array. Shift registers can have both parallel and serial inputs and outputs. There are also types that have both serial and parallel input and types with serial and parallel output. Shift registers are a type of sequential logic circuit, mainly used for storage of digital data. As the flip flops are cascaded the output of one flip flop is provided as the input for other. All flip-flop is driven by a global clock. There are four types of shift registers available but in this paper only Serial In - Serial Out shift register is considered. The storage capacity of a register is the total number of bits (1 or 0) of digital data it can retain. Each stage (flip flop) in a shift register represents one bit of storage capacity. Therefore the number of stages in a register determines its storage capacity.

II. COMPLEMENTARY METAL OXIDE SEMICONDUCTOR (CMOS)

The MOSFET is used in digital complementary metal–oxide–semiconductor (CMOS) logic, which uses p- and n-channel MOSFETs as building blocks. Overheating is a major concern in integrated circuits since ever more transistors are packed into ever smaller chips. CMOS logic reduces power consumption because no current flows (ideally), and thus no power is consumed, except when the inputs to logic gates are being switched. CMOS accomplishes this current reduction by complementing every nMOSFET with a pMOSFET and connecting both gates and both drains together. A high voltage on the gates will cause the nMOSFET to conduct and the pMOSFET not to conduct and a low voltage on the gates causes the reverse. During the switching time as the voltage goes from one state to another, both MOSFETs will conduct briefly. This arrangement greatly reduces power consumption and heat generation. In this paper section II discuss about D flip flop and pulsed latch using CMOS and section III describes the CNTFET based D flip flop and pulsed latch. section IV describes the conclusion.

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A. CMOS based SET D Flip Flop

SET D-flip flop is designed from power pc603 SET D-FF . The CMOS based flip flop design is shown in Fig.1 .This flip-flop is a Master Slave flip flop structure and it consists of two data paths. As conventional n-type pass transistors give weak high output, but in this design the n-type pass transistors are followed by an inverter to give strong high output. Hence the SET D-Flip Flop is free from threshold voltage loss. Thus the designed Single Edge Triggered D-Flip-Flop has become more efficient in terms of area, power and speed and hence provides better performance than conventional Flip Flops.

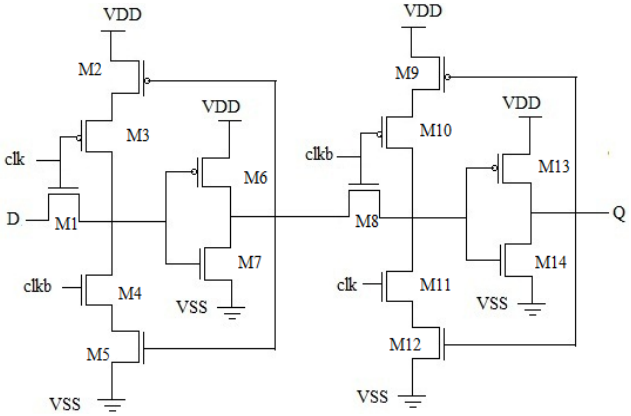

Fig 1. SET D Flip Flop

B. CMOS based Pulsed Latch

CMOS is the most popular MOSFET technology. Here the SSASPL pulsed latch is realized using the CMOS logic which is shown in fig.2. The SSASPL consists of 15 transistors in which the transistors (M1-M8) are used to generate the pulsed clock signal and the transistors (M9-M15) are the schematic of SSASPL [15].

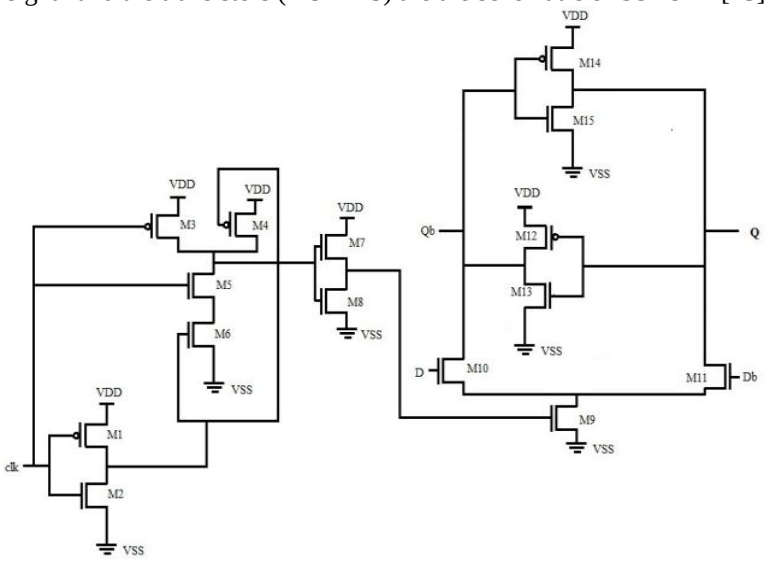

Fig. 2 CMOS based SSASPL

The pulsed clock signal generation circuit consists of AND gate, inverter and clock buffer. The clock signal is given to the inverter which inverts the signal and then the inverter output is given to one input of AND gate and another input is the clock signal which performs the AND operation. The output is given to the clock buffer which stores the data and given to the transistor M9 as the pulsed clock signal.

The total size of the clock buffers is determined by the total clock loading of latches. The SSASPL updates the data with three NMOS transistors and it holds the data with four transistors in two cross-coupled inverters. It requires two differential data inputs (D and Db) and a pulsed clock signal. When the pulsed clock signal which is given to the gate of the transistor M9 is high, its data is updated. The node Q or Qb is pulled down to ground according to the input data (D and Db). The pull-down current of the NMOS transistors must be larger than the pull-up current of the PMOS transistors in the inverters. The power is consumed mainly in latches and clock-pulse circuits. Each latch consumes power for data transition and clock loading.

III. CNTFET: CARBON NANO TUBE FIELD EFFECT TRANSISTOR

CNT is a carbon allotropic variety which comes from the fullerenes family. It is made of nano sized carbon atom and rolled in seamless cylindrical form of single atomic layered thick graphene sheet [4]. Fig. 3 (a) shows a CNT which is made from one sheet of graphene rolled in cylindrical structure which is called Single Wall Carbon Nanotube (SWCNT) and Fig. 3 (b) shows Multi Walled Carbon Nanotube (MWCNT) where multi-layers of graphene are rolled as

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a concentric tube [5-7]. CNT based nano devices are comprised of wide range of nano structures. CNTFET could be used as valve or controlled switch in electronics. Carbon Nano Tube Field Effect Transistors for NEMS are emerging day by day not only in IC industry but also in medical science, mechanical system, automobile industry and recreational instruments [8].

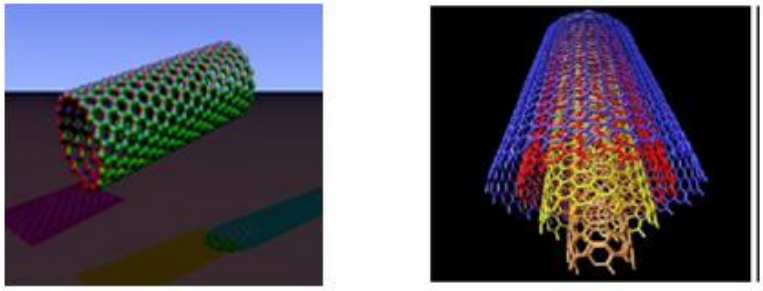

Fig.3 a) SWCNT (b) MWCNT [14].

Depending on their chirality (i.e., the direction in which the graphite sheet is rolled), the single-walled carbonanotubes can either be metallic or semiconducting [9], [10]. CNFETs are one of the molecular devices that avoid most fundamental silicon transistor restriction and have ballistic or near ballistic transport in their channel [11],[12]. Therefore a semiconductor carbon nanotube is appropriate for using as channel of field effect transistors [10]. Applied voltage to the gate can control the electrical conductance of the CNT by changing electron density in the channel.

By using appropriate diameter suitable threshold voltage for CNFET can be achieved. The threshold voltage of the CNFET is proportional to the inverse of the diameter of CNT and can be expressed as:

$$V_{TH} = \frac{0.42}{d(nm)} \quad \text{------- (1)}$$

For a CNT with (n, m) as chirality and as lattice (that is carbon to carbon atom distance) the diameter is [13]:

$$D_{CNT} = \frac{a\sqrt{n^2 + nm + m^2}}{\pi} \quad \text{------- (2)}$$

CNTFETs are having similar properties to that MOSFETs. A single wall CNT consists of only one cylinder which is a promising alternative for the MOSFET. An CNT can be either semiconductor or metallic depending on its rolling and the chiral angle.

A. Nanotube Geometry

There are three unique geometries of carbon nanotubes. The three different geometries are also referred to as flavors. The three flavors are armchair, zig-zag, and chiral [e.g. zig-zag (n, 0); armchair (n, n); and chiral (n, m)]. These flavors can be classified by how the carbon sheet is wrapped into a tube is shown in Fig.4

A1. Zigzag

The length L of the chiral vector Ch is directly related to the tubule diameter d. The chiral angle 0 between the Ch direction and the zigzag direction of the honeycomb lattice (n,O)[14]. The zig-zag model is the easiest one to count and the best one to try and copy when learning these geometries. Remember, our goal is to start and end at the same point. Hold the starting point between the finger and thumb of one hand (0,0) and use the other hand to count around the rolled up sheet and try to end where you begin. So, count each carbon atom around the tube - (1, 0) (2, 0) (3, 0) (4, 0) (5, 0) etc., until you get back to the starting point. Once you have done this, you have just made a simple carbon nanotube model. The chiral angle in zigzag is zero.

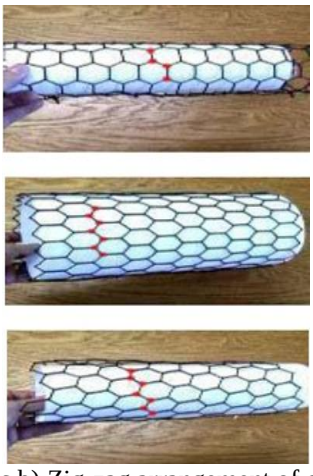

Fig.4 a)Armchair arrangement of carbon atoms b) Zig-zag arrangement of carbon atoms c) Chiral arrangement of carbon atoms.

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A2. Armchair

When you count around the tube, note that you are counting at an angle and it will not be possible to get back to your starting point unless you turn a corner. Note that you have to pick the right place to turn so that you end up at your starting point because you can only turn once. Again, count each carbon atom around the tube - (1, 0) (2, 0) (3, 0) (4, 0) (5, 0) until you get to a corner; after you turn, the count continues as - (5, 1) (5, 2) (5, 3) (5, 4) etc. - until you get back to the starting point. The chiral angle in armchair is 30 degree.

A3. Charial

The last one is the chiral model. I think it is the most difficult to copy. It can be counted similarly like the armchair model because it also has a turn it. Remember to try and end up where you start such that the charial angle fomed will be between 0 and 30 degree. The parameter of CNTFET is shown in the table I

Table I Nominal process parameters of CNTFET model

Parameter	Value
Supply Voltage (V_{DD})	1.0v
Physical channel length (L)	32nm
Diameter of the CNT (d)	1.487nm
The length of doped CNT source-side extension region. (L_{SS})	32nm
The length of doped CNT drain-side extension region.(L_{DD})	32nm
The thickness of high-k top gate dielectric material (T_{OX})	4nm
The dielectric constant of high-k top gate dielectric material (K_{OX})	16
The distance between the centers of two adjacent CNTs within the same device.	20nm
Chiral Vector	(19,0)

B.CNTFET based SET D Flip Flop

Carbon Nanotube Field Effect Transistor (CNTFETs) is considered as a most promising device, which is an alternative for CMOS transistors in future nanotechnology because of its excellent current capabilities, ballistic transport operation and its superior thermal conductivities. CNTFET is the efficient one to reduce the consumption of power.so the flip flops are designed using the carbon nanotube field effect transistor.

The CNTFET based SET D flip flop design is shown in fig. 5 which is designed from power pc603 SET D-FF. An edge-triggered flip-flop achieves control the clock signal by combining in series a pair of latches. The positive edge triggered D flip-flop where two D latches are connected in series and a clock signal Clk is connected to the E input of the latches, one directly, and one through an inverter. The first latch is called the master latch.

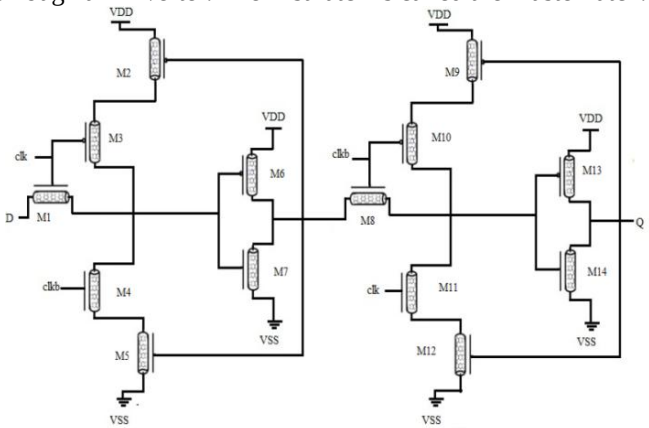

Fig.5 CNTFET based SET D Flip Flop

The master latch is enabled when Clk = 0 and follows the primary input D. When Clk is a 1, the master latch is disabled but the second latch, called the slave latch, is enabled so that the output from the master latch is transferred to the slave latch. The slave latch is enabled all the while that Clk = 1, but its content changes only at the beginning of the cycle, that is, only at the rising edge of the signal because once Clk is 1, the master latch is disabled and so the input to the slave latch will not change. This is called a positive edge-triggered flip-flop because the output Q on the slave latch changes only at the rising edge of the clock.

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C. CNTFET based pulsed latch

CMOS based SSASPL is replaced by the CNTFET based SSASPL [15] i.e. the NMOS and PMOS are replaced by NCNTFET and PCNTFET which is shown in fig. 6.

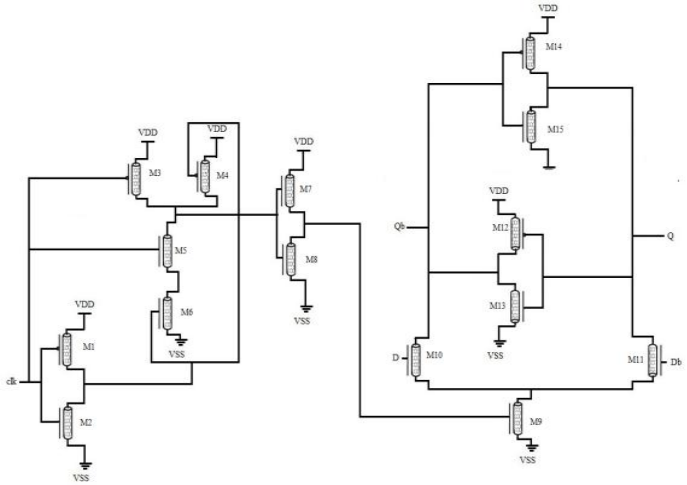

Fig. 6 CNTFET based SSASPL

The CNTFET (M1-M8) is used to generate pulsed clock signal. The pulsed clock signal is given to the M9 of SSASPL circuit. The SSASPL consists of three NCNTFET and the two inverter (i.e., two NCNTFET and two PCNTFET) which is cross coupled.. The output is taken from the two cross coupled inverter of SSASPL i.e., between one CNTFET inverter M11, M12 and another inverter M14, M15. The operation of CNTFET based SSASPL is same as that of CMOS based SSASPL.

IV. CONCLUSION

CNTFET is the ongoing technology in today's world. CNTFET consumes less power than the CMOS. Here the pulsed latch and D Flip Flop are discussed in which the pulsed latch consumes less power than the flip flop. The future work of designing the shift registers are going to be done using the pulsed latch.

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