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Clock Zone Based QCA Adder Architecture Design

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Abstract- Quantum-dot Cellular Automata (QCA) is considered as an advanced technology compared to complementary metal-oxide-semiconductor due to QCA's merits. In QCA the basic boolean primitive is the majority gates. In majority and inverter operation is used to design majority gate, inverter gate logic and adder architecture. This work is to reduce the adder architecture complexity compared to CMOS adder design. Adder architecture is the important block in more type of digital core architecture and is used to control the system functionality. Many logical circuits are designed using QCA which consume low power and with reduced area. This work concentrates on the design of adder using QCA DESIGNER.

Keywords: Quantum- dot cellular automata, Full adder, Carry save adder, Majority gate, Inverter

I. INTRODUCTION

Nanotechnology is a promising future for designing Quantum-dot cellular automata (QCA).Comparing to CMOS technology QCA is very effective it take less time. CMOS technology cannot be further scaled down due to several reasons like sub-threshold leakage, fabrication costs, short channel effects and interconnect delay etc [1]. QCA technology provides a capable opportunity to overcome the imminent limits of conventional CMOS technology. For this reason, in recent years the design of logic circuits based on QCA has received a great compact of attention, and special efforts have been directed towards arithmetic circuits, such as adders .multipliers and comparators [2] .Devices based on quantum-mechanical principles hold the guarantee of faster speeds and greatly reduced sizes. Most quantum device designs examined have been similar to usual device implementations in that they use currents and voltages to encode information. Digital computers and calculators consist of arithmetic and logical circuits that add, subtract, multiply and divide binary numbers.

The basic QCA cell, that is capable of representing a logical bit, occupies nano-scale area. A primitive QCA cell commonly contains two electrons, whose two possible coulomb repulsion placements represent "1" and "0" [1]. The electron are used to store and transmit the data. These electrons are transmit through tunneling junction. Due to the repelling force the electrons moves to opposite corners of the quantum cell, resulting in two possible arrangements representing binary 0 and 1. A QCA design are partitioned the clock zones that are gradually associated with four clock signals.

II. BASIC PRELIMINARIES

Quantum-Dot Cellular Automata

QCA is a square nanostructure. Each cell has four quantum dots. The cell can be charged with two free electrons shown in FIG 1 .Electron transmission occurs on columbic interaction. QCA do not use transistors. QCA size is smaller than CMOS it can be implemented in molecule or atom size [1],[2]. QCA power consumption is extremely lower than CMOS because there are not any current in the circuit. QCA cell design considers the distant between Quantum dots to be about 20nm, and a distance between cells of about 60nm.

logic 0 logic1

FIG.1. QCA cell

Quantum dot is a nanometer sized structure that is capable of trapping electrons in three dimensions. Quantum dots become the backbone of future electronics and photonic devices because of their unique properties due to quantum confinement of electrons in three dimensions [2],[3].

In Quantum cell clock phases define the flow of information into the circuit. By the clocking mechanism, the electron can tunnel through to neighboring cells during the clock transistion by the interaction between electrons. The behaviour of each cell in a circuit is controlled by a clock signal.

A. QCA gates

There are two primary QCA gates

1. QCA Inverter(QI)

The QCA cells can be used to form the primitive logic gates [3]. The simplest design of inverter is shown in FIG 2.

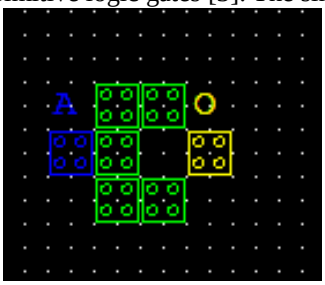

FIG. 2.Inverter

2. QCA Majority(QM) gate

Important primary QCA gate realizes the three input majority function. Majority gate with three inputs and one output are shown in FIG 3. In this structure, the electric field effect of each input on the output is indistinguishable and preservative, with the whichever input state(binary 0 or binary 1) is in the majority becomes the state of the output cell [4]. For example, if inputs A and B exist in a "binary 0" state and input C exists in a "binary 1" the output will exist in a "binary 0" state since the combined electrical field effect of inputs A and B together is greater than that of input C.

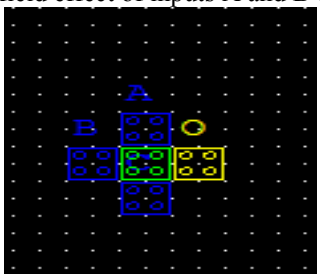

FIG. 3.Majority Gate

A QM gate with one input fixed to "0" or "1" acts as an AND or OR gate, respectively. Therefore, the combination of QM and QCA inverter make a complete logic set.

B .Crossover (QX)

The collection of two intersecting wires is known as a crossover.

1. Multi-layer crossover

Multilayer crossover uses more than one layer of cells(analogous to multiple metal layers in a conventional IC). Multilayer QCA circuits can potentially consume less area. This QX architecture uses two substrate layers to avoid interference [1].

2. Coplanar crossover

Single layer designs are possible with QCA because of the ability to create coplanar crossover. Coplanar crossover using two cell types Regular and Rotated. In rotated cell the Quantum dots rotated by 45degree [5]. The majority of designs employ the coplanar due to its simplicity.

C. QCA clock

In each clock zone, the clock signal has four states: high-to-low, low, low-to-high and high. The cell begins computing during the high-to-low state and holds the value during the low state. The cell is released when the clock is in the low to high state and inactive during the high state. The QCA clocking signal is used to control the signal propagation along the QCA cells arrangement. There are four different clocking phases such as switch, hold, release and relax [6].

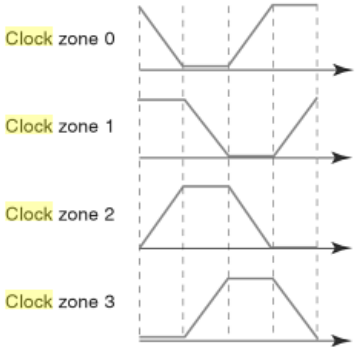

FIG. 4 . Four phases of the QCA Clock

With zone clocking, all the cells in a design are grouped into one of four available clocking zones; that is, all the cells in a particular clocking zone are connected to one of the four available phases of QCA clock shown in FIG 4. A wire, which clocked from left to right with increasing clock zones, will propagate information in the same direction. As a result, QCA circuits are pipelined at the clock zone level. This also permits more than one bit of information to be present on a particular wire [6]. QCA Designer has been developed around this particular approach to clocking.

D. QCA fabrication technologies

QCA cells are realized within different fabrication technologies ; namely Metal Island, Semiconductor, Molecular, and Magnetic [9]. The advantage of Molecular implementation include very high switching speeds, highly symmetric QCA cell structure [7].

III. NEW QCA FULL ADDER

Three Majority gates and two inverters can be used to design full adder architecture design. The clock zones of vertical and horizontal wires are marked with 2 and 0, respectively, except for the central cell, which is unmarked [1],[8].

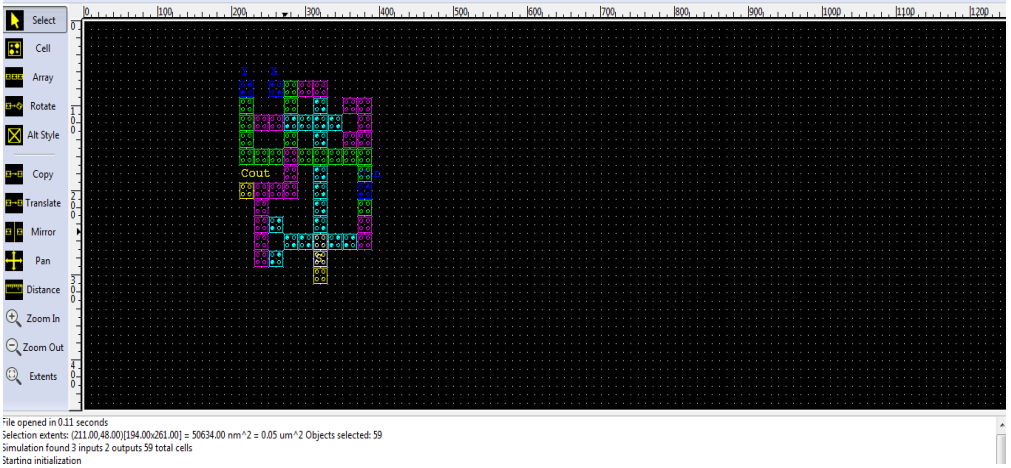

FIG.5. QCA Designer layout

The one level layout of QCA Full Adder (QFA) is shown in FIG 5. Simulation found 3 inputs, 2 outputs and 59 total QCA cells. The total area occupied by QFA is 0.05μm^2 which is displayed below the simulation window.

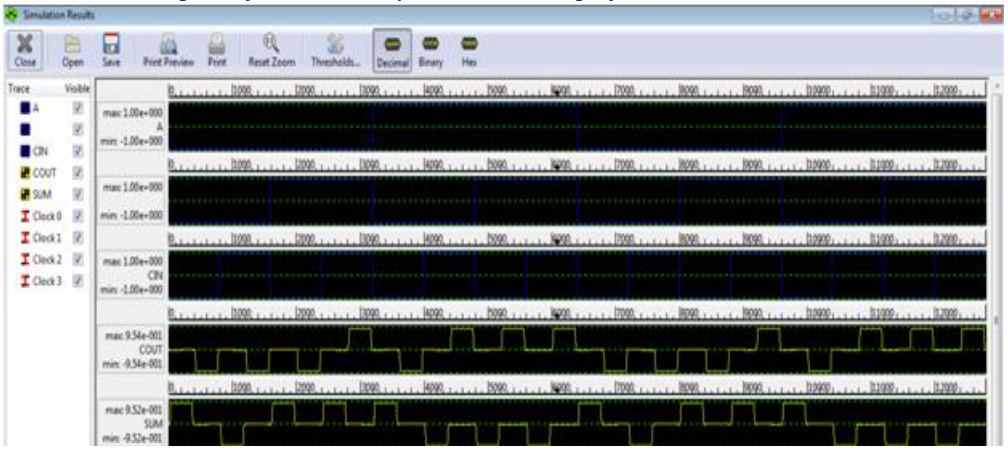

FIG .6 . Input /Output waveform for QFA

IV. CONCLUSION

The transistor logic is modified to quantum logic. The single atom quantum dots measure less than one nanometer in diameter and enable unprecedented control over single electrons. Cost of the proposed QFA design is far less than all the previous QCA adders [9],[10]. This architecture is to improve the system performance level compare to existing CMOS design methodology. The cell count of QFA is reduced hence the area is minimized.

REFERENCES

[1] D. Abedi, G. Jaberipur, and M. Sangsefidi ,"Coplanar Full Adder in Quantum-Dot Cellular Automata via Clock-Zone Based Crossover" IEEE Transactions on Nanotechnology 2015.

[2] Stefania Perri, Pasquale Corsonello ," Design of Efficient Binary Comparators in Quantum-Dot Cellular Automata" IEEE Transactions on Nanotechnology 2013.

[3] J. Huang, M. Momenzadeh, M. B. Tahoori, and F. Lombardi, "Defect characterization for scaling of qca devices [quantum dot cellular automata]," in Defect and Fault Tolerance in VLSI Systems, 2004. DFT 2004. Proceedings. 19th IEEE International Symposium on. IEEE, 2004, pp. 30–38.

[4] Santanu Santra, Utpal Roy ,"Design and Implementation of Quantum Cellular Automata Based Novel Adder Circuits" International Journal of Computer, Electrical, Automation, Control and Information Engineering Vol:8, No:1, 2014.

[5] P. D. Tougaw and C. S. Lent, "Logical devices implemented using quantum cellular automata," Journal of Applied physics, vol. 75, no. 3, pp. 1818–1825, 1994.

[6] Namit Gupta and Nilesh Patidar, Sumant Katiyal, K. K. Choudhary , " Design of Hybrid Adder-Subtractor (HAS) using Reversible Logic Gates in QCA" International Journal of Computer Applications (0975 – 8887) Volume 53– No.15, September 2012 .

[7] Lu, Yuhui, Mo Liu, and Craig Lent. "Molecular quantum-dot cellular automata: From molecular structure to circuit dynamics." *Journal of applied physics* vol. 102, no. 3, p. 034311, 2007.

[8] Momenzadeh, Mariam, Marco Ottavi, and Fabrizio Lombardi. "Modeling QCA defects at molecular-level in combinational circuits." Defect and Fault Tolerance in VLSI Systems, 2005. DFT 2005. 20th IEEE International Symposium on. IEEE, 2005.

[9] Weiqiang Liu, Liang Lu, M´aire O'Neill, A First Step Toward Cost Functions for Quantum-Dot Cellular Automata Designs IEEE TRANSACTIONS ON NANOTECHNOLOGY, VOL. 13, NO. 3, MAY 2014

[10] H. Cho and E. E. Swartzlander, "Adder and multiplier design in quantum dot cellular automata," Computers, IEEE Transactions on, vol. 58, no. 6, pp. 721–727, 2009.

