



Analysis of Partial Selection SRAM Cell with Low-Voltage and Low-Leakage Power

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Abstract— *Low-power consumption in memory plays an important part in VLSI. But this memory consumes more power. The sub-threshold leakage power is the main reason to increase the leakage power. Proposed 10T SRAM design is used to reduce the leakage power and to obtain better performance at minimum VDD compared with conventional design. Another major problem suffered by SRAM during write operation is Partial-selection of cells. Therefore, a new 10T SRAM is designed using new low-power internal write-back scheme. To obtain low-voltage and low-leakage power 10T SRAM can be designed based on FinFET technology. The simulations have been carried out using the LTSPICE software.*

Key Words— *low power, memory, sense amplifier, static random access memory (SRAM), subthreshold.*

I. INTRODUCTION

Static RAMs are used widely in modern processors as on-chip memories due to their large storage density and small access latency. Static power is the power dissipated in a design in the absence of any switching activity. SRAM consumes more power in VLSI systems, because of regular increase of on-die cache memory [1]. One effective solution is to reduce leakage power and supply voltage to operate in subthreshold region. In subthreshold region, MOSFETs suffer from short-channel problems. This is due to weak channel control in these transistors in subthreshold, which also leads to increased sensitivity to process variation in these devices. The sub-threshold leakage power is the main reason to increase the leakage power [2]. This leakage is the only source of energy consumption in an idle circuit. Hence, the design of low-leakage SRAM cell is highly desirable. By the advancement of CMOS technology, SRAM undergo considerable degradation of cell stability due to the variation in V_{th} of the cell. Accurate V_{th} control is essential for high read stability. Similarly, variability and device leakage affect the write ability of the cell. Read and write operation in SRAM is performed by using individual bit-line of the cell so both read stability and write ability problem is avoided. Partial selection takes place when word-line WL of the SRAM is ON and the bit-lines are OFF leading to poor stability [3]. In this paper, a new low-power internal write-back scheme is used to overcome the problem of partial selection during write operation in SRAM.

The rest of this paper is organized as follows. Section II describes the challenges of conventional and previously published designs for SRAM cell. Section III proposes our new design for SRAM cell. The conclusion is given in Section IV.

II. RELATED WORK

Conventional 6T SRAM cell has serious difficulty in sizing of the transistors which is referred as access transistor sizing conflict. During write operation the weak access transistors cannot break the feedback loop to force the data into the cell which is referred as poor write-ability [4]. In 9T SRAM cell, there are two write access transistors which is managed by write signal (WR) and the data is stored in the upper circuit memory. The lower part of 9T SRAM cell consists of read access transistor and bit-line access transistor. Here there is improvement in read stability of 9T SRAM cell. But there is problem in maintaining the write-ability of the cell. The ST(Schmitt-Trigger)10T SRAM consists of internal feedback so it has large hold static noise margin. The ST10T SRAM design provides better noise immunity. But it has greater power consumption when compared to all other SRAM cells.

1) Conventional 6T CMOS SRAM Cell

The Conventional SRAM cell consists of six MOS transistors ('4' NMOS and '2' PMOS), Fig. 1. Each bit is stored in four transistors namely M1, M2, M3 and M4 which forms two cross-coupled inverters. The access transistors M5 and M6 are controlled by the Word Line (WL). The cell protects either '0' or '1' state, when the power is given to the bit-cell. Here, it has less static power dissipation. Thus during switching the cell draws current from the power supply.

8T SRAM cell has single-ended write operation so charging and discharging of write-bitline consumes less power compared with other differential write cells, and also the number of write drivers is half the other designs. Thus, write power of 8T SRAM is the lowest among all. Single-ended read operation in 8T SRAM cell leads to smaller power consumption for precharging read-bitlines before read operation. The read-bitline is not discharged. Conversely, always one of the read-bitlines in differential read SRAMs is discharged. 8T SRAM cell with feedback interrupt during write operation improves write-ability when compared with conventional 6T SRAM cell.

III. PROPOSED DESIGN FOR SRAM CELL

A 10T SRAM cell consists of 10 transistors Fig. 3. Out of these transistors, four pull-up transistors are M1, M2, M3 and M4, four pull-down transistors are M5, M6, M9 and M10 and two are access transistors namely M7 and M8. The four pull-down transistors are connected to ground. During the read operation the ground signal is connected to VDD [6]. In 10T SRAM cell, the access transistors are connected in between pull-up transistors M1, M2 and M3, M4. The storage nodes are q and qb. Due to this, the storage nodes are separated from the BL and BLB and for that reason during the read operation, the read current does not flow through the storage nodes and hence the read stability is maintained.

In write operation, the ground signal is connected to VDD and one of the bit-lines e.g. BL is grounded. Assume that the node Q is storing 1 and node Qb is storing 0. When applying a high supply voltage, the node Q is pulled down to 0 due to discharging through the access transistor M7 and the pull-up transistor M2. Here standard V_{th} pull-up transistors, low V_{th} access transistors and high V_{th} pull-down transistors are used. Due to the low V_{th} transistors, the gate voltage (V_g) required for activation of the access transistors are low and thus, the access speed for the data stored increases considerably. Also the high V_{th} Pull-down transistors decrease the leakage in the circuit.

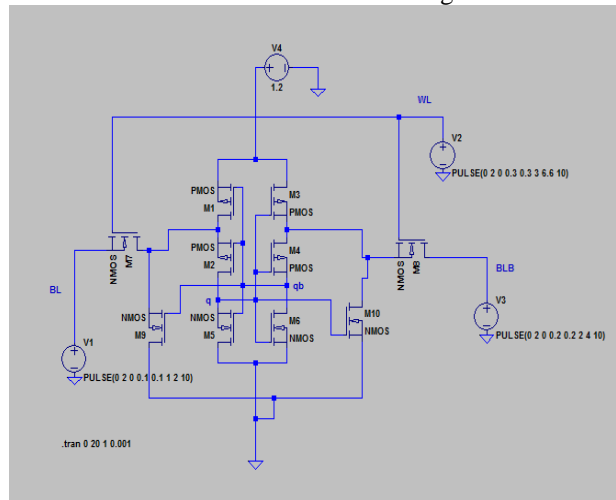


Fig. 3 10T SRAM Cell

IV. FINFET TECHNOLOGY

FinFET device is a quasi-planar double-gate transistor. Compared with bulk CMOS this structure allows FinFET devices to enhance the energy efficiency, ON/OFF current ratio, and soft-error immunity [7]. The FinFET technology is now used as an alternative to the bulk CMOS for improved scalability [8]. The three-terminal FinFET device structure is shown in Fig. 4(a) where both gates are shorted. Here H_{FIN} is height of the silicon fin, T_{Si} is thickness of the silicon fin, and L_{FIN} is gate length of the fin. Layout of a three-terminal FinFET with four fins is shown in Fig. 4(b). The main component is the fin which provides the channel for conducting current when the device is switched on. The gate is in either side of the vertical fin, it helps to reduce the leakage current and the short-channel effects [9], [10]. The ten transistor cell configuration is used to improve the stability of the cell and is used for sub-threshold purposes.

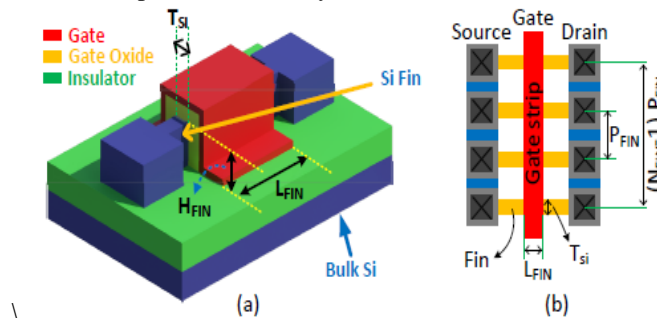


Fig. 4 FINFET Device: (A) Structure, (B) Layout

The true internal value on the write-bitline is setted without going through the whole rewriting process in order to eliminate the state of half selection. So there will be no false changing of internal nodes in the design translating to lower power overhead compared with previous write back schemes.

V. CONCLUSION

In this paper, a new 10T SRAM is designed and it is compared with different SRAM bit cell configurations. At $V_{DD_{min}}$ the proposed design has lower power consumption compared to other SRAM cells. A 10T SRAM is designed to overcome the problem of partial selection during write operation by using low-power internal write back scheme. By designing 10T SRAM cell using FinFET technology the low-voltage and low-leakage SRAM cell can be obtained.

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