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New Design Current Mirrors for Better Performance

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Abstract: ***This paper is designed with a view to provide better design configuration of the current mirror and to improve the output characteristics. The paper is based on new hypothesis and instinct. All simulation is done on Orcad Capture and Pspice.***

Keywords: Current Mirror, Cascode Current mirror.

I. INTRODUCTION

Current mirrors are vital circuits used for replicating the input current at the output terminal, in an integrated circuit design. In this paper a new design approach to the current mirror has been followed. The idea of the basic current mirror has been taken from the book of **Microelectronics by Sedra and Smith .**

A **Simple Current Mirror Figure1.** can be thought of as a circuit containing two transistors connected in such a way that, one serves as the master and the other acts as a slave. The master transistor is connected with such a configuration that it forces the slave transistor to work in saturation by itself being in saturation all the time. The operation is such that the input current becomes the replica of the output current. The given **Figure1** shows the simple current mirror together with its output characteristics in **Figure2**. The circuit consists of two transistors **M1** and **M2** which are perfectly matched in all aspects. The transistor **M1** is diode connected with $\mathbf{V_{GD1}=0V}$, so $\mathbf{V_{GS1}=V_{DS1}}$ **.** Since it is in connection with **M2** so the same gate – source voltage is applied to the transistor **M2 i.e.** $\mathbf{V_{GS1}=V_{GS2}}$**,** in order to force it in saturation. Under this condition $\mathbf{V_{DS1}=V_{DS2}}$ **,** i.e. the drain to source voltages of the two transistors become equal. This forces the input current equal to the output current. Thus the circuit replicates the current at the input to the output terminal. So we have for a simple current mirror

$$\mathbf{I_O = (W_2/L_2)/(W_1/L_1)\, I_{REF}} \qquad \mathbf{(1)}$$

The ratio $\mathbf{(W_2/L_2)/\ (W_1/L_1)}$ is called the transfer function of the current mirror. We can see that it is simply the ratio of the aspect ratio of the two transistors.

The input current can be generated by any means that is, it can be generated by a current source or a voltage source. The most important point of a current mirror is that the output current is insensitive to the variations in the output voltage, and this can be clearly seen from the output characteristics of the current mirror.

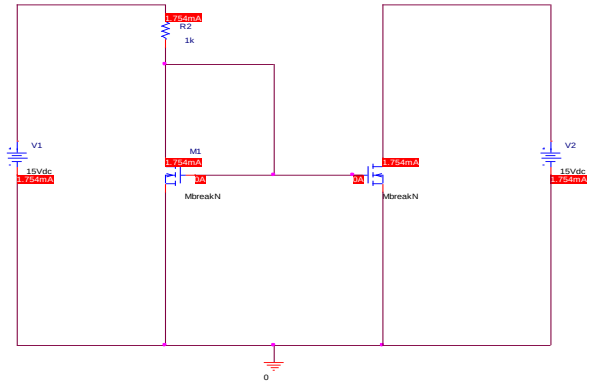

Figure 1. A simple current mirror

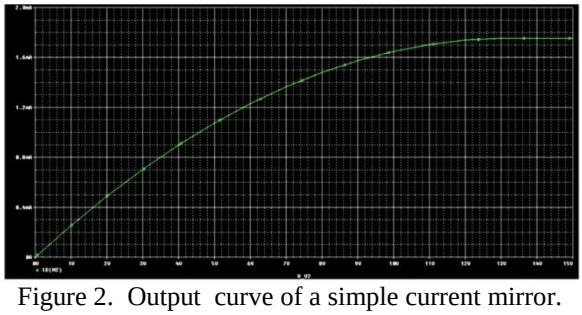

Figure 2. Output curve of a simple current mirror.

Cascode Current Mirror: A better performance current mirror can be designed by cascoding the two simple current mirrors as shown in the following **Figure 3.**

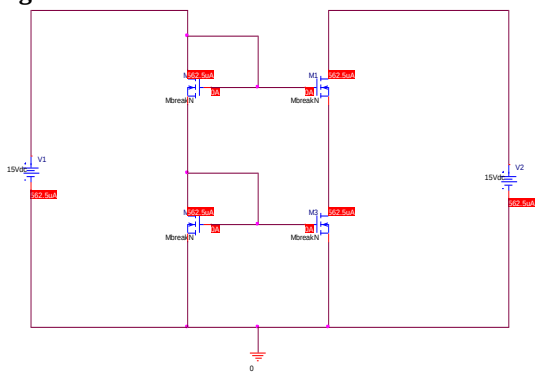

Figure 3. A cascode current mirror.

The **Cascode Current Mirror** is shown above it can be seen as the vertical concatenation of two simple current mirrors. Transistors **M1 & M2** form the upper current mirror. And transistors **M3 and M4** form the lower current mirror. The circuit has greater output impedance due to the extra device and also it has a lower output swing. For the above circuit we have

$$V_{DS2} >= V_{GS2} - V_T \quad (1)$$

$$V_{DS3} >= V_{GS3} - V_T \quad (2)$$

So for V_{GS2} for the output side we have

$$V_{GS2} = (2V_{SAT} + 2V_T) - V_T = 2V_{SAT} - V_T \quad (3)$$

All the transistors are matched in their aspect ratios therefore,

$$W_1/L_1 = W_2/L_2 = W_3/L_3 = W_4/L_4 \quad (4)$$

$$\&,\ V_{GS1} = V_{GS2} = V_{GS3} = V_{GS4} \quad (5)$$

M2 & M4 are always in saturation. This forces **M1 & M3** to go in saturation for the circuit to work properly. It clearly shows that

$$(W_1/L_1)/(W_2/L_2) = (W_3/L_3)/(W_4/L_4) \quad (6)$$

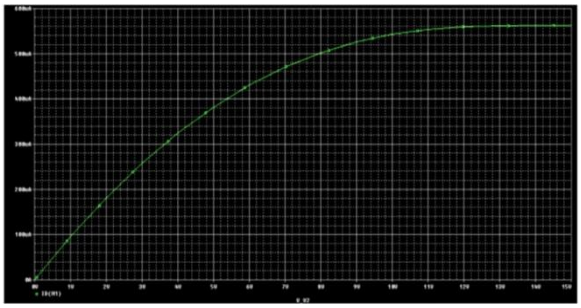

Figure 4. Output curve of a cascode current mirror

The output characteristics of the cascode current mirror can be shown as above.

II. PROPOSED CIRCUITS FOR CURRENT MIRROR

With an aim in mind to improve the output curves of the mirrors new designs has been introduced, the following new designs are shown as,

2.1 Improved Cascode Current Mirror

Abetter design of cascode current mirror can be thought of in a new way as shown below,

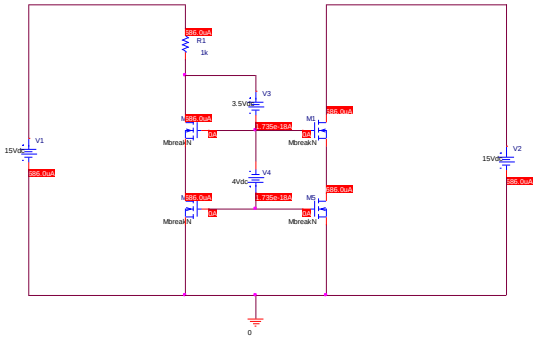

Figure 5. Improved cascode current mirror

The above design of the Cascode Current Mirror increases the current but also improves the output characteristics as shown in **Figure 6.**

The baising of the circuit with the additional voltages in the drain to gate path of the upper circuit of the mirror and in the four gates commonly increases the current and also the constancy. The circuit has **(5-3.5) V** that is 1.5V additional potential to hike the current. The main important point to note in this circuit is that the resultant of the two voltages at the gate keeps the channel always in saturation. In the simple current mirror circuit the we have $\mathbf{V_{GD}=0V}$, we have an advantage of 1.5V in this circuit such that gates of all the four transistors of the mirror are strongly fixed at the same voltage.

The output characteristics of the mirror are greatly improved as we can see that the constancy is obtained from 6V onwards. The output characteristics also show that the current has increased to a greater extent.

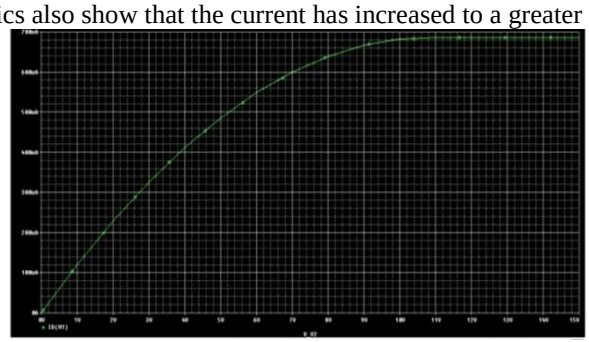

Figure 6. Output curve of the improved cascode current mirror

2.2 P- mirror

A new circuit of the current mirror is proposed in which a third transistor has been introduced which is connected in strong saturation and in perpendicular orientation to a transistor connected in saturation the circuit looks like as shown in **Figure 7**.

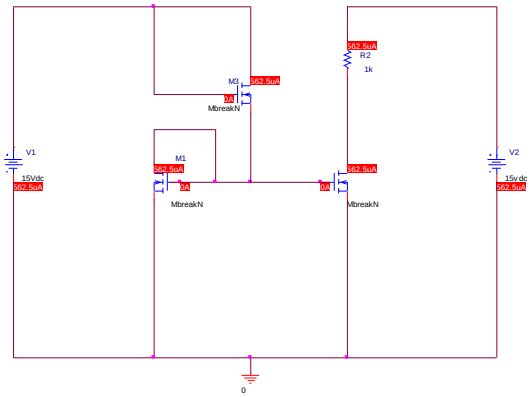

Figure 7. A P-mirror

The proposed circuit has given the name, because it resembles the English letter P in the two transistor connections, M1 & M3.

The transistors M1 & M3 are working in saturation and their source to gate connection provides the circuit with

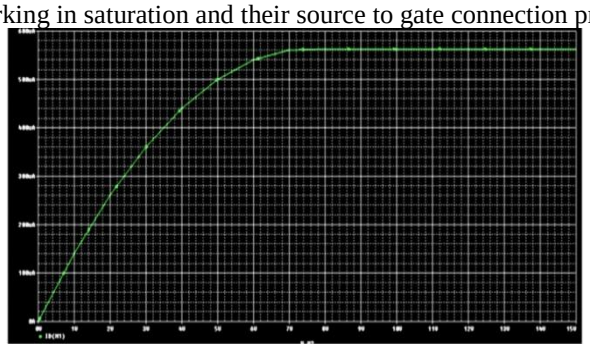

Figure 8. P –mirror output curve

greater constancy in current as the two transistors are diode connected the transistor M3, provides a greater current source thus increases the current up to a large extent. Device output characteristics can be shown in **Figure 8.**

2.3 Baised P-mirror

It is found that if the above P mirror is baised with an additional voltage souirce, the current will increase to a much greater extent than above. The circuit of the baised current mirror is shown in **Figure 9**.

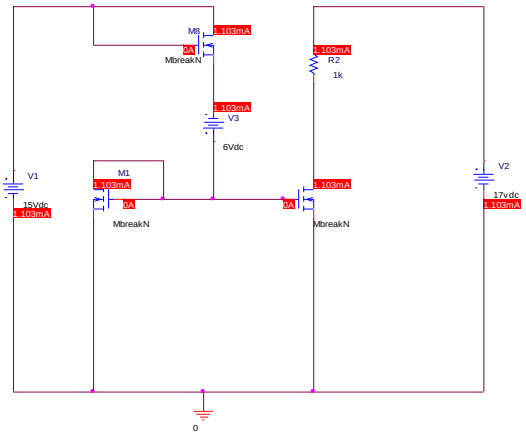

Figure 9. A biased P –mirror

The output characteristics of the baised P mirror can be shown in **Figure 10**.

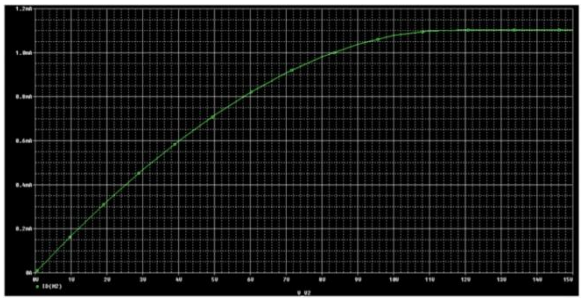

Figure 10. Biased P – mirror output curve

The output characteristics show that though the constancy is reduced than the previous one but, there is a great increase in the value of current. The additional biasing thus enhances the current by providing a strong saturation.

2.4 Nested P- mirror

The circuit of the Nested P- mirror looks like **Figure 11**. It can be seen that it consists of a simple current mirror nested in the upper "P" of the circuit. The circuit preformance can be viewed from the output characteristics of the mirror,**Figure 12** and it can be seen that the nested current mirror circuit is proviiding and additional support to the constancy,and also the current is also at greater value than the simpler configurations.

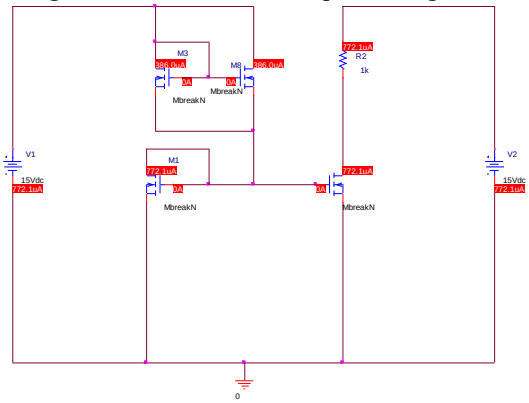

Figure 11. A Nested P-mirror

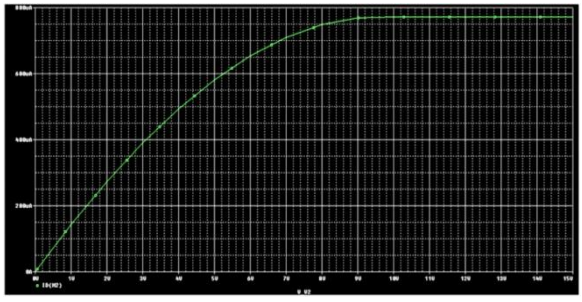

Figure 12. Output curve of the Nested P-mirror

III. SIMULATION AND RESULTS

The work is purely experimental and simulation based. All the circuit design and simulation is done on Orcad Capture and Pspice. The following table shows the result of the circuit simulationfor various designs.

Table 1. Output of simulations of various current mirror designs.

Serial no.	Design	Current	Constancy
1.	**Simple current mirror**	1.754mA	From 13 V onwards
2.	**Cascode current mirror**	562.5 uA	After 13 V onwards
3.	**Improved cascode current mirror**	686uA	From 10V onwards
4.	**P-mirror**	562.5uA	From 7 V Onwards
5.	**Baised P-mirror**	1.103mA	From 10V onwards
6.	**Nested P- mirror**	772.1uA	From 7V onwards

IV. CONCLUSION

The above designs show us that the constancy and the output current has a trade off in some designs and we can see that the new designs are giving more ideal characteristics. From the above given table we can see that the P – mirror is giving constancy from 7 volts which is the similar result with nested P –mirror. However, the current value is increased in baised P- mirror, with a compromise of constancy.

REFERENCES

[1] Sedra & Smith ,Pearson Publicatons.
[2] Robert J Boyelstad , Pearson Publication.
[3] Principles of Electronics Malvino & Bates ,Tata McGraw Hill.

