



Comparative Analysis of CSL, CPL and DPL Based Adder Using 90NM, 130NM and 180NM Technology

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Abstract: Continuous scaling of the transistor size and reduction of the operating voltage has led to a significant performance improvement of integrated circuits. Low power consumption and smaller area are some of the most important criteria for the fabrication of DSP systems and high performance systems. In this paper an effort has been made to determine the best solution to this problem by comparing a few adders.

We have implemented Different 16-bit adders such as CSL, CPL and DPL by sharing the common Boolean logic term. In this, we used Tanner tool for simulation and different technologies 90nm, 130nm and 180nm and results are simulated accordingly. In this, circuits are simulated with different gate width and different channel length. Our results show that CSL is more efficient than CPL and DPL in terms of power consumption, area and delay.

Keywords: CSL, CPL, DPL, Low power design.

I. INTRODUCTION

The adder is the most commonly used arithmetic block of the Central Processing Unit (CPU) and Digital Signal Processing (DSP), therefore its performance and power optimization is of utmost importance. With the technology scaling to deep sub-micron, the speed of the circuit increases rapidly. At the same time, the power consumption per chip also increases significantly due to the increasing density of the chip. Therefore, in realizing modern Very Large Scale Integration (VLSI) circuits, low-power and high-speed are the two predominant factors which need to be considered. Like any other circuit's design, the design of high-performance and low-power adders can be addressed at different level, such as architecture, logic style, layout and the process technology. As a result, there always exists a trade-off between the design parameters such as speed, power consumption and area.

Arithmetic circuits like adders are one of the basic components in the design of communication circuits. Recently, an overwhelming interest has been seen in the problems of designing digital systems for communication systems and digital signal processing with low power at no performance penalty. Designing low power, high-speed arithmetic circuits requires a combination of techniques at four levels; algorithm, architecture, circuit and system levels. The remainder of this paper is organized as follows; section 2 describes the theoretical background. Section 3 describes the circuit designing and implementation of CSL, CPL and DPL adders. While corresponding experimental results and comparison of CSL, CPL and DPL adders are presented in section 4. Conclusion is described in section 5. Finally, future scope is given in section 6.

II. THEORETICAL BACKGROUND

The research efforts of the past years in the field of digital electronics have been directed towards the low power of digital systems. Recently, the requirement of probability and the moderate improvement in battery performance indicate power dissipation is one of the most critical design parameters. Day by day the demand of probability and mobility is increasing. Also the area of chip design is taken into consideration while talking about probability. Hence three most widely accepted parameters to measure the quality of a circuit or to compare various circuit styles are area, delay and power dissipation.

The reduction of the power dissipation and the improvement of the speed require optimization at all levels of the design procedure. Since most digital circuitry is composed of simple AND/OR complex gates, the best way is to implement logic and arithmetic functions in order to achieve low power dissipation and high speed. Several circuit design techniques are compressed in order to find their efficiency in terms of speed and power dissipation. In these days transistors are used for designing logic gates, same transistors are used to design other blocks such as flip-flops or memories. Ideally, a transistor behaves like a switch. For NMOS transistors, if the input is a 1 the switch is on, otherwise it is off. On the other hand, for the PMOS, if the input is 0 the transistor is on, otherwise the transistor is off [2].

There are three major sources of power consumption in digital CMOS circuits, which are summarized in the following equation [1].

$$P_{total} = P_{switching} + P_{short-circuit} + P_{leakage}$$

$$= (\alpha_{0 \rightarrow 1} \times C \times V_{dd}^2 \times f_{clk}) + (I_{sc} \times V_{dd}) + (I_{leakage} \times V_{dd}) \quad (1)$$

The first term represents the switching component of power, where C is the load capacitance, f_{clk} is the clock frequency and $\alpha_{0 \rightarrow 1}$ is the node transition activity factor. The second term is due to the direct path short circuit current, I_{sc} , which arises when both the NMOS and PMOS transistors are simultaneously active, conducting current directly from supply to ground. Finally, leakage current, $I_{leakage}$, which can arise from substrate injection and sub threshold effects, is primarily determined by fabrication technology considerations. However, while supply voltage reduction is the most effective way to reduce the power consumption, such a reduction require new design methods for low-voltage and low power integrated circuits. Since an average of 15-20% of the total power is dissipated in glitching, low power can also be achieved by reducing the glitches of the circuit [1].

III. CIRCUIT DESIGN AND IMLEMENTATION

This section contains the circuit designing and implementation of CSL, CPL and DPL adders.

3.1. CONVENTIONAL STATIC CMOS LOGIC (CSL)

Conventional static CMOS logic is used in most chip designs in VLSI applications. It consists of complementary NMOS pull-down and PMOS pull-up networks to drive '0' and '1' outputs. The features of this logic style are good noise margin, fast speed, low power and easy to design. Other advantage of static CMOS logic style is its robustness against voltage scaling and transistor sizing which enables reliable operation at low voltages and arbitrary transistor sizes. The schematic diagram of a conventional static CMOS AND gate and full adder cell is illustrated in Figure 1 and Figure 2 respectively [3].

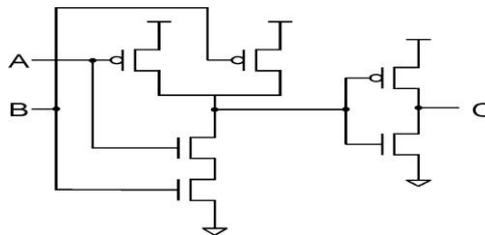


Figure 1: Schematic diagram of CSL AND gate

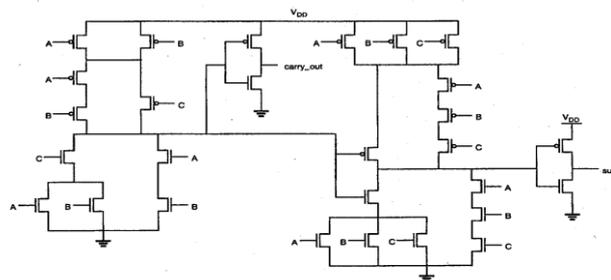


Figure 2: Schematic diagram of CSL Full Adder

3.2. COMPLEMENTARY PASS-TRANSISTOR (CPL)

CPL consists of complementary inputs, outputs, an NMOS pass transistor logic network, and CMOS output inverters as shown in Figure 3.

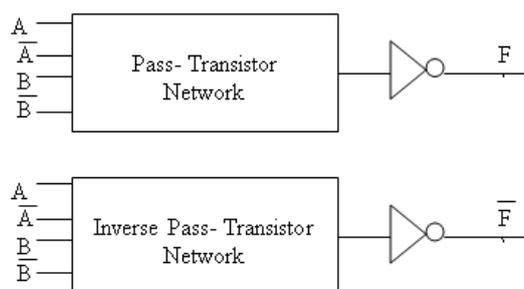


Figure 3: Basic Concept of CPL

As inverted and non-inverted inputs are needed to drive the gates of the pass-transistors, the complement of the logic also needs to exist. The pass-transistor network and inverse pass-transistor network is generate F and \bar{F} . The schematic diagram of the CPL AND gate & full adder circuit is shown in Figure 3. The equations for Figure 3 are given as [4]:

$$F = A.B + \bar{A}.B = A.B \quad (2)$$

$$\bar{f} = \bar{A}.B + \bar{B}.\bar{B} = \bar{A}.B + \bar{B} = \bar{A} + \bar{B} = \overline{AB} \quad (3)$$

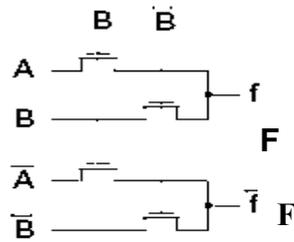


Figure 4: Schematic diagram of CPL A AND Gate

3.3. DOUBLE PASS TRANSISTOR LOGIC (DPL)

The DPL is a modified version of CPL. The DPL also has complimentary inputs and outputs and thus it is implemented using dual-rails. In DPL circuits, full voltage swing is achieved at outputs by adding a PMOS transistor in parallel with NMOS transistors. Although the addition of PMOS transistors results in increased capacitance compared to CPL style but this does not limit the performance of DPL because DPL gates have balanced input capacitance, thus reducing the dependence of delay on input data.

The problems of noise margin and speed degradation in CPL circuits due to high reduced voltage level are solved out in DPL design style. The output buffers are not necessary, since the full swing is achieved by the addition of PMOS transistor. The schematic diagram of the DPL AND gate & full adder circuit is shown in Figure 5 [5].

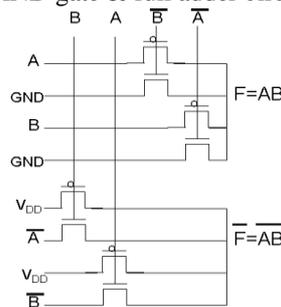


Figure 5: Schematic diagram of DPL AND gate

IV. RESULTS & COMPARISON

4.1. WAVEFORM OF CPL ADDER

The waveform of CPL adder is shown below in Figure 6 . In this there are three inputs A, B and C and two outputs sum and carry.

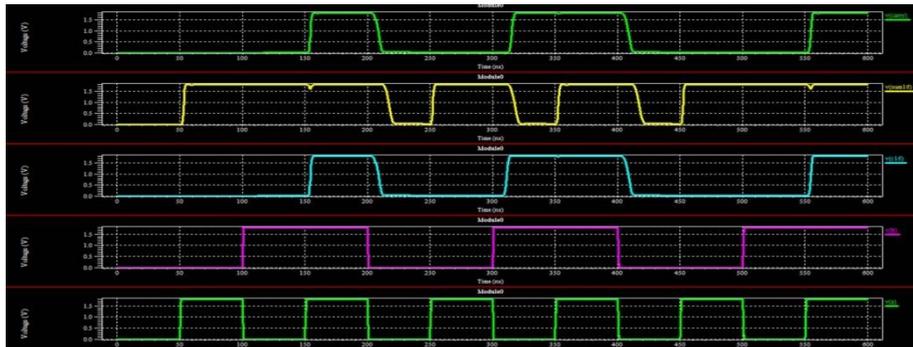


Figure 6 : Waveform of CPL Adder

4.2. WAVEFORM OF CSL ADDER

The waveform of CSL adder is shown below in Figure 7. In this there are three inputs A, B and C and two outputs sum and carry.



Figure 7 : Waveform of CSL Adder

4.3. WAVEFORM OF DPL ADDER

The waveform of DPL adder is shown below in Figure 8. In this there are three inputs A, B and C and two outputs sum and carry.

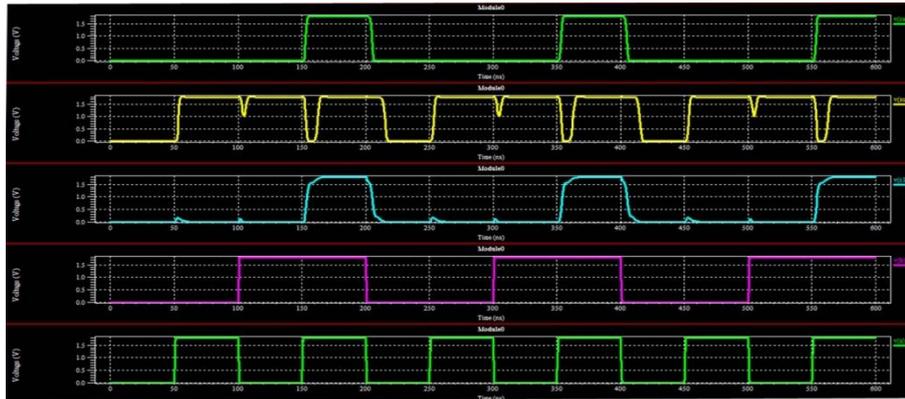


Figure 8 : Waveform of DPL Adder

In this design process, all simulations are run using Micron Technology’s 90nm,130nm,180nm process models with typical n-channel and p-channel drive, a .9v, 1.3v and 1.8v power supply. In the schematics all logic is designed using a minimum gate length of 90nm,130nm,180nm and a minimum width of 1.35µm,1.95µm, 270µm for NMOS and for PMOS 4.05µm, 5.85µm and 810µm gate width. According to the power dissipation, delay and area, CSL adder is better as compared to CPL and DPL adder.

Table 1 Performance Parameters of 16-Bit Adders

Design Style	No. of transistors	Minimum Length (nm)	Width of NMOS (nm)	Width of PMOS (nm)	Avg. Power Consum. (watts)	Prop. Delay at Sum (sec)	Prop. Delay at carry (sec)	PDP of Delay at sum	PDP of Delay at carry
CPL	352	90nm	135nm	405nm	5.463139e-004 watts	1.9960e-009	5.4511e-009	10.904527e-013	29.780395e-013
		130nm	195nm	585nm	5.014173e-004 watts	1.4479e-009	4.2761e-009	7.260021e-013	21.441105e-013
		180nm	270nm	810nm	6.556204e-004 watts	1.8265e-009	5.1997e-009	11.974906e-013	34.090293e-013
CSL	448	90nm	135nm	405nm	3.228008e-004 watts	3.0494e-009	2.2550e-009	9.8434875e-013	7.279158e-013
		130nm	195nm	585nm	2.588378e-004 watts	2.7986e-009	2.1491e-009	7.2438346e-013	5.5626831e-013
		180nm	270nm	810nm	2.654090e-004 watts	5.1513e-009	1.7670e-009	13.672013e-013	4.689777e-013
DPL	544	90nm	135nm	405nm	7.716474e-004 watts	2.1229e-009	2.4261e-009	16.381302e-013	18.720937e-013
		130nm	195nm	585nm	7.237165e-004 watts	2.2997e-009	2.5425e-009	16.643308e-013	18.400492e-013
		180nm	270nm	810nm	7.672943e-004 watts	1.9779e-009	2.2433e-009	15.176317e-013	17.212717e-013

V. CONCLUSION

Focus of this paper was mainly on low power and high performance adder. The adder designed in this work provides the low power requirement. It also presents an area efficient approach to low power, less number of transistors for any design.

16-bit adders were designed in Tanner (Evaluation version) tool using 90nm, 130nm and 180nm and analysis of dynamic power dissipation, delay and area was done. Table 1 above shows the power comparison. The results in table 1 are at Channel length for both NMOS & PMOS using 90nm, 130nm and 180nm.

VI. FUTURE SCOPE

CSL, DPL, CPL based advanced full adder circuit reduces the transistor count, power consumption and delay of the circuit. The work of this paper may be further extended by various ways as:

- The work can be extended to 64-bit adders.

- The research steps may be taken further to optimize the parameters like using frequency, capacitance, length, width etc.
- The work can be extended to change the technology file.
- The efforts can be made to decrease the transistor count further Power, area and delay can be minimized by changing the parameters.
- Research steps can be taken by using the other types of adders like Ripple Carry Adder, Hybrid adder etc.

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