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A Delay Optimized Adder with Self Checking Property

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Abstract— The paper proposes a design methodology to contribute the requirements for the designing of adders with reduced delay and also having Self-checking property. Self checking designs gains interest in various industrial applications as the requirements of high fault coverage and reduced hardware cost with reduced design effort is full filled. Here a new self-checking adder with dual duplicated functional outputs is presented. The sum function as well as its inverse is implemented within a single cell. The hardware overhead for the implementation of the proposed adder is lower than the hardware overhead required for complete duplication of the Adder. Thereby, the error detection capabilities are almost the same as for the complete duplication. The designed adder has been simulated for the Vcc voltage 1.20 V and input output voltage 3.30 V at 27^{o}C and 70^{o}C in CMOS 50 nm , 70 nm and 90 nm technologies using Microwind. The results shows the reduction in delay compared to other adders and also self testing for primary inputs.

Key Words—totally self Checking, hybrid adder, differential XOR , CMOS pass transistor logic.

I. INTRODUCTION

Interest in on-line error detection continues to grow as VLSI circuits increase in complexity [24]. Online checking is increasingly becoming advantageous as it detects transient faults that may occur in a circuit during normal working operation. Online Error Detection techniques allow the detection of transient faults, which probably not be detected in off-line testing, since they may not occur in test mode.

Adder is the core element of complex arithmetic circuits like addition, multiplication, division, exponentiation, comparators parity checkers etc [1]-[7]. Therefore, making it self checking, reducing the delay and increasing the speed in adders, will reduce the overall delay of the whole system and also making the system self checking. Most of the VLSI applications, such as digital signal processing, image processing, video processing and microprocessors, extensively use arithmetic operations. Binary addition is considered as the most crucial part of the arithmetic unit because all other arithmetic operations usually involve addition. That's why, building self checking, low-power, high performance adder cells are of great interest and any modifications made to the full adder would affect the system as a whole. The vast use of this operation in arithmetic functions attracts many researchers to this field. In recent years several variants of different logic styles have been proposed to implement 1-bit adder cells [5]-[20]. They commonly aimed to reduce delay , power consumption and increase speed. These papers have also investigated different approaches realizing adders using CMOS technology ,each has its own advantages and disadvantages.

II. SELF CHECKING CIRCUITS

Self Checking Circuit Designing is a suitable approach to the design of complex VLSI IC's to cope with the growing difficulty of on line and off line testing [24]. Self checking circuits are class of circuits in which occurrence of fault can be determined by observation of the outputs of the circuits. An important subclass of these self-checking circuits is known as totally self-checking (TSC) circuits. Self-checking is a design philosophy which assures on-line testability of a circuit. [24]
A totally self-checking (TSC) functional block satisfies the two following properties:

- For any valid input code word and any single fault, the circuit, either produces an invalid code word on the output, or (fault secure) i.e. does not produce the error on the output.
- Any single fault is detectable by some valid input code word (self-testing property)

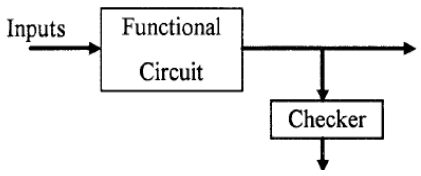

Figure 1 Basic Block diagram of self checking logic circuit

TSC circuits are used to detect errors concurrently with normal operation. These circuits operate on encoded inputs to produce encoded outputs. TSC checkers are used to monitor the outputs to indicate error when a non-code word is detected. The concept of TSC circuits was generalized in [23] as follows

Definition 1. : A circuit is self-testing if for each fault f, present in the circuit, there exists at least an input code word that produces a non code word output

Definition 2. : A circuit is fault-secure if for any fault, f present in the circuit, the output for a code word input will be the correct output or a non valid output code word

Definition 3: A circuit is *totally self-checking* if it is fault secure and self-testing.

Definition 4: A circuit is *code disjoint* if it always maps code word inputs into code word outputs and noncode word inputs into noncode word outputs.

Definition 5: A circuit is a *totally self-checking checker* if it is self-testing and code-disjoint.

A totally self-checking (TSC) functional block satisfies the two following properties:

- For any valid input code word and any single fault, the circuit, either produces an invalid code word on the output, or (fault secure) i.e. does not produce the error on the output.
- Any single fault is detectable by some valid input code word (self-testing property)

III. BASIC CMOS FULL ADDER

Full Adder is a combinational circuit with three inputs i.e. A, B and C and two outputs i.e. SUM and CARRY [1]-[4]. It is one of the basic building blocks of the digital design the truth table of full adder is shown in table 1.

Table 1: Truth Table of Full Adder

A	B	C	SUM	CARRY
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

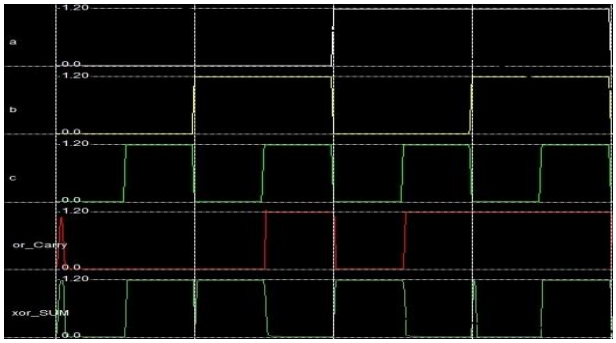

Figure 2 Waveform of Full Adder

SUM = A XOR B XOR C

CARRY = AB + BC + CA

The CMOS design style is not area- efficient for complex gates with larger fan-ins. Thus, care must be taken when a static logic style is selected to realize a logic function. The CMOS structure combines PMOS pull-up and NMOS pull-down networks to produce considered outputs. In this style all transistors are arranged in completely separate branches, each may consist of several sub-branches. Mutually exclusiveness of pull-up and pull-down networks is of a great concern. Figure 4 shows the conventional CMOS 28-transistor adder [6,9].

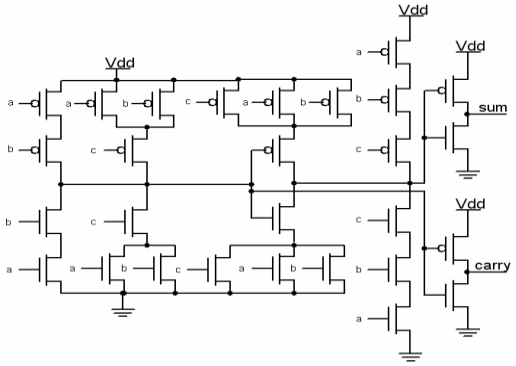

Figure 3.Conventional CMOS full adder.

IV. DIFFERENT HYBRID FULL ADDERS

Hybrid adders consist of more than one logic styles in its implementation and they may be classified in various categories depending upon their output structure and signals.

A. Logic Design Approaches of XOR-XNOR (4T) Based Full Adder Module.

Adder topologies are based on basic two circuits: one to generate H (XOR) with H (XNOR), and the other to generate the Sum output function as shown in Figure 4. The Carry signal is obtained by using one MUX (multiplexer).

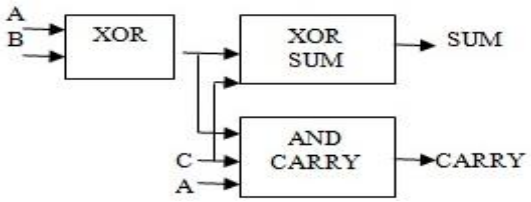

Figure 4 Basic Design Aproach For Hybrid Full Adder

Sum = A XOR B XOR C and Carry = AB + C (AXOR B)

Powerless P-XOR and Groundless G-XNOR are as new set of low power 4 transistor XOR and XNOR circuits respectively are proposed in [15-17]. The P-XOR and GXNOR consumes less power than other design because it has no power supply or ground connection.

B. 14 T and 16T Full Adder with Full Swing output Logic

A full adder circuit 14T & 16T has been designed using low power 4T XOR-XNOR design and transmission gates as shown in Figure 5. 14T transistors utilizes the low power XOR/XNOR circuit and a pass transistor network to produce a non full swing sum signal and uses four transistors to generate a full swing carry signal, which do not provide enough driving power [13].

Due to using pass transistor networks, the output signals of 14T do not provide good driving power A 16T adder is derived from the 14 transistors circuit [9], which has 16 transistors, generates full swing XOR and XNOR signals by utilizing a pass transistor based DCVS circuit. As mentioned in [11], this leads to higher speed and better performance in comparison with the circuit proposed in [12]

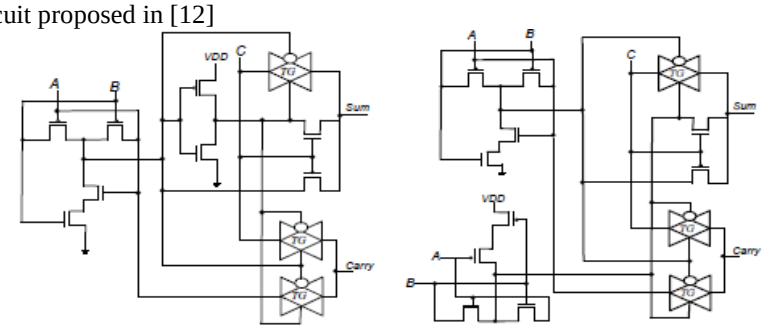

Figure 5 (a) 14 T Full Adder (b) 16 T Full Adder

C. 10T Full Adder

The designs of the 10T adder requires two XOR operations to calculate the Sum function. Each XOR operation requires 4T transistors. 2X1 MUX is used for Carry function implemented using two transistors. In [15] different components have been combined to make 41 new 10T transistor full adders. Some 10T full adders can be designed by interchanging the inputs of the module having lowest propagation delay amongst all the 10T full adder circuits.

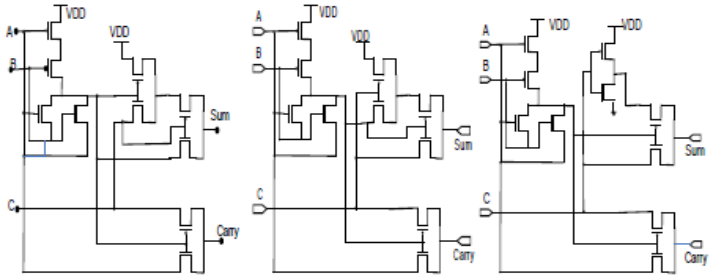

Figure 6(a)9A Ful Adder (b)9B Full Adder (c)13A Full Adder

The 9A full adder is shown in Figure 6 (a), implements 4- transistor XOR-XNOR circuit, 4-transistor groundless XNOR circuit and 2X1 multiplexer. The 9B full adder has shown in Figure 6(b), implements using 4-transistor XORXNOR circuit, 4-transistor groundless XNOR circuit and 2X1 multiplexer. A transistor –level implementation for 10 transistor full adder 13A is shown in Figure 6(c). 10 transistors full adders 13A and 9B have better critical delay than the 10 transistors SERF full adder in all loading condition.

D. SERF Full Adder

The Static Energy Recovery Full adder (SERF) is a 10 transistor (10T) adder shown in Figure 7[14]. The circuit is claimed to be extremely low power consuming because it does not contain direct path to the ground . The elimination of the path to the ground reduces the total power consumption by reducing the short circuit power consumption.

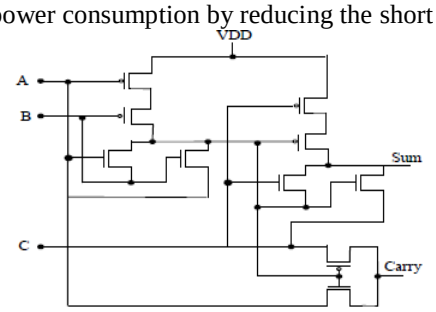

Figure 7 SERF Full Adder

There are some problems in this circuit. First Sum is generated from two cascaded XNOR gates which leads a long delay. Second, it cannot work correctly with a low voltage.

E. CLRCL Full Adder

Liu, Hwang, Sheu and Ho, however, could minimize the threshold loss problem in a 10T full adder reported in [16] as a Complementary and Level Restoring Carry Logic (CLRCL) figure 8 full adder. In the CLRCL adder, 2X1 MUX and CMOS inverters are used to realize the Sum and Carry functions. The double threshold loss problem encountered by the 10T full adders (SERF) is also alleviated by it. The goal is to reduce the circuit complexity and to achieve faster operation.

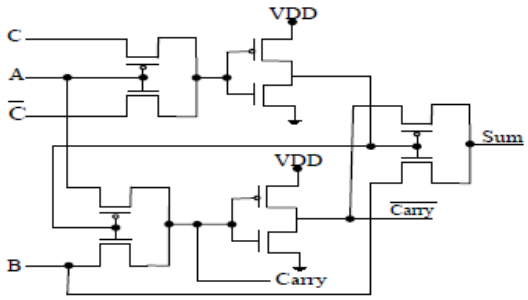

Figure 8 CLRCL based adder

The limitation of CLRCL full adder design is a skew between inputs to the various sub-sections in CLRCL full adder.

F. XOR-XNOR (4T) based Full Adder

The XOR based full adder consists of one exclusive OR/NOR function (XOR /XNOR) two transmission gates in the middle, and one XOR gate on the right. This hybrid circuit is a designed combination of TG with PT logic style that shows high-speed and energy efficiency [7]. The reported circuit has the least number of transistors and no complementary input signals are required. The complementary outputs of the XOR/XNOR gate are used to control the transmission gate which together realizes a multiplexer circuit producing the Carry output function.

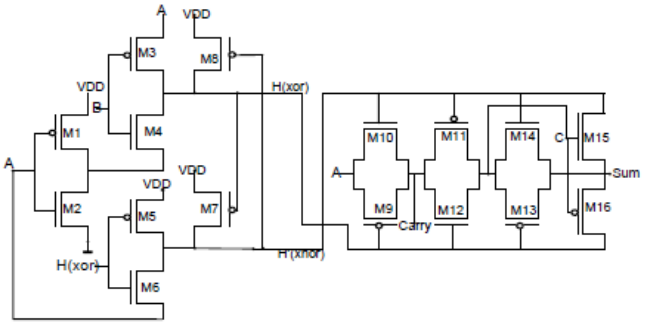

Figure 9 XOR-XNOR (4T) based 16T (4T) Full Adder

V. PROPOSED SELF CHECKING ADDER.

The exclusive-OR (XOR) and exclusive-NOR (XNOR) are fundamental components in full adders[4 , 6 , 18 , 22] and in larger circuits such as multipliers, parity checkers etc.[19, 20]. The XOR gate can be implemented using AND, OR and NOT CMOS gates. However, this solution requires large hardware overhead. On the other hand, pass transistor logic is attractive as fewer transistors are needed to implement important logic functions, smaller transistors and smaller capacitances are required, and it is faster than conventional CMOS.

Many different pass-transistor logics have been proposed. These structures are generally, composed by an NMOS pass-transistor network to realize the logic function followed by a suitable level-restoring circuit. A novel differential XOR designed in CMOS pass transistor logic is presented in Fig 10. This gate has dual inputs and generates dual outputs. XOR and XNOR functions are performed with only four transistors.

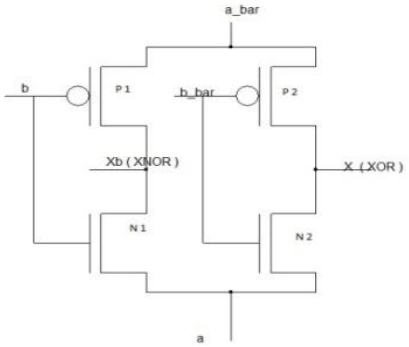

Figure 10 Self Checking XOR schematic

To increases the reliability of *Totally Self Checking* adder we use hardware redundancy. The simplest hardware redundancy approach is to designing a *Totally Self Checking* logic circuit using dual duplication. Typically, the design provides two copies of the circuit output. The second copy produces output values complementing the value of the first copy, and a tree of two rail code. (TRC) checkers makes a bitwise comparison of the outputs, Whenever the natural and complementary outputs configurations differ from each other, or whenever a fault affects one of the self-checking *TRC* checkers, the error signal reports the presence of fault.

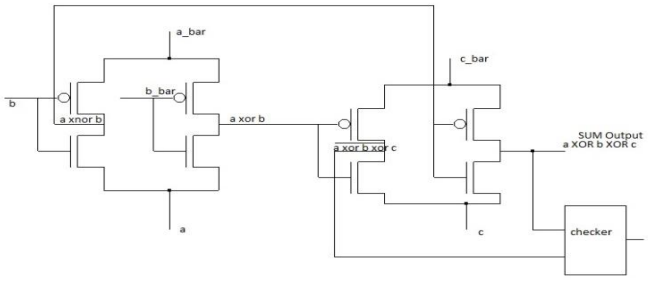

Figure 11. Three inputs Xor (sum function) circuit. (Using self checking XOR)

Figure 11 shows the schematic of sum function which has been designed using self testing XOR. The output function generates two outputs one is a XOR b XOR c and other one is the compliment of the same.TRC(Two Rail Checker) checker checks the output of both and generates an error signal in the presence of fault. The advantage of designing the sum logic using self checking XOR makes it totally self checking for all single faults. The sum logic requires 8 transistors and 6 transistors are required for complimentery inputs. logic expressin for sum is

SUM = A XOR B XOR C

Figure. 12 illustrate a sharing transistor implementation of carry function. Its logic expression is as follows

Carry□□a □b □□a □□c □□b □□c

The transistors in circles (Fig. 12) are sharing transistors. "Sharing transistors" provide the possibility of sharing the transistors of different paths to create a new path from supply lines to an output. These transistors help the circuit to reduce delay. These transistors must be arranged in such a way that not only validate the correctness of the circuit, but also preserve pull-up and pull-down networks mutually exclusive. The circuit in figure below is also designed using duplication scheme in which the output from pull up network is compared with the output of pull down network using a checker which generates an output high in presence of fault. Thus we can see that we need 10 transistors to implement the carry function.

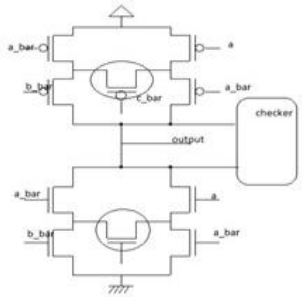

Figure 12 Carry generator circuit. (Using sharing transistor)

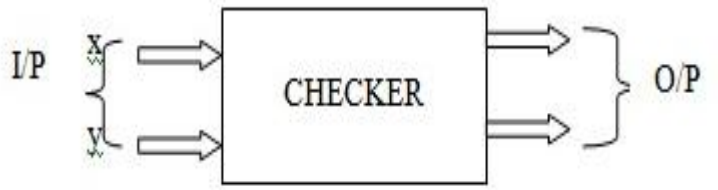

Figure 13 Block Diagram of a Checker (y = x_bar)

Table 2: Error Detecting Capability of Checker

X	Y = X_bar	O/P
0	0	Error
0	1	Ok
1	0	Error
1	1	Ok

A checker is basically a equality comparator gate which compares the input and gives the output high in presence of fault. Table 2 shows the error detecting property of a checker. A total of 18 transistors (8 for sum and 10 for carry) are required for implementing our design (generally complimentary inputs are present) which are less then conventional one (which requires 28 transistors) and also making our adder totally self checking. The improvement in speed over conventional CMOS adder is achieved due to less delay in the path due to sharing transistor, which leads to a better power-delay product. A complete fast full adder can be built by placing the sum circuit of Fig. 11 and the carry generator of Fig. 12 together as a whole circuit and these full adder cells can be placed to make a complete fast self testing adder with less number of transistors as well.

VI. PROPOSED ADDER (TOTALLY SELF CHECKING PROPERTY) ANALYSIS

The highest level of protection is offered by the combination of fault secure and the self testing properties.[17 , 24].The behavior of the differential XOR Gate of figure 4(b) is analyzed in terms of fault secure and self testing properties which includes logical stuck at faults and stuck open faults. For inputs, we consider the logical *stuck-at fault model (gate* stuck-at 0 and gate stuck at 1 fault).a and a~, b and b~ are normally complementary inputs. Table 3 shows the fault secure property for primary inputs.

Table 3: Primary Inputs Fault Secure Property

Inputs				**Outputs**		**Conclusion**
a	a~	b	b~	X	Xb	
0	0	0	0	0	0	Multiple Fault Detected
0	0	0	1	0	0	Single Fault Detected
0	0	1	0	0	0	Single Fault Detected
0	0	1	1	0	0	Multiple Fault Detected
0	1	0	0	1	1	Single Fault Detected
0	***1***	***0***	***1***	***0***	***1***	***OK (valid inputs)***
0	***1***	***1***	***0***	***1***	***0***	***OK (valid inputs)***
0	1	1	1	0	0	Single Fault Detected
1	0	0	0	0	0	Single Fault Detected
1	***0***	***0***	***1***	***1***	***0***	***OK (valid inputs)***
1	***0***	***1***	***0***	***0***	***1***	***OK (valid inputs)***
1	0	1	1	1	1	Single Fault Detected
1	1	0	0	1	1	Multiple Fault Detected
1	1	0	1	1	1	Single Fault Detected
1	1	1	0	1	1	Single Fault Detected
1	1	1	1	1	1	Multiple Fault Detected

The self testing property of differential XOR can be proved by using the fault equivalence principle, for single transistor stuck open faults. A PMOS transistor open is equivalent to a PMOS whose gate is stuck-at 1, and a NMOS transistor open is equivalent to a NMOS whose gate is stuck-at 0. [24]

To prove the self-testing property, we will show that for each fault there is ***at least one input vector***, occurring during the circuit normal operation that detects it.

- *Transistor P1 stuck-open*

P1 gate receives the signal b.
P1 stuck-open ⇔ b stuck-at 1. This fault, as shown in the table 1, is detectable by the input vectors (a a~ **b** b~) = (01**0**1) and (a a~ **b** b~) = (10 **0**1).

- *Transistor N1 stuck-open*

N1 gate receives the signal b.
N1 stuck-open ⇔ b stuck-at 0. The input vector (a a~ b b~) = (0110) or (10 10) detects this fault

- *Transistor P2 stuck-open*

P2 gate receives the signal b~.
P2 stuck-open ⇔b~ stuck-at 1. The input vector (a a~bb~) = (0110) or (10 10) detects this fault

- *Transistor N2 stuck-open*

N2 gate receives the signal b~.
N2 stuck-open ⇔b~ stuck-at 0. The input vector (aa~bb~) = (0101) or (10 01) detects this fault
By observing the input vectors we see that all these vectors belong to the set of valid input codes. Consequently, the differential XOR is self-testing for all single transistor stuck-open faults.

VII. SIMULATION RESULTS

The simulation has been performed in Microwind for different technologies 120 nm , 90 nm , 70 nm , 50 nm . Voltage range for 120 nm is 1.20 V and for input output is 3.30 V for 90 nm and 70 nm is 1V and input output 3.30 V for 50 nm is 0.5 V to and input output 2.50V which allow us to compare the speed degradation that is the delay of newly designed adder topology. The results of the designed circuits in this paper are compared with a reported standard CMOS full adder circuit of [7] . Temperature of operation for circuits is kept at 27^{o}C to 70^{o}C. Default values of the channel width (W) and length (L) for nMOS and pMOS for all technology are taken. By the proposed design it is possible to reduce the delay of all the adders without significantly increasing the power consumption, and transistor sizes can be set to achieve minimum *power delay product* (PDP). Each one-bit full adder has been analyzed in terms of propagation delay.

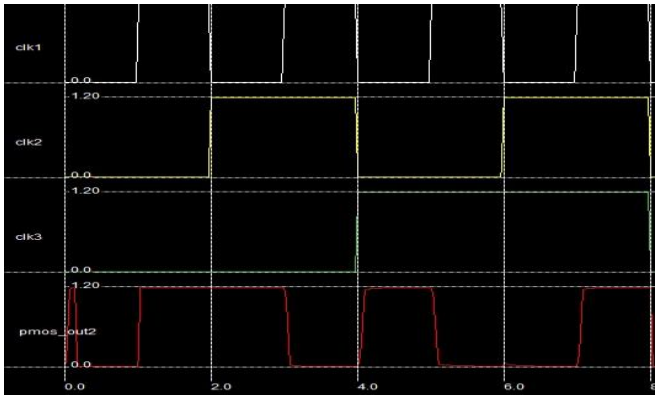

Figure 14 Waveform of Sum for Proposed Adder

Table 4: Simulation Result Of Proposed Adder For Different Technology And Voltage Range For Sum

Technology	Delay in Ps	
	Temp 27 ^{0}C	**Temp 70^{0}C**
0.12 um	30 ps	22ps
90 nm	22 ps	33ps
70 nm	18 ps	16 ps
50 nm	45 ps	27 ps

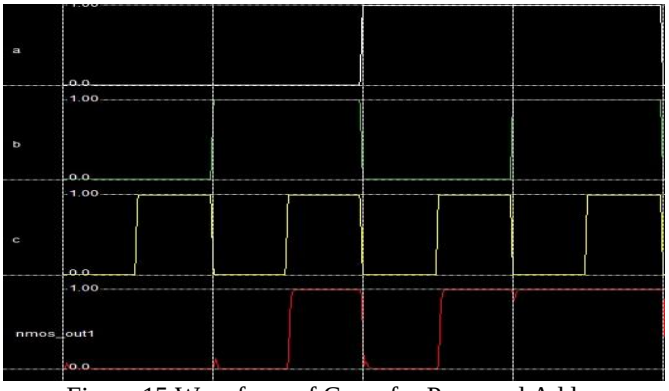

Figure 15 Waveform of Carry for Proposed Adder

Table 5: Simulation Result Of Proposed Adder For Different Technology and Voltage Range For Carry

Technology	Delay in Ps	
	Temp 27 ^{0}C	**Temp 70^{0}C**
0.12 um	30 ps	22ps
90 nm	22 ps	33ps
70 nm	18 ps	16 ps
50 nm	45 ps	27 ps

Table 6: Simulation Result of Previous Adder for Delay [7]

Design	Delay in Ps
	Temp 70^{0}C
C-CMOS	542
Hybrid	862
14 T	57
10 T	48.2
SERF	49
XOR 4T based	46

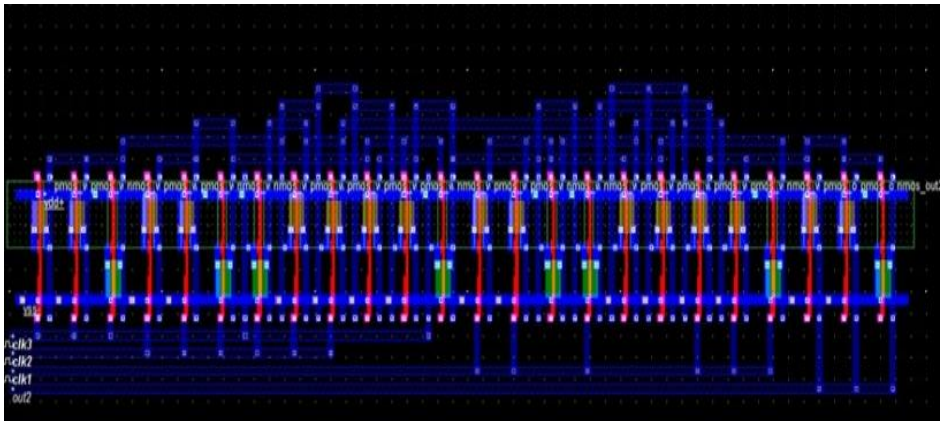

Figure 16 Layout of Sum for Proposed Adder

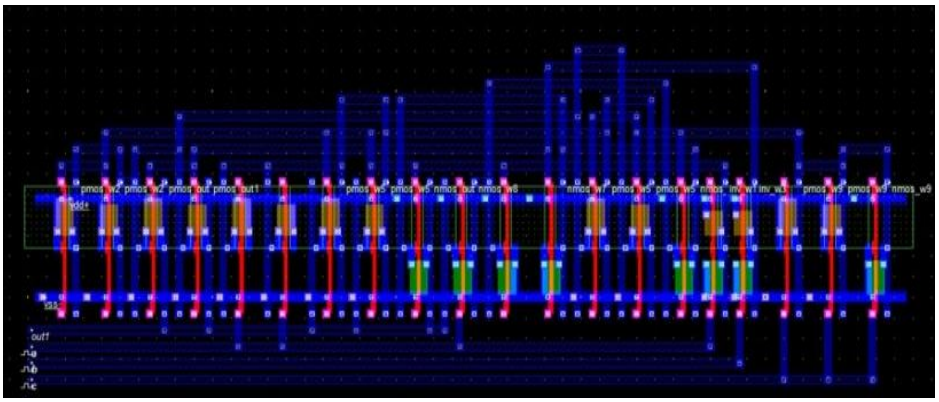

Figure 17 Layout for Carry For Proposed Adder

Figure 14 and 15 shows the sum and carry waveform for proposed self checking adders. By observing the simulation result obtained in table 4 and table 5 we can see that the designed self checking adder have reduced delay then table 6 and a better power delay product.

VIII. CONCLUSION

The newly designed full adder is an example of hybrid-CMOS design style. Pass transistor with CMOS logic are presented in this paper that targets reduced delay and Power delay product with adder having self checking property An performance analysis in terms of delay and self checking property has been presented for of 1-bit full adder cell ,the result is been compared with different adder logic styles. An delay optimized design of this self checking adder cell for an adder will certainly, improve the performance (delay , speed , power delay product, self testing) and reduce the hardware overhead and also making the adder circuitry totally self checking.

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