Volume 4, Issue 8, August 2014 ISSN: 2277 128X
International Journal of Advanced Research in Computer Science and Software Engineering
Research Paper
Available online at: www.ijarcsse.com

Novel SIPO Shift Register using Reversible Logic Gates

A. Anjana
Department of Electronics and Communication,
Adhiparasakthi Engineering College
India

Abstract— Design of shift registers opens the door for large memory than individual flip- flops. Shift registers are designed so as to support large sequential circuitry. The shift registers acts as temporary storage in the processor unit. The shift register, in this paper, is proposed with reversible logic gates. The Serial In Parallel Out (SIPO) shift register is implemented by connecting the RS flip- flop in serial order to feed the input and the output is extracted in the parallel order. Time delay of the reversible Shift register is much minimized in the order of 11.373ns with the reduced power consumption of 203.27mW.

Keywords—Reversible logic gates, RS flip- flop, Shift Register.

I. INTRODUCTION

Shift registers are used in the processor for the temporary data storage with high speed when compared to the main memory. Use of large number of registers regulates the speed of the calculation drastically at higher rate. Shift registers are used as a storage device in the various circuitries in the place of state machines, counter, serial to parallel convertor, parallel to serial convertor, communication and beyond. The SIPO shift register proposed in this paper is implemented using the reversible logic gates. The shift register require reversible memory circuits. The use of the reversible logic gates provide error free output for the given binary input data bits [1]. Therefore, reversible SIPO shift register proposed in this paper provides reduced delay and low power dissipation.

II. REVERSIBLE LOGIC GATE

Reversible logic gates are those in which the number of input is same as that of the number of output. The design of RS flip- flop is performed using reversible logic gates which are much effecient than the conventional logic gates. The reversible logic gates are those which poccess the charecteristics of zero error. The reversible logics namely TNORG gate and Toffoli gate are used in the design of RS flip flop [2]. The reversible logic gates pocesses the garbage values that are used to retrive the input data from the output without any loss in the data. The reversible logic gates has thew input and output combinations as shown below.

Input vectors = Output vectors + Garbage values

The unused output vectors are called as the garbage values. These garbage values are used to retrive the input data from the output vector without any loss in the information [3].

III. RS FLIP FLOP

RS flip flop server as a memory unit which generates four output bit such as high, low, don't care and invalid. It can be constructed by using the cross coupled pair of NOR logic gates. The SR flip-flop provides forbidden output at the state of both S and R tends to be high. This design of RS flip-flop is performed using the reversible logic gates. The reversible logic gates reduce the delay and the power consumption of the flip-flop. These are also said to be the error free gates. When compared to D flip flop implementations for shift registers, the RS flip flop are much efficient. The RS flip flop is designed with the reversible logic gates such as TNORG gate and Toffoli gate. The reversible logic gates provide the efficient use in the manipulation of the data without any loss in the information [2]. This zero loss of information in the design of a combinational logic gates provides an efficient architecture for memory unit.

IV. SIPO SHIFT REGISTER

SIPO shift register is also used as a serial to parallel converter. The use of RS flip flop for the design of SIPO shift registers provides reduces delay of 11.373ns with the power consumption of 203.27mW. SIPO reversible shift register is designed using the SR flip flop. To design a shift register for 4 bit input data we use the connection in the cascade order. Cascading of the reversible logic is the only cheapest way to get the low quantum realization [4]. In this architecture the input is feed in the order of serial way and the output is obtained in the parallel order.

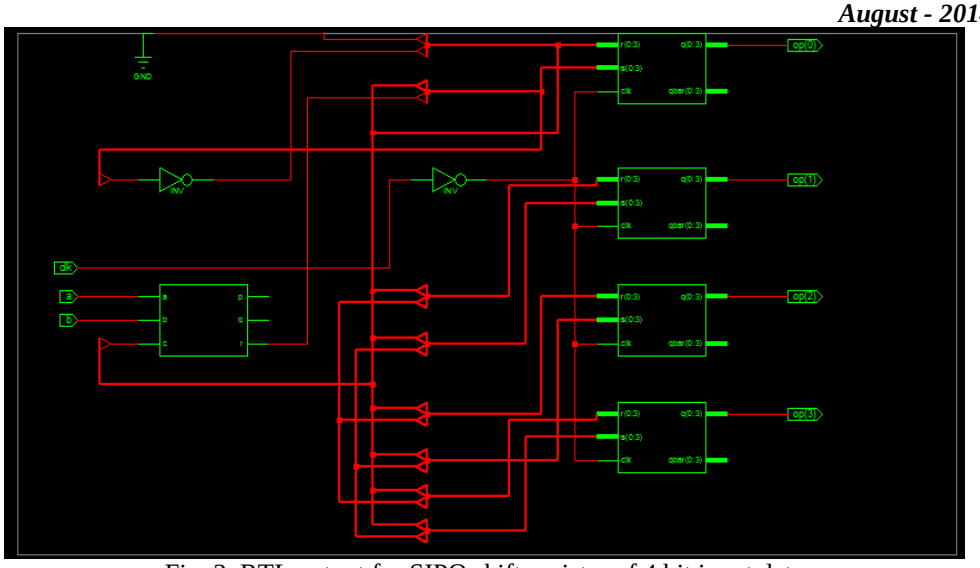

Fig. 2 RTL output for SIPO shift register of 4 bit input data

We infer the architectural design of the SIPO shift register using the reversible logic gates. From fig.2 the design of 4 bit input data of shift register is performed using the toffoli gate and TNORG gate is synthesised.

TABLE I: Synthesis Report For Reversible SIPO Shift Register

Device utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of slices	4	14752	0%
Number of 4 input LUT's	10	29504	0%
Number of bonded IOB's	7	250	2%

The power consumption was estimated to about 203 mW when the junction temperature of the each Field Effect Transistor is about 29 deg C. The delay for 4 bit reversible SIPO shift register is estimated by implementing using the reversible TNORG and Toffoli gate minimizes the latency to about 11.373 ns which is synthesized using 'Xilinx'.

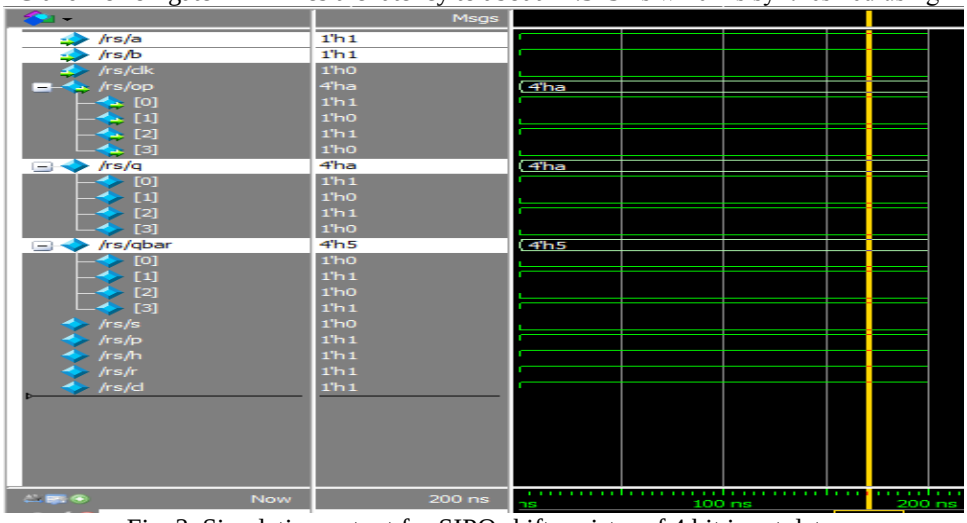

Fig. 3 Simulation output for SIPO shift register of 4 bit input data.

From fig. 3 represents the simulation output of the reversible SIPO shift register for 4 bit input data. The clock signal is fed in the combinational logic gates with the synchronous clock signal. The proposed SIPO shift register is simulated.

V. CONCLUSIONS

In the proposed paper, the design of SIPO reversible shift register is designed using the RS flip flop. Reversible logic gates used in this proposed architecture are Toffoli gate and TNORG gate. The reversible logic gates are those, which generates the output with much efficiency without any loss in the output data and requires low power consumption for manipulating the input data of 4 bit input data. This proposed reversible SIPO shift register is used effectively in the sequential logic gates for the purpose of memory unit with zero loss of information. This proposed architecture requires very less number of gates of about 18 reversible logic gates. The power consumption is estimated about 203.27 mW and the delay is about 11.373 ns. It is concluded that, this proposed architecture is much efficient than that of the conventional SIPO shift registers.

REFERENCES

[1] Madhusmita Mahapatro, Sisira Kanta Panda, Jagannath Satpathy, Meraj Saheel, M.Suresh, Dr. Ajit Kumar Panda and M K Sukla, "Design of Arithmetic Circuits Using Reversible Logic Gates and Power Dissipation Calculation", International Symposium on Electronic System Design, 2010.

[2] A.Anjana, "Design of RS flip flop using reversible logic gate", IPASJ International Journal of Electronics & Communication (IIJEC), Volume 2, Issue 4, April 2014, pp 6-8. .

[3] Anindita Banerjee and Anirban Pathak, "An Algorithm for Minimization of Quantum Cost,"Appl. Math. Inf. Sci. 6, No. 1, 157-165 (2012)/ www. naturalspublishing.com /amis/.

[4] C.S. Wallace, "A Suggestion for a Fast Multiplier", IEEE Transactions on Electronic Computers, EC-13, p.14-17, 1964.

