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Design and Simulation of Fpgas Based Digital Multi Channel Analyzer for Nuclear Spectroscopy Application

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Abstract— This paper describes the designing and simulation of Field Programmable Gate Array's based digital multi channel analyzer (MCA) circuit used in nuclear spectroscopy. Complete circuit was designed by writing appropriate program in Very High Speed Integrated Circuit Hardware Description Language & ISE foundation 6.1i. Maximum frequency of our designed MCA was 331.675 MHz with a minimum period of 3.015 ns. 62 slices out of 3584 were used. The designed system was simulated using Modelsim simulator SE 6.3 f. Our system can be implemented on Xilinx Spartan 3 XC3S400~4pq208.

Keywords— VHDL, FPGAs, Nuclear spectroscopy, Multi channel analyzer, Pulse height analysis.

I. INTRODUCTION

In nuclear physics experiment nuclear particle interact with detector and produces a pulse. By measuring the height of pulse, energy of particle can be estimated and the process in known as Pulse height analysis [1] [2]. Traditionally pulse height analysis process is realized by analog circuitry like integral Discriminator, Single channel analyzer (SCA), Multi channel analyzer (MCA) etc. But in analog circuitry hardware manipulation is necessary to adjust the measuring parameters which is either not possible all the time or difficult. At the same time analog system relies on resistors, capacitors and inductors; its stability is limited to their tolerance. In addition, as a compact alternative to bulky analog electronics, digital processing is of great benefit in many applications. Digital signal processing systems are flexible and easily upgradable. It is not only easy to implement mathematical algorithms but performance is also exactly repeatable [3]. Emerging high level hardware description and synthesis technologies in conjunction with Field Programmable Gate Array's (FPGAs) have significantly lowered the threshold for hardware development; opportunities exist to integrate these technologies into a tool for exploring and evaluating micro-architectural designs [4]. The use of hardware description languages (HDLs) allows FPGAs to be more suitable for different types of designs where errors and components failures can be limited. Embedded circuits can be designed using Very High Speed Integrated Circuit Hardware Description Language (VHDL) and can be implemented on FPGAs. Because of their advantage of real-time in-circuit reconfigurability, the FPGAs based digital systems are flexible, programmable and reliable [5] [6].

In this paper we present a detailed description of the designed digital MCA on reconfigurable platform FPGAs. It is assumed that preamplifier output signal is first acquired using high speed Analog to Digital Converter (ADC) and then it is processed and analyzed by FPGAs based digital MCA unit. Section II briefly describes the theoretical description of analog MCA. Section III presents the digital FPGAs based MCA along with the associated Datapath unit and Control unit. The operations performed by the different section of both the units are described in detail. VHDL implementation and basic procedure utilized for verification is discussed in section IV. Section V presents the schematics, simulation results, device utilization summary and Timing report of various units. In section VI result obtained from simulation are presented and section VII concludes the paper.

II. MULTI CHANNEL ANALYZER

In terms of internal functioning, multi channel analyzer (MCA) is quite different from SCA. MCA is modified version of SCA. It performs the same task with a number of threshold windows. Thus it eliminates the need to count pulses at each threshold window individually, making the process faster and less vulnerable to uncertainties related to time variations in radiation flux. Fig.1 shows a simple block diagram of a MCA. The MCA records and stores pulses according to their height. Each storage unit is called a channel. It is constructed using ADC's combined with memory that is equivalent to thousands of SCA's and counters. It digitizes the input signal for analysis as opposed to the all-analog processing by SCA's. The ADC converts the pulse height into a digital number. Each digitized pulse is in turn stored in a particular channel corresponding to certain energy. The distribution of pulses in the channels is an image of the distribution of the energies of the particles [7]. The memory contains the energy spectrum. At the end of a counting period, the spectrum that was recorded may be displayed.

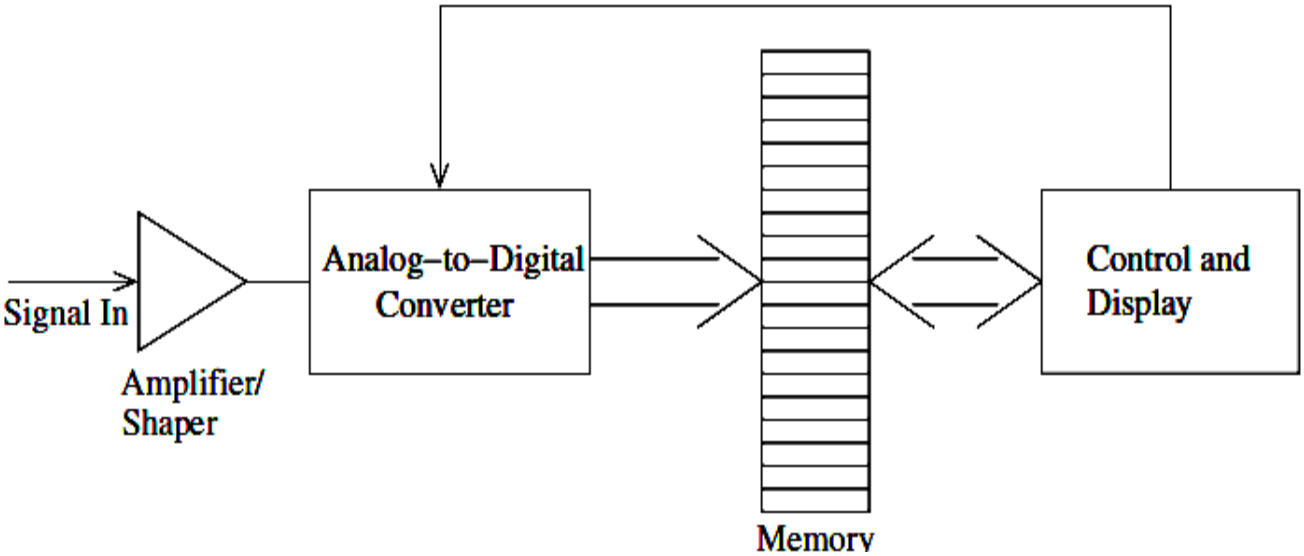

Fig. 1: Block diagram of a Multi channel analyzer [7].

III. FPGA BASED DIGITAL MCA

The detailed theory of analog MCA with suitable diagram is given in section II. In this section, we had manually designed the FPGAs based digital MCA for counting the pulses which fall above the predefined energy levels. Our designed system has two main units: Datapath unit and Control unit.

A. Algorithm Description

A following mentioned sequence of operations is performed each time when pulse is analyzed:

- 8-bit data from ADC is accepted by comparator unit and checked for the presence between the five predefined levels.
- Outputs of comparators are transferred towards appropriate logic units to produce logic pulses.
- These logic pulses are counted by counter unit and result is displayed in binary form.

B. Units required to implement FPGA based digital MCA unit

After analyzing the algorithm presented in subsection III-A, we conclude that the following functional units are required for the designing of Datapath unit and Control unit.

- An 8-bit ADC interface unit (UA)
- An 8-bit comparator unit. (U0)
- Four 1-bit logical units. (U1,U2,U3,U4)
- Four 1-bit buffer units. (U5,U6,U7,U8)
- Four 4-bit counter units. (U9,U10,U11,U12)
- A finite state machine (FSM).

C. Datapath unit of digital MCA

Schematic of our designed dedicated Datapath unit for FPGAs based digital MCA is shown in Fig.2. It contains all the processing units required for implementation of algorithm mentioned in subsection III-A.

Datapath unit for MCA was composed of 8-bit interface unit between ADC and comparator unit (UA), 8-bit comparator unit (U0), four 1-bit logical unit (U1,U2,U3,U4), four 1-bit buffer (U5,U6,U7,U8), and four 4-bit counter unit (U9,U10,U11,U12). An 8-bit interface unit (UA) between ADC and comparator unit (U0) has 8-bit input Adcin and 8-bit output Adcout. By asserting Adc_wr signal ADC data can be passed to comparator unit at rising clock edge. Output of 8-bit interface unit is connected to input of comparator unit. It has six 8-bit inputs, E1, E2, E3, E4, E5 and I1. E1, E2, E3, E4, E5 is predefined threshold level and I1 is connected to output of ADC interface unit. By asserting compload signal, the value at the input ports is loaded into comparator and compared for presence of data between predefined threshold values i.e. between E1 and E2, E2 and E3, E3 and E4 etc. Output of comparator is assigned to any one of four 1-bit outputs i.e. z1, z2, z3 and z4. Units U1, U2, U3 and U4 performs the logical AND operation. These units have 1-bit inputs A1, B1, A2, B2, A3, B3, A4, B4 and one 1-bit output C1, C2, C3 and C4 respectively. By asserting signal u1_load, u2_load u3_load and u4_load the value at the input ports are loaded and logical AND operation is performed on input data. Units U5, U6, U7 and U8 are tristate buffers. It has four 1-bit inputs as D1, D2, D3, D4 respectively and four 1-bit outputs as or1, or2, or3 and or4 respectively. It isolates the logical pulse from counter unit and logical units. It can be activated by asserting signals OE1, OE2, OE3 and OE4.

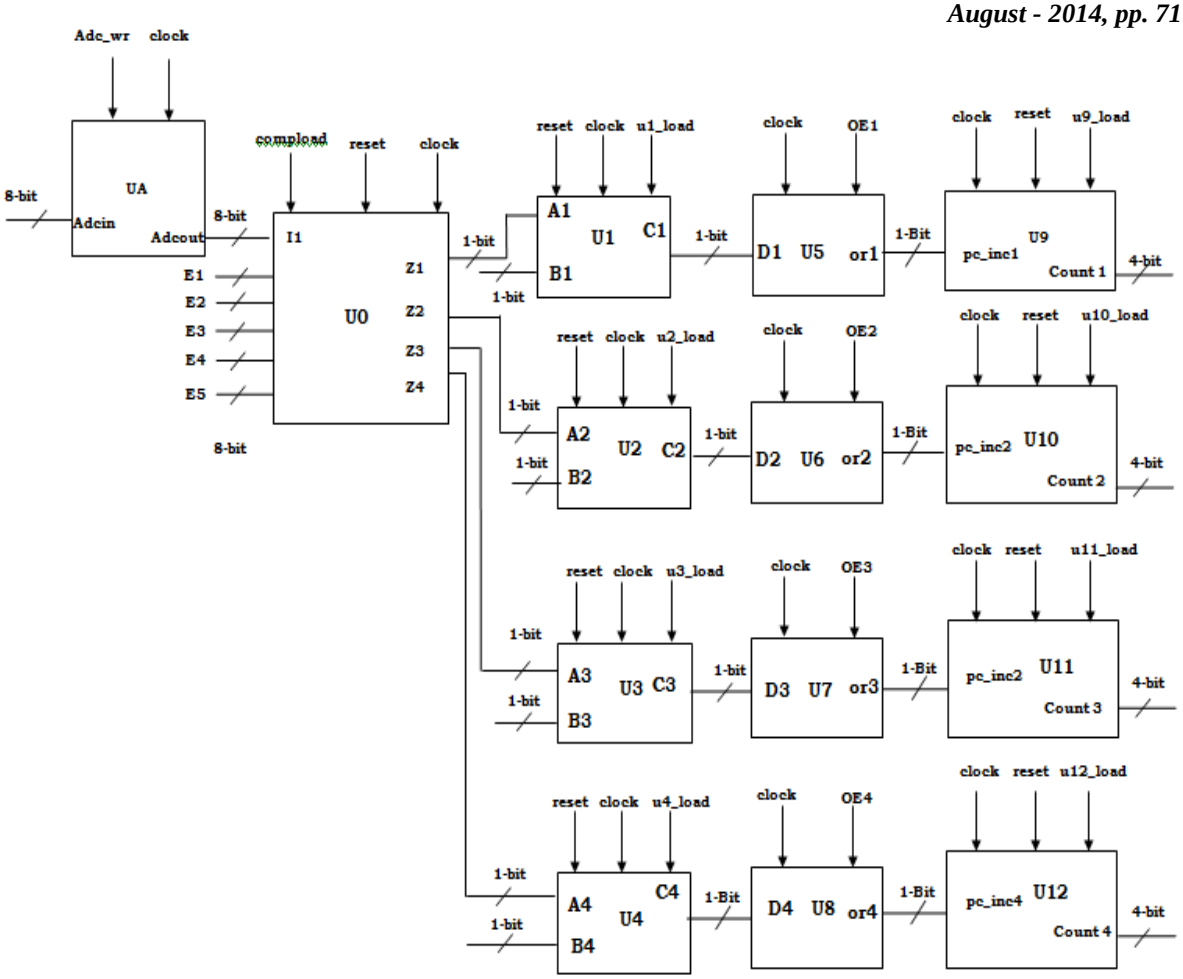

Fig.2: Schematic circuit of Datapath unit of FPGAs based Multi channel analyzer unit.

Units U9, U10, U11 and U12 act as a counter. Output from tristate buffer units act as input for these units. In presence of u9_load, u10_load, u11_load and u12_load these units are activated. Output is obtained in binary form.

D. Control unit of FPGA based digital MCA

Control unit of FPGA based digital MCA was composed of a finite state machine. It had 4 states; S0, S1, S2 and S3. Operation like initialization, comparison of data with predefined levels, generation of logical pulses and counting are performed during these states. The state diagram for the control unit of FPGAs based MCA is shown in Fig.3.

i. During state S0, initialization operation is performed. Signal reset is asserted high so that output of every unit must be zero.

ii. During state S1, interface unit UA is activated to accept the data from ADC and passed towards comparator unit by asserting signal adc_wr high. Unit U0 is also activated by asserting signal compload, which allow the comparator to compare input data with predefined inputs and produces outputs.

iii. During state S2, units U1, U2, U3, and U4 are activated. Logical input is provided by comparator and logical output is produced. These logical outputs is forwarded toward counter units U9,U10,U11 and U12 by activating buffer units U5, U6, U7, and U8 by activating signals u1_load, u2_load, u3_load and u4_load.

iv. During state S3, signals u9_load, u10_load u11_load and u12_load are asserted high to activate the counter units. After that control transfer from state S3 to state S1 unconditionally.

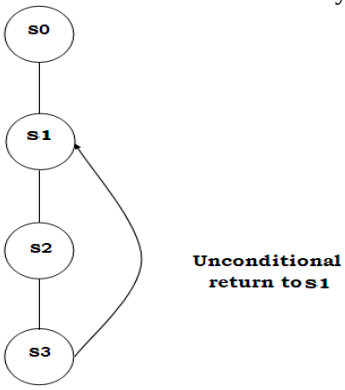

Fig. 3: State diagram for control unit of FPGAs based digital MCA.

IV. VHDL IMPLEMENTATION OF FPGAs BASED DIGITAL MCA UNIT

All the units related with Datapath unit and Control unit mentioned in section III were designed. These units were described in VHDL modules using ISE foundation 6.1i. Test benches had been written to test functionality of each module individually. The functionalities of each unit were verified by using Modelsim simulator SE 6.3f. Finally Datapath and Control unit was combined by writing appropriate codes in VHDL to form complete the digital MCA Unit. Finally designed digital MCA is synthesized by using synthesis tools provided in the Xilinx Webpack 6.1i. Again test benches had been written to test functionality of MCA unit. The designed system was simulated using Modelsim simulator SE 6.3f. Various aspects of designing parameter and timing are discussed with suitable schematic diagrams, waveform, circuit and time analysis reports in section V.

V. SIMULATION AND VERIFICATION

A. Datapath unit of FPGAs based MCA

The detailed description of the Datapath unit is given in subsections III-C. Portion of synthesis report presented below shows all the synthesizing units, device utilization summary and timing report. Fig. 4 shows schematic of the component used to construct Datapath unit. It is generated by Synthesize-XST tool of Webpack 6.1i. Table 1 presents the device utilization report of Datapath unit. It gives the estimation of resources utilized during the designing process. Timing Summary report of Datapath unit is presented in Table 2. The maximum operational frequency of designed unit is 331.675 MHz.

TABLE 1
DEVICE UTILIZATION SUMMARY REPORT OF DATAPATH UNIT OF FPGAS BASED DIGITAL MCA UNIT.

Selected Device: 3s400pq208-4				
Number of Slices:	59	out of	3584	1%
Number of Slice Flip Flops:	40	out of	7168	0%
Number of 4 input LUTs:	107	out of	7168	1%
Number of bonded IOBs:	94	out of	141	66%
Number of GCLKs:	2	out of	8	25%

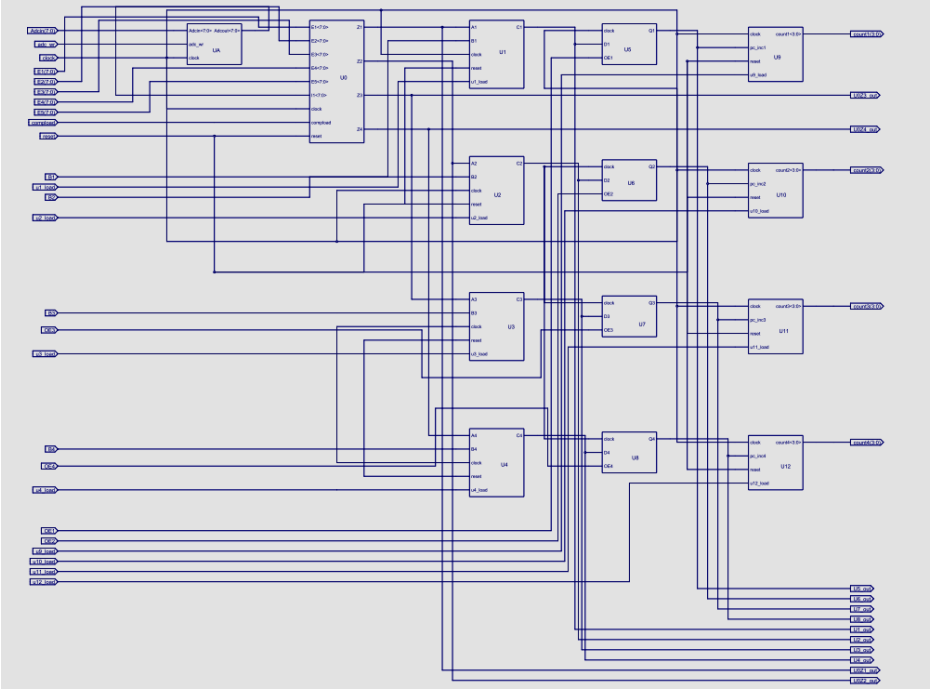

Fig. 4: Schematic of component of datapath of FPGAs based digital MCA Unit.

TABLE 2
TIMING SUMMARY REPORT OF DATAPATH UNIT OF FPGA BASED DIGITAL MCA UNIT

Speed Grade: -4
Minimum period: 3.015ns (Maximum Frequency: 331.675MHz)
Minimum input arrival time before clock: 8.287ns
Maximum output required time after clock: 6.716 ns
Maximum combinational path delay: No path found

B. Control unit of FPGA based digital MCA

The detailed description of the Control unit is given in subsections III-D. Fig.5 shows schematic of the component used to construct Control unit. It is generated by Synthesize-XST tool of Webpack 6.1i. Table 3 presents the device utilization report of Control unit. Timing report of Control unit is presented in Table 4. The maximum operational frequency of designed unit is 373.552 MHz.

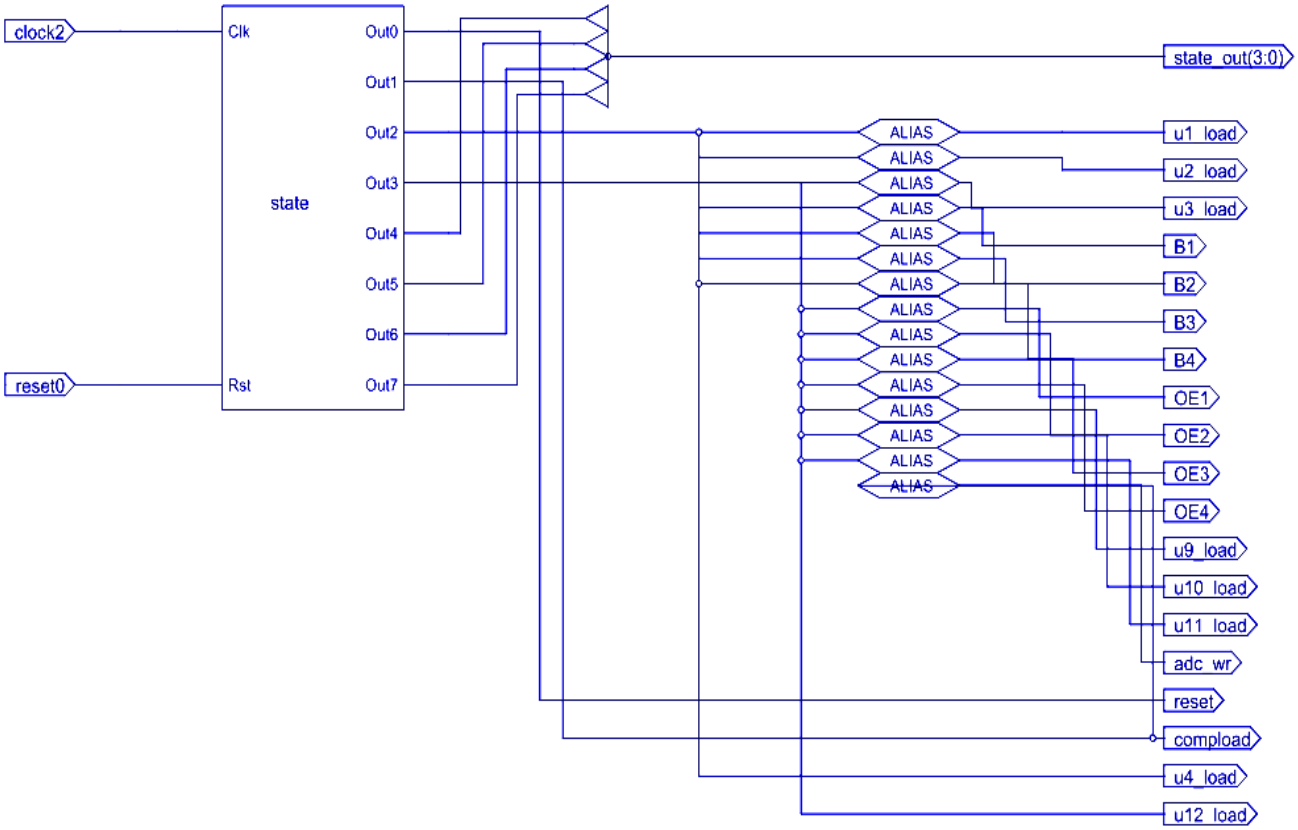

Fig. 5: Schematic of component of control unit of FPGA based digital MCA Unit.

TABLE 3
DEVICE UTILIZATION SUMMARY REPORT OF CONTROL UNIT OF FPGA BASED DIGITAL MCA

Selected Device: 3s400pq208-4				
Number of Slices:	3	out of	3584	0%
Number of Slice Flip Flops:	5	out of	7168	0%
Number of 4 input LUTs:	3	out of	7168	0%
Number of bonded IOBs:	24	out of	141	17%
Number of GCLKs:	1	out of	8	12%

TABLE 4
TIMING SUMMARY REPORT OF CONTROL UNIT OF FPGA BASED DIGITAL MCA

Speed Grade: -4
Minimum period: 2.677ns (Maximum Frequency: 373.552MHz)
Minimum input arrival time before clock: No path found
Maximum output required time after clock: 7.827ns
Maximum combinational path delay: No path found

C. FPGAs based digital MCA unit

The detailed description of the FPGAs based digital MCA model is given in section III of this paper. Fig. 6 shows schematic of the component used to design digital MCA unit. It is a combination of Datapath unit and Control unit. It is generated by Synthesize-XST tool of Webpack 6.1i. Fig. 8 shows the waveforms generated by the FPGAs based digital MCA unit. From the waveform proper functioning of designed units are confirmed. Table 5 present the device utilization report of FPGAs based digital Discriminator unit. It gives the estimation of resources utilized during the designing process. Timing report of FPGAs based digital MCA unit is presented in Table 6. The maximum operational frequency of designed unit is 331.675MHz.

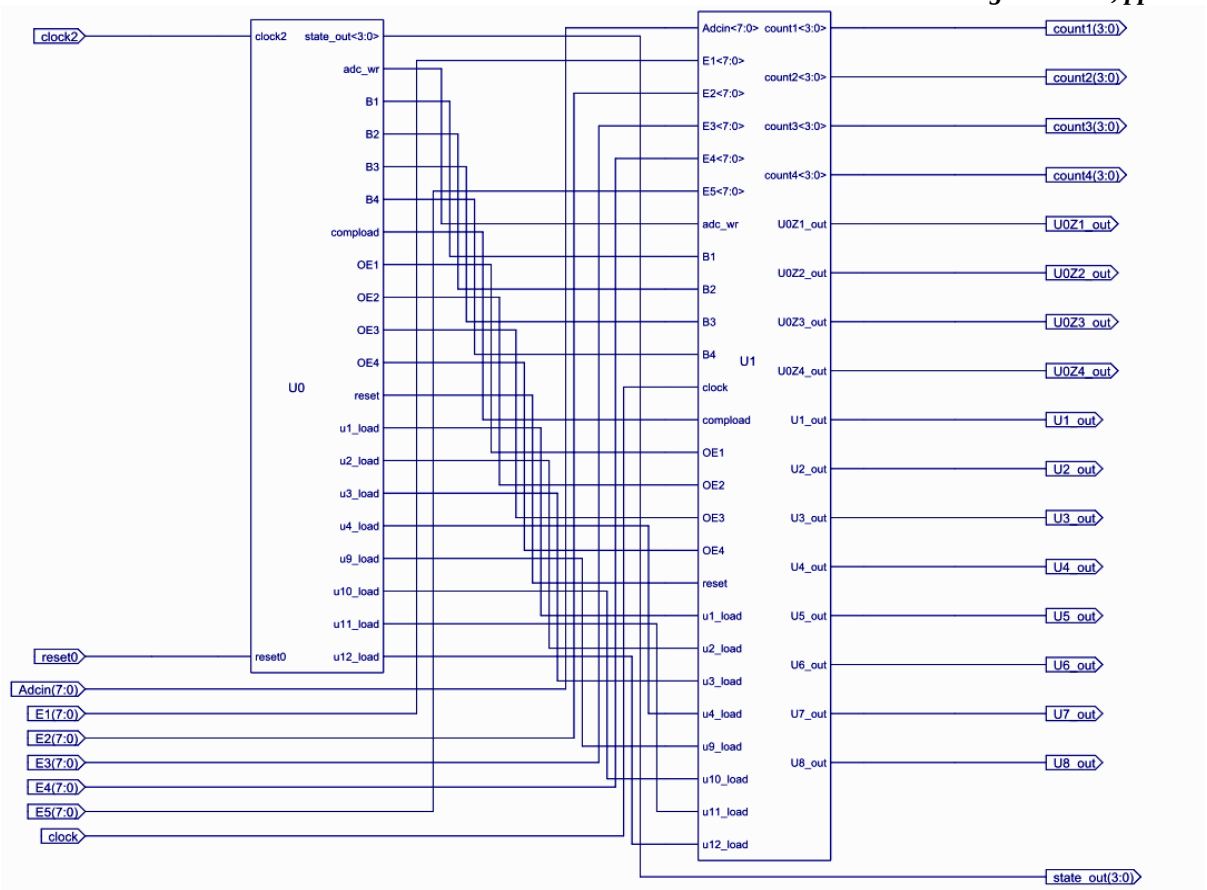

Fig. 6: Schematic of component of MCA Unit

Where U0 & U1 are datapath and control unit of digital MCA.

As an illustrative example, threshold values i.e., E1, E2, E3, E4 and E5 were set to 1V, 2V, 3V, 4V and 5V respectively. These threshold levels form the windows. Pulses fall within these windows were counted, else was rejected. Proper functioning of all designed modules was verified by simulating the digital systems by applying suitable test benches and checking the results with the help of waveforms generated by Modelsim SE 6.3f as shown in Fig.7.

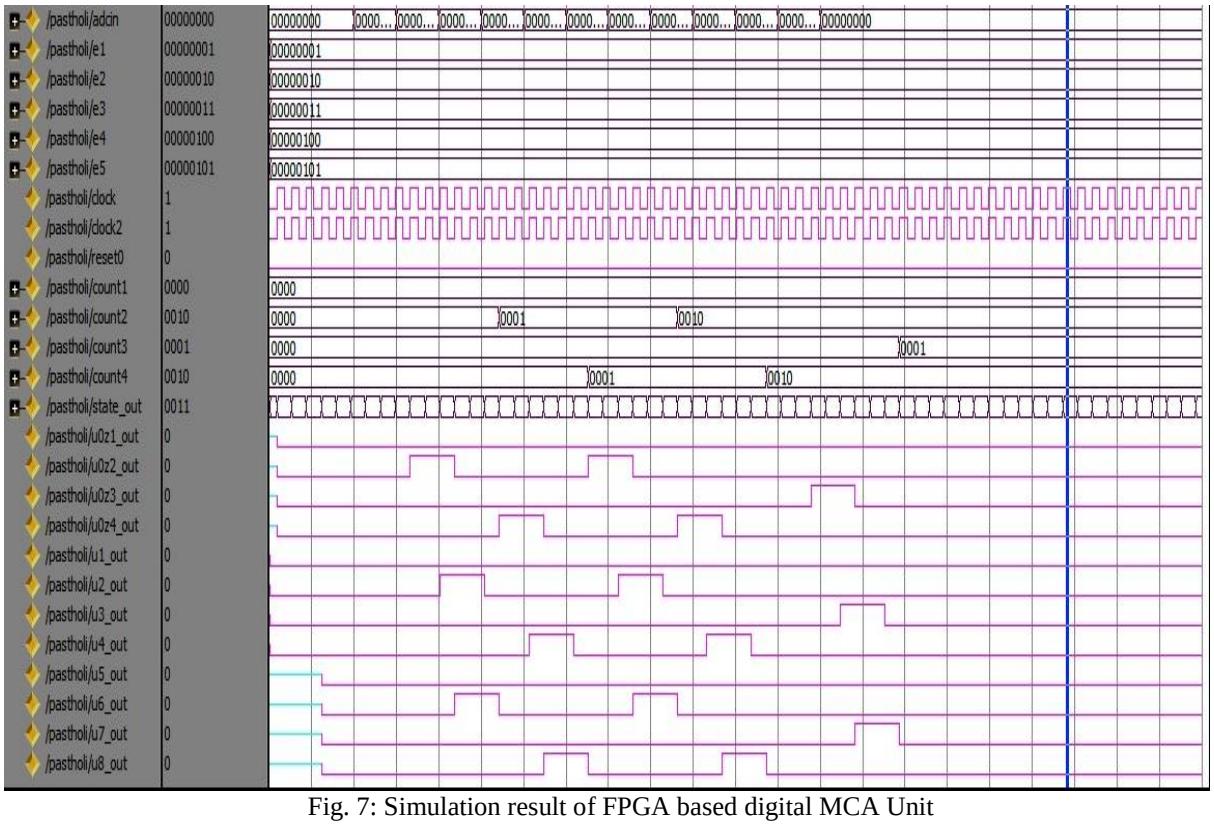

Fig. 7: Simulation result of FPGA based digital MCA Unit

TABLE 5
DEVICE UTILIZATION SUMMARY REPORT OF FPGAS BASED DIGITAL MCA UNIT

Selected Device: 3s400pq208-4				
Number of Slices:	62	out of	3584	1%
Number of Slice Flip Flops:	45	out of	7168	0%
Number of 4 input LUTs:	110	out of	7168	1%
Number of bonded IOBs:	81	out of	141	57%
Number of GCLKs:	2	out of	8	25%

TABLE 6
TIMING SUMMARY REPORT OF FPGAS BASED DIGITAL MCA UNIT

Speed Grade: -4
Minimum period: 3.015ns (Maximum Frequency: 331.675MHz)
Minimum input arrival time before clock: 8.287ns
Maximum output required time after clock: 7.916ns
Maximum combinational path delay: No path found

VI. RESULTS AND DISCUSSIONS

In this paper we described the principles, design, simulation and implementation of fully reconfigurable FPGAs based digital MCA. Designed digital MCA is made of Control unit and Datapath unit. The complete digital MCA is programmed inside a Xilinx Spartan 3 XC3S400 FPGAs by using ISE foundation 6.1i. Complete circuit is designed using VHDL and verified by using Modelsim simulator SE 6.3f. Datapath unit for MCA was composed of 8-bit interface unit between ADC and comparator unit, 8-bit comparator unit, four 1-bit logical units, four 1-bit buffer, and four 4-bit counter units. Its maximum operational frequency is 331.675MHz. Control unit is composed of a finite state machine. It has 4 states. Its maximum operational frequency is 373.552MHz. Maximum operational frequency of designed FPGAs based digital MCA is 331.675MHz.

VII. CONCLUSIONS

This FPGAs based system can replace complex analog MCA circuitry. It is based on measuring the height of pulses coming from detectors, which is proportional to energy carried by the particles. All of the processing blocks used in this simulation system were translated into a hardware system using VHDL. Each processing block in the proposed system can be easily modified without any modification in the hardware of system.

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