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FGMOS Based Current Mirror

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Abstract— Floating gate MOS (FGMOS) structure is suitable for low voltage applications owing to programmability of its threshold voltage. This paper presents FGMOS based circuit structures and their application as current mirror. Performance has been verified using PSpice simulation 0.5um CMOS technology at +/- 0.75 volts

Keywords— FGMOS, low voltage circuits, current mirror.

I. INTRODUCTION

The current trend in CMOS is to increase density and speed of digital circuit by making devices smaller. To increase driving capabilities of transistor the gate oxide thickness is also decreased. The reduction in thickness oxide requires that the supply voltage must be decreased to avoid excessive electric field in the devices. So the three main reasons for the advent of low voltage circuits can be summed up as:

1. In order to ensure device reliability the supply voltage has to be reduced (down to 1.5 V and below in the near future) as the channel length is scaled down into sub microns and the gate-oxide thickness becomes only several nanometers thick.
   The scaling of gate length also scales down the threshold voltage and as the off state current of MOSFET varies exponentially with the threshold voltage V_t , reducing V_t results in higher off state current.
2. The second reason arises because of increasing number of components on a single chip. Only a limited amount of power per unit area can be dissipated on a silicon chip. The increasing density of components allows more electronic function per unit area, so the power per electronic function has to be lowered in order to prevent overheating of the chip.
3. The third reason is dictated by battery-powered portable equipment's. In order to have an acceptable operation period from a battery, both the supply power and the supply voltage have to be reduced. Reduced power supply voltage requires some special circuit techniques are normally not an advantage for analog design.
   Therefore the challenge derived from market requirements is to reduce the power consumption of the circuit. Many new design techniques for low voltage analog circuits are available [3], for instance,(a) MOSFETs operating in the sub-threshold region(b) bulk driven transistors (c) self-cascode structures (d) floating gate MOS (FGMOS) (e) the level shifter techniques. This paper discusses characteristics of current mirror based on FGMOS.

II. CURRENT MIRROR

A current mirror is a circuit that produces a copy of current in one active device by replicating the current in second active device. Relatively high output impedance and low input impedance are important features as they help to keep output current and input current constant regardless of load conditions and drive conditions respectively. Ideally a current mirror is a current amplifier with a gain of -1. Current mirrors are often used as active load and to provide bias currents in amplifiers. The current mirror circuit basically converts the current entering the circuit into a voltage, and then this voltage is used to control current exiting the circuit [1,2].

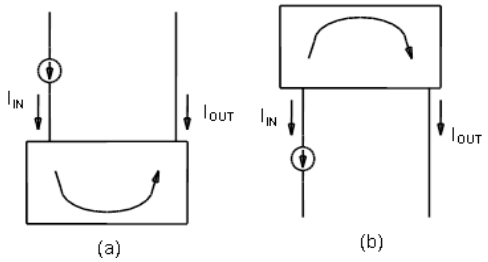

Fig (1) Block Diagram of Current Mirror.

III. FLOATING GATE MOSFET

The gate of a standard MOS transistor is electrically isolated for the fabrication of a standard MOS transistor. Floating gate has a number of inputs deposited above it, which are electrically isolated from the floating gate. Floating gate is completely surrounded by resistive materials and inputs are connected to it capacitively only. So in terms of DC operating point floating gate is a floating node [4].

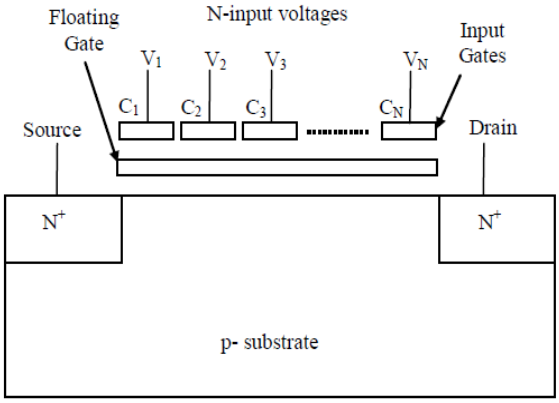

Fig (2) Structure of Floating gate MOSFET.

Structure of an N-input floating gate MOSFET is shown in figure(1). The input voltages are capacitively coupled to the floating gate of the MOSFET, these voltages modulate the channel current.

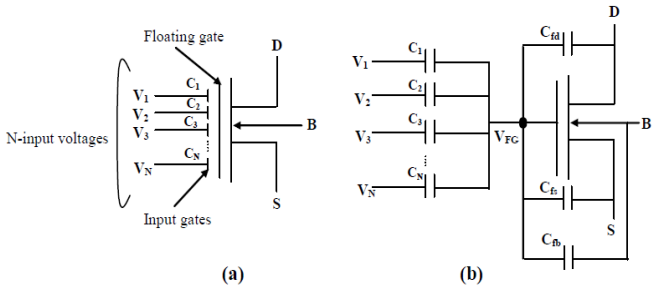

Fig (3) FGMOS Symbol and equivalent circuit model.

The Floating gate voltage (V_{FG}) is expressed as

$$V_{FG} = \frac{\sum_{i=1}^{N} C_i V_i + C_{fd} V_{DS} + C_{fs} V_{ss} + C_{fb} V_{bs}}{C_T}$$

C_1, C_2.....C_N : N input capacitances between control gate and floating gate.
C_{fd} : parasitic capacitance between floating gate and drain.
C_{fs} : parasitic capacitance between floating gate and source.
C_{fb} : parasitic capacitance between floating gate and substrate.
V_i : input voltage of i^{th} input gate.
V_{DS} : drain source voltage
V_{ss} : Source Voltage
V_{BS} : Substrate Source Voltage
C_T(Total capacitance):$\sum_{i=1}^{N} C_i + C_{fd} + C_{fs} + + C_{fb}$
The above equation indicates that the total potential on floating gate is linear sum of all input voltages (drain-source voltage, source voltage and source substrate voltage) weighted by capacitive coupling coefficients.
In case of a two input FG-MOSFET, a high DC voltage V_b is applied at one of the two gates trough C_{G1} and is called as bias gate, the input signal is applied at second gate through $C_{G2.}$ Assuming zero initial conditions and neglecting parasitic capacitances as compared to C_{G1} and C_{G2} , the gate voltage is
$V_{FG} = K_1 V_{in} + K_2 V_{bias}$
Where $K_1 = C_{G1}/C_{Total}$, $K_2 = C_{G2}/C_{Total}$
The new equivalent threshold voltage for MOSFET is given as
$V_{T,eq} = (V_T - V_b K_1)/K_2$
The above equation implies that $V_{T,eq}$ will be less than V_T if V_b, K_1 and K_2 are properly selected.

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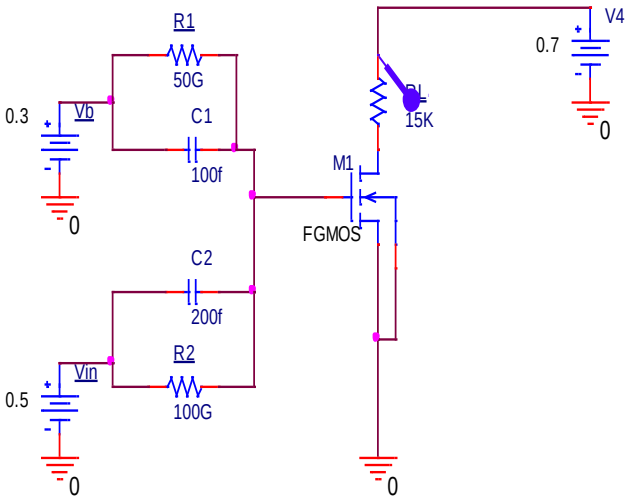
IV. PSPICE SIMULATION OF FGMOS

FGMOS simulation is carried out using ORCAD PSPICE for 0.35um technology. As PSPICE does not support floating gate, resistances are placed parallel to each capacitor. These resistances are selected in the range of giga ohms and capacitors are selected in the range of femto farad. A two input common-source FGMOS circuit shown figure(4) , is simulated by selecting C1 = 100fF, R1 = 50 Gohms, C2 = 200fF and R2 = 100 Gigaohms and W/L = 50um/1um using supply voltage of 0.75 volts and bias voltage of 0.3 V. Because SPICE cannot accept floating node which has no DC branch to ground, one resistor is added with each capacitor, which should have a value more than 10^{18} to minimize the loading effect to the circuit. Each branch should have the same time constant - which is the product of R and C, i.e.,$R_{G1}C_{G1}= R_{G2}C_{G2}=\ldots= R_{Gn}C_{Gn}= R_{FGD}C_{FGD}= R_{FGS}C_{FGS}= R_{FGB}C_{FGB}$ [5,6].
If the above condition stands, the DC voltage of the floating gate will not be affected by the introduction of the resistors.
The drain characteristics and transfer characteristics for different input signals are plotted in figure 5 and figure 6.



Figure(4)

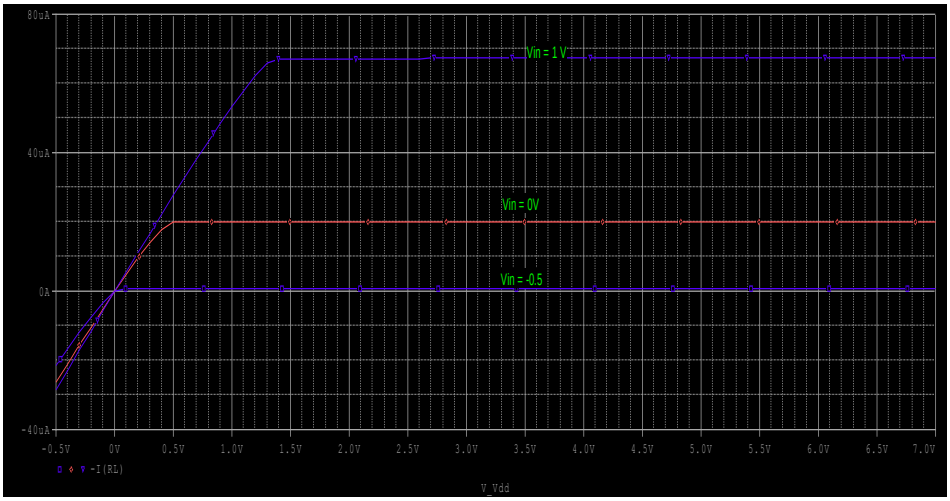


Figure (5) Drain Characteristics

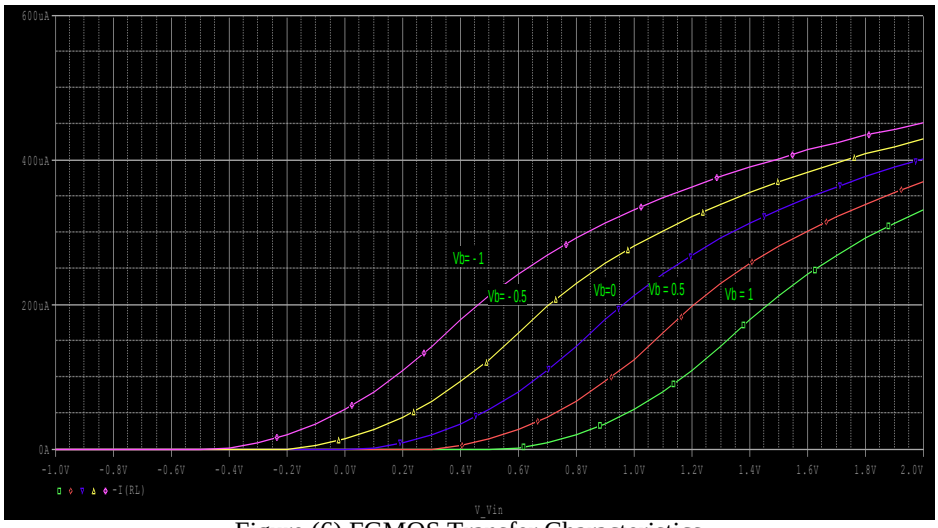


Figure (6) FGMOS Transfer Characteristics

The voltage at the bias gate of FGMOS enables us to vary the threshold voltage of the FGMOS and it can be observed that FGMOS can be operated at lower voltages (even negative voltages) as compared to conventional MOS

V. FGMOS BASED CURRENT MIRROR

A current mirror (CM) possesses properties of an ideal current source like zero input resistance and infinite output resistance. A CM produces a scaled version of input current.

A simple current mirror consists of two identical MOSFET's with equal gate source voltage as shown in fig (7)

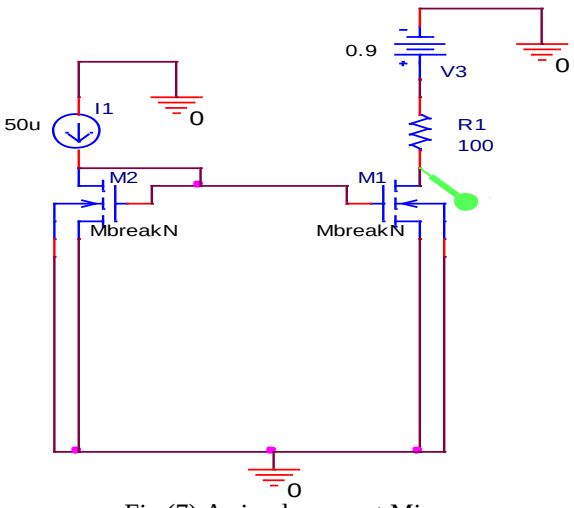


Fig (7) A simple current Mirror

The least voltage drop across M2 is given as:

$V_{in} = V_{DS2(sat)} + V_{T2}$

V_{DS1} : Drain –Source saturation voltage.

V_{T1} : Threshold voltage of M2.

It's value is very high in some low voltage applications.

FGMOS improves the performance of current mirrors in low voltage areas by programming its threshold voltage [7].

FGMOS based current mirror (FCM) is shown in fig (8)

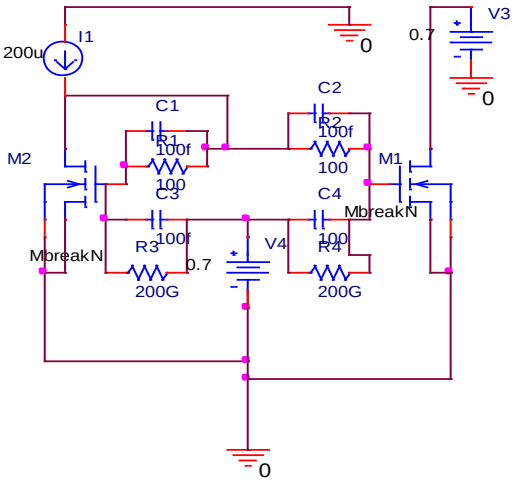


Fig (8) FCM

A FCM employs two input FGMOS where one of the gate terminals is used for signal processing purpose and the other is used for modulating the threshold voltage. The characteristics of FCM are verified through PSPICE simulation choosing Was 50 um and L as 1um at 0.75 supply voltage.

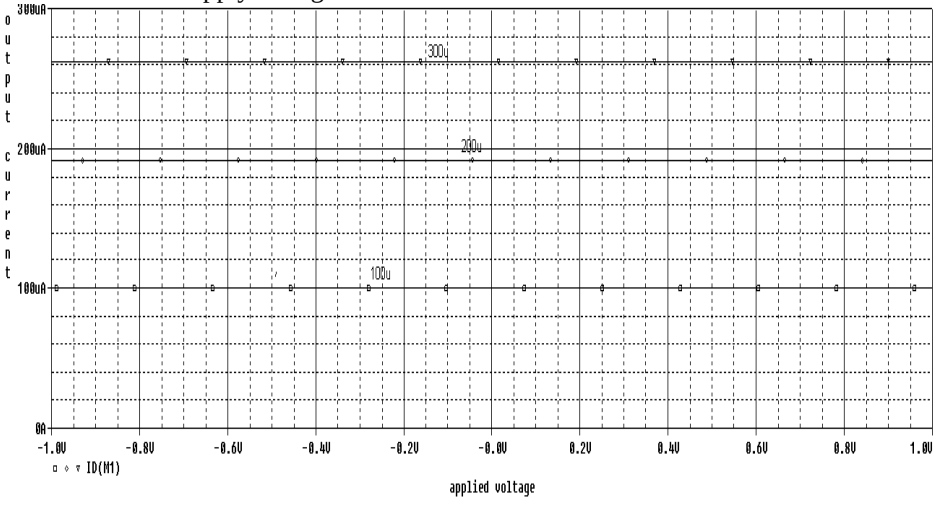


Fig (9) Output current v/s applied voltage

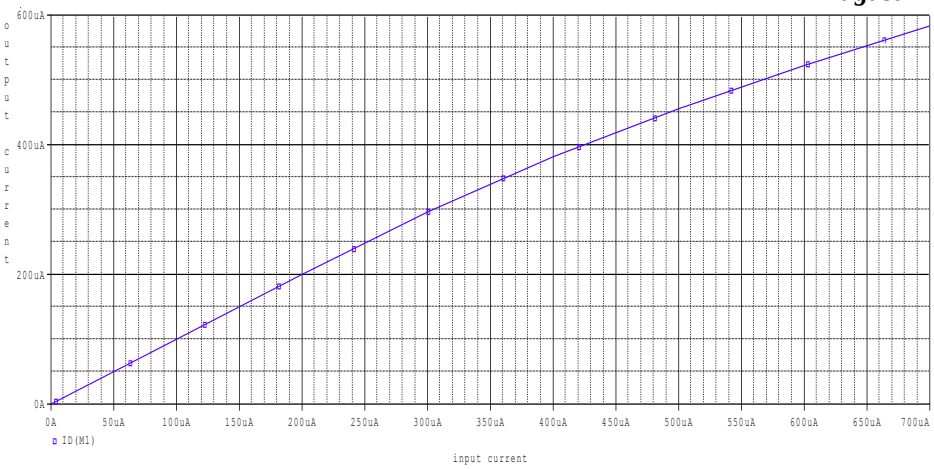


Fig (10) output current v/s input current

Fig(9) shows variation of output current with the input voltage, the plot was plotted for different values of reference input current and it was observed that the output current changes only with the reference input current. Fig(10) shows an almost linear relation between output and input current.

VI. CONCLUSION

This article shows characteristics of a promising Low Voltage technique i.e. FGMOS and its application in the fundamental building block of Analog Signal Processing element that is current mirror. Behavior is depicted through PSpice simulation

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