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Analysis of Power and Stability of 7T SRAM Cell

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Abstract— This paper addresses a novel seven transistor (7T) CMOS SRAM cell design to enhance the stability, reduce dynamic power, leakage power and area in various applications. The designed cell has an inbuilt mechanism for charge sharing, by which power has been saved for write operation. The proposed 7T SRAM cell uses charging/ discharging single Bit Line (BL) mechanism, which results in reduction in the dynamic power consumption. In this work the stability has been studied and calculated by N-curve method. The measured results have reduced 10.88% and 47.18% of leakage and dynamic power respectively. Moreover the area is reduced by 12.15%.

Keywords— Dynamic power, leakage power, stability, N-curve, static voltage noise margin, static current noise margin, write trip voltage, write trip current

I. INTRODUCTION

CMOS memories are traded as mass products worldwide and it satisfy nearly all practical requirements in operational speed, size, power and environmental tolerance [1]. Applications powered by battery such as calculators, hearing aids, military equipment drove low power electronics, requires prolong battery life [2]. A good power efficiency, which is a design goal for high performance system, can be achieved by lower power dissipations [3] i.e. by improving the performance of the circuit and to integrate more function into each chip.

In order to continue the growth of modern memory technology, it is important to increase the access-time speed while curbing the energy usage [4]. For faster access-time, new innovations in manufacturing processes and novel circuit designs are needed. Similarly, new efforts are required to control the power and energy consumption of storage, computing, and IT facilities and their cooling systems. Besides the environmental impact [5], excessive power consumption also reduces system reliability and increases cost of cooling. Effective power and thermal management will help to relieve the bottleneck of today‘s VLSI design and accelerate the growth of the information technology and many other similar industries [1]. It will also enable today‘s computing and communication devices to work efficiently with emerging energy storage and energy harvesting technologies to achieve energy autonomy [6].

The remainder of this paper is organized as follows: section II describes the existing architectures. Section III discusses the stability metrics. Section IV describes the proposed 7T SRAM cell and analyse its effectiveness. Section V discusses the analyses and simulation work between the cells presented & proposed cell, and finally in section VI draw the conclusion. Throughout this paper 90nm technology is employ for simulation.

II. EXISTING ARCHITECTURES

To overcome the read/write failure and achieve the high stability [7] at low supply voltage, various advanced SRAM cells have been presented. These advance cells provide the highest data stability [8], [9], the lowest leakage power consumption, high speed and the smallest memory cell. Various 6T, 8T and dual-7T SRAM cells are available in the literature, out of which some of the architecture of SRAM cell will be discussed in the section as follows.

A. ***Conventional 6t SRAM cell:-***Conventional 6T SRAM cell consists of 4 NMOS and 2 PMOS transistor, in which 2 NMOS is used as access transistor and rest MOS is compose of two cross couple inverter. Gate terminal of access transistor is connected to word line, which is used to select the cell. Source of access transistor is connected to bit-lines, which is used to perform write and read operation on the cell [3], [6], [10], [11]. The static noise margin of conventional 6T SRAM cell is improved by supply voltage, cell ratio and pull-up ratio. Drawbacks of cell are read and write failure.

B. ***8T SRAM cell:-***The read and write failure in conventional 6T SRAM cell is due to disturbance of bit line. The stability of 8T SRAM cell is enhanced by separating read port from the write bit line [6]. Read operation can used separate Read Bit Line (RBL) and write operation can used separate Write Word Line (WWL). It’s improved read and write noise margin and reduces leakage current.

C. ***7T SRAM Cell:-***7T Dual Vt SRAM cell simultaneously reduce active and standby mode power consumption and enhanced the circuit speed and data stability. Read operation is separated from the word line provides stability to cell

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[3], [6]. Write power is reduce due to utilization of single bit line for transfer of new data into the cell. Two separate signals WL and R lines are used to control write and read operation. It reduces area overhead of the 7T SRAM as compared to 8T SRAM cell, enhancing the read SNM up to 87% as compared to 6T SRAM cells and reducing the leakage power consumption up to 66%.

III. STABILITY ANALYSIS (N-CURVE)

The N-curve method is simple technique to find the stability of the cell. By using N-curve Fig. 1, four parameters (SVNM, SINM, WTV and WTI) are find which measures the write and read ability of cell [11]–[14].

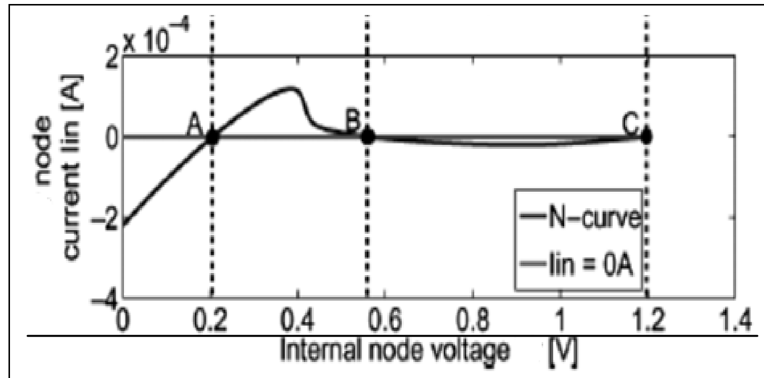

Fig.1 N-curve of SRAM cell [11]–[14]

For better read stability, the values of SVNM, SINM and the value of static power noise margin SPNM (product of mean of SVNM and mean of SINM) should be larger. For better write ability the value of WTV, WTI and the value of WTP (product of mean of WTV and mean of WTI) must be smaller [5], [11]–[14].

IV. PROPOSED 7T SRAM CELL

The schematic of proposed 7T SRAM cell, with transistors sized of 90nm is shown in Fig. 2. In the proposed circuit the charge has transferred from read to write bit-line to reduce the leakage current and dynamic power consumption. This design has not required the pre-charge circuitry for the write operation. Instead of this a write driver has used to drive the bitline either high or low, depending upon the input data. The read and write operations are controlled by Write Word Line (WWL) and Read Word Line (RWL) respectively. Bit Line (BL) & Read Bit Line (RBL) come in picture during write and read operation. There are two cases to study the working of proposed cell.

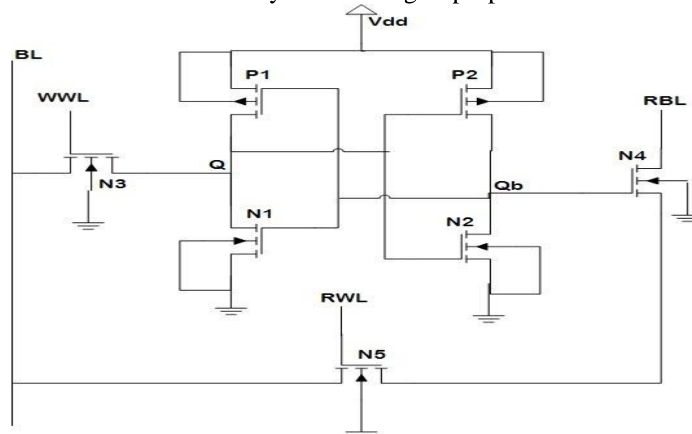

Fig. 2 Proposed 7T SRAM Cell

Case I: In the read operation, the RBL is pre-charge to Vdd. To start the read operation the read signal RWL transitions to Vdd while write signal WWL is maintained at V_{GND}. If a "1" is stored at Qb, RBL is discharged through the transistor N4 and N5 to bitline (BL). Alternatively, if a "0" is stored at Qb RBL is maintained at Vdd forming transistor stack. During read the charge is shared between read bitline (RBL) and write bitline (BL). The storage points (Q and Qb) are completely isolated from the bitline during a read operation.

Case II*:* In the write operation, the BL is already at a mid-level voltage, the write driver only has to drive it from mid-level voltage to full swing voltage. To start write operation, the write signal WWL transitions to Vdd while the read signal RWL is maintained at V_{GND}. The data is forced onto Q through access transistor N3.

In the read phase the charge is shared between the read bitline RBL and uncharged bitline BL during read '1' at Qb. Hence, it effectively reduces the write power. The transistor stack (N4 and N5) formation reduces leakage current (DIBL, Sub-threshold etc. [15], [16]).

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V. ANALYSIS AND SIMULATION WORK

N-curve analysis has been done at 90nm technology. N-curve of proposed 7T cell at 0.7V and 0.9V is shown in Fig. 3 and Fig. 4; there are different points on curve which give whole information as explain in section III. N-curve parameters of proposed 7T SRAM and reference cell [3] at different Vdd are shown in Table 1.

TABLE I
N-CURVE OF REFERENCE AND PROPOSED CELL

Parameter	Reference Cell at 0.9 V	Proposed Cell at 0.9 V	Reference Cell at 0.7 V	Proposed Cell at 0.7 V
SVNM (mV)	339.8	445.6	283.64	339.9
SINM (µA)	263.7	284.9	64.28	63.54
SPNM (µW)	43.216	63.47	8.12	11.43
WTV (mV)	436.8	454.5	336.5	359.8
WTI (µA)	–26.65	–30.09	–5.693	–6.59
WTP (µW)	5.82	6.84	0.96	1.11

Table 1 contain the stability parameter of reference cell and proposed cell. Fig. 5 to Fig. 8 shows the comparison of parameter between reference cell and proposed cell.

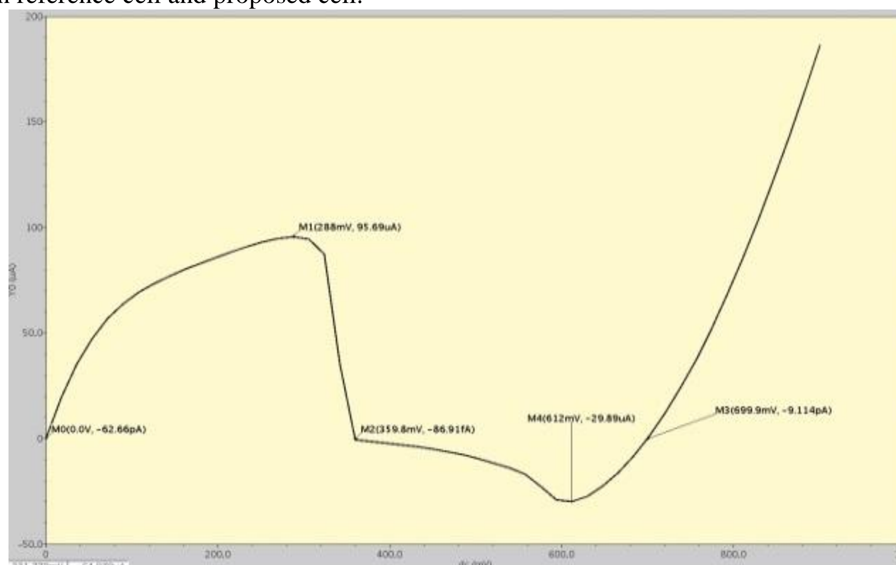

Fig. 3 N-curve of proposed 7T SRAM cell at 0.7V

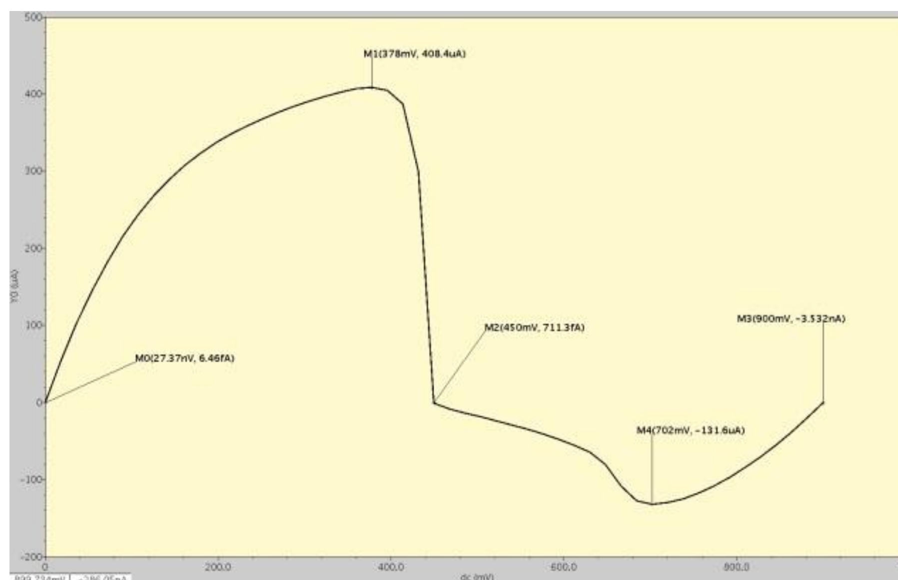

Fig. 4 N-curve of proposed 7T SRAM cell at 0.7V

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Fig. 5 to Fig. 8 shows the compared result of all N-curve parameters, we can see that the all parameters of proposed cell has high value as compared to reference cell that mean proposed cell is more stable then reference cell.

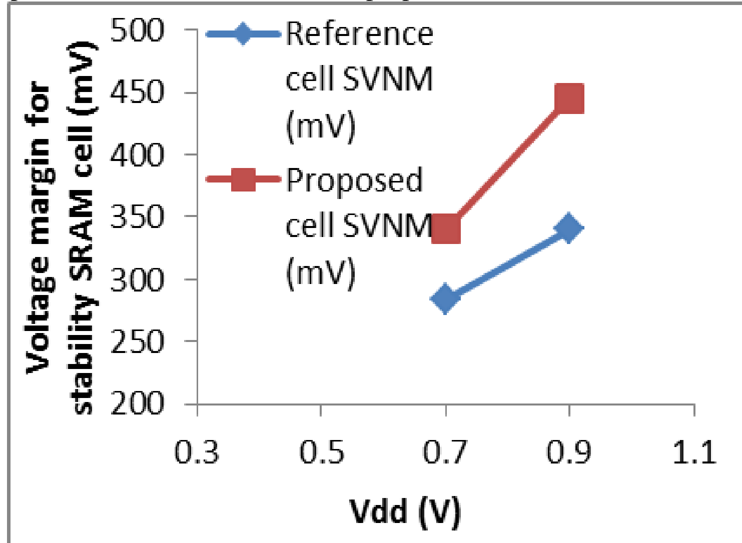

Fig. 5 SVNM of reference and proposed SRAM cell versus supply voltage

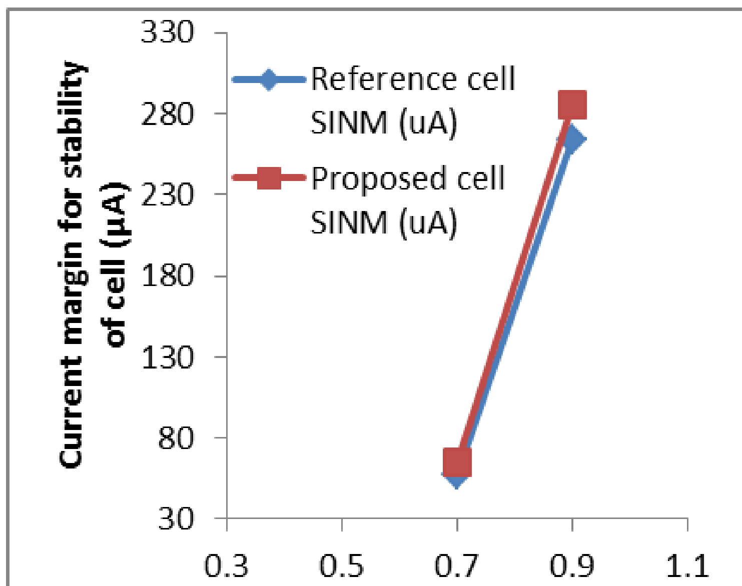

Fig. 6 SINM of reference and proposed SRAM cell versus supply voltage

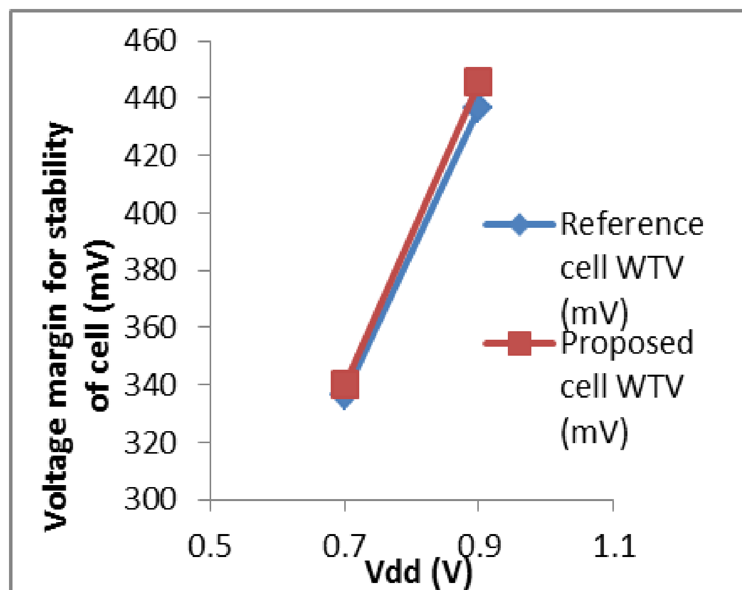

Fig. 7 WTV of reference and proposed SRAM cell versus supply voltage

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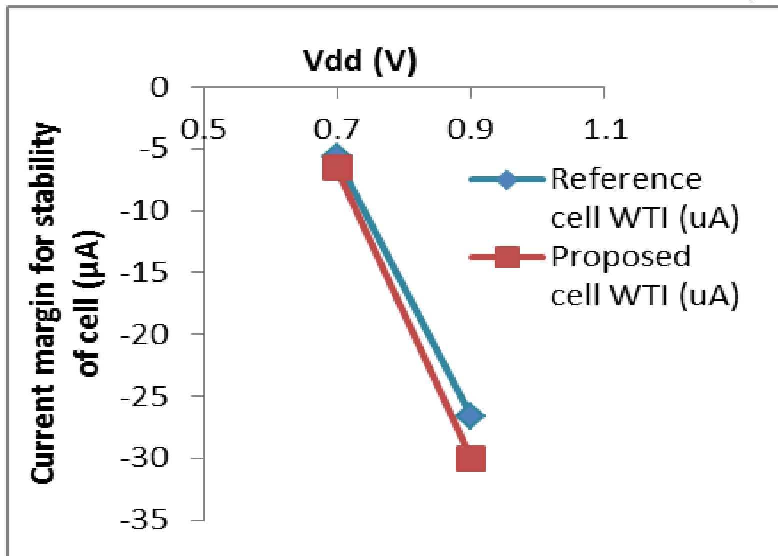

Fig. 8 WTI of reference and proposed SRAM cell versus supply voltage

Dynamic power loss [17] is due to switching of state. By reducing the switching and clock frequency, dynamic power is reduced [4]. The proposed 7T SRAM cell reduces the dynamic power 47.18% and static power i.e. leakage power 10.88% as shown in Fig. 9.

TABLE II
DYNAMIC AND STATIC POWER OF REFERENCE AND PROPOSED SRAM CELL

Parameters	**Reference cell at 0.9V**	**Proposed cell at 0.9V**
Static power (nW)	23.71	21.13
Dynamic power (µW)	8.35	4.41

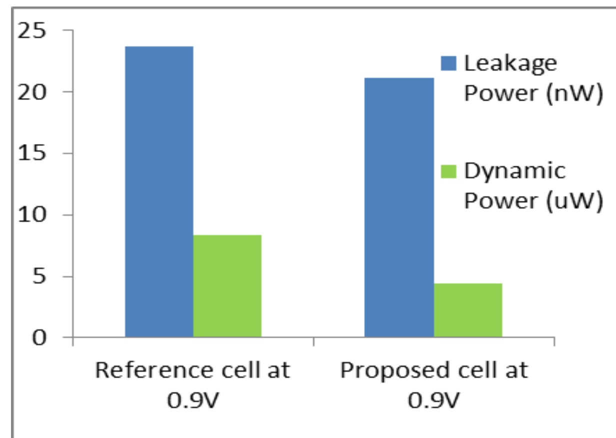

Fig. 9 Dynamic and Leakage power of reference and proposed SRAM cell at 0.9V

Area is also one of most important parameter, area increases with SRAM size more rapidly than access-time [6]. This higher rate of increase is mainly due to the addition of bank decoders, bank-interconnects, and several banks, each having their own main components [3] (such as row-decoder, pre-charge, etc.). Area of proposed 7T SRAM cell is reduce by 12.15% as compare to reference cell.

VI. CONCLUSIONS

A novel 7T SRAM cell has been presented with an inbuilt mechanism for charge sharing. This technique saves power for the write operation and enhances the stability. The compared results show validation of proposed 7T design approach. For stability N-curve is used which gives the information about read stability and write ability. With this proposed 7T SRAM cell dynamic power and leakage power are reduced by 47.18% and 10.88% respectively. Area has also reduced by 12.15%.

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