Volume 4, Issue 6, June 2014 ISSN: 2277 128X

International Journal of Advanced Research in Computer Science and Software Engineering

Research Paper

Available online at: www.ijarcsse.com

Implementation of Decision Making Sub-System Using SET and Hybrid CMOS-SET – A Case Study

Jayanta Gope
ECE Dept.
School of Engg. & Tech
India

Aloke Raj Sarkar
EE Dept
Camellia School of Engg. & Tech
India

Abhishek Bar
ECE Dept
Univ. Inst. of Tech The Univ. of Burdwan, India

Abstract— 'Decision Making' subsystems is a fascinating but challenging endeavour in modern technology involving human brain, previously adapted practices, improved and skilful knowledge of problem statement and integrating all with sophisticated logical synthesis in technological milieu. Numerous attempts in this regards have been reported in reputed scientific publications so far. The concurrent research trend articulates several decision making subsystems in smart phones, different switching systems, remote sensing panels and not but least in sophisticated computer systems. Several dedicated decision making software are in market. The very recent approach to incorporate nano-scaled decision making systems has attracted academics and industries worldwide; especially using Single Electron Device [SED] based decision making systems. One such model is reported here in this present context. Furthermore, the system is empirically tested on Monte-Carlo environment to make the highest exposure of the proposed model. Subsequently another alternative model is demonstrated to calibrate the result with the previous one. Both the models are then compared to achieve the best consequences and subsequently it is revealed that the second model is more viable.

Keywords— Hybrid, SET, MOS, SPICE, Decision Making sub-system

I. INTRODUCTION

"The decision making process is best served when uncertainty is communicated as precisely as possible, but no more precisely than warranted" – stated by Budescu and Wallsten 1987 [1]. Decision making subsystems when realized in hardware has – 1) the potential to enhance the quality of decisions accredited, 2) the talent to take decisions more rapidly, and 3) reduces the risks associated with making quality decisions. This is why research trend in this category has flourished manifold. The unmatched popularity of such subsystems has stimulated device engineers to integrate several prediction based software into smartphone.

Concurrently, a growing interest in the possibilities of designing electronic circuits using evolutionary technique is observed keenly. Since 2005 the introductions of single electronic tunnelling devices have received a great deal of attention both in terms of the physics of the coulomb blockade and for potential device applications. As revealed in different reputed scientific journals, Single Electron Tunnelling (SET) devices exploit effects that arise due to the quantized nature of change. These effects have been observed in several empirical studies made in different research labs and also in systems of small metal structures and in semiconductor structures made from conducting polymers. As these effects are ubiquitous in small structures, they certainly have greater control on any future nano scale electronic circuits. Henceforth, these devices are considered indispensible in low power circuits as only a few electrons are needed to be transported. Another distinctive characteristic of the SET technology that makes SET a promising candidate for future low-power ULSI/VLSI technology is that the charge transport occurs in discrete quantities, i.e., one electron at a time [2-6]. This has enormously augmented the capacity of the SET device designers to realize SET models where the transport of every particular electron needs to be precisely controlled.

SET posses a number of profits but also it has various open challenges to come with elegant solutions such as room temperature operation regarding fabrication techniques and mass production. Scientists then approached with a different research which further developed into a fundamental research area of solid state physics – called CMOS-SET hybridization. This technique has greater trade-off as such an integration offers new functionalities which are quite intricate to achieve either by pure CMOS or by pure SET approaches. Thus it is particularly significant to optimize the effects of energy quantization on hybrid CMOS-SET integrated circuits.

Here the authors intend to demonstrate a novel architecture based on SET for 'decision-making' and further studies are made for the empirical results based on Monte –Carlo equation of the structure. Subsequently the authors recombine SET structure with conventional TTL synthesis to derive the most effectual linkage amid SET and CMOS-SET hybrid circuit. The problem statement is attributed in the subsequent sections. The last section describes the comparative studies of the two propose structures so that to investigate the best and optimum design methodology.

II. SET IN TECHNOLOGICAL MILIEU

The intrinsic characteristics like generality and robustness of the effect and the relative simplicity of the device structures endorse the SEDs as the most likely candidate for future ultra dense digital circuits. The uniqueness lies in the fact that a single electron is sufficient to store a bit of information unlike CMOS transistors; thus the power consumption is drastically reduced. SEDs that let manipulation of single electrons are eventual forms of the electron devices. Their potential integration level is apparently high due to its small size. Extremely low operational power resolves various instability and reliability problems. The speed power product is predicted to lay proximity to the quantum limit set by the Heisenberg's uncertainty principle. The processing speed of such device is anticipated to be identical to electronic speed. Furthermore, the superb sensitivity is approximately five orders of magnitude which are far better than conventional solid-state MOSFET transistors. The integration density is much higher than that available in the existing CMOS based VLSI / ULSI circuits.

Presently, a growing interest in the possibilities of designing electronic circuits using evolutionary techniques has ushered new dimension in device research. In the decade long discovery of SET made SEDs, the design approaches have gained high popularity, both in terms of the physics of the Coulomb blockade and for potential device applications. SET devices, as envisaged have exploited underlying effects that arise due to the quantized nature of charge. These effects have been keenly observed in systems of small metal structures, semiconductor structures, and in structures made from conducting polymers. These devices are indispensably functional in low power circuits as only a few electrons are needed to be transported. Dense memories where bits are represented by the presence or absence of only a few electrons can also be realized with the use of single electron devices. An approach to such new devices can be built on the basic of the concept of binary decision diagrams. The unit function of this device is a simple two way switching. A binary decision diagram represents a digital function as a directed cyclic graph with each node labelled by a variable. It provides a complete and concise representation for most digital functions encountered in logic-design applications. This actually motivated us to realize some simple and also complicated digital circuits. All logical circuits starting from NOT gate to CPU of a digital computer can be realized with the help of single electron circuits [7-11]. Timing analysis together with propagation delay in case of single electron device based digital circuits can also be estimated.

There has been very few research attempts reported so far to mold this SET technology in a CMOS-like design style by realizing new SET based circuits that are truly identical to MOS circuits. But vis-à-vis the actuality that SET devices exhibit entirely dissimilar functioning than the MOS transistor, these efforts limits the talent of the technology itself. SET is recognized at its best only if its unique characters are noticeably exploited at all design levels, i.e., device, circuit and system i.e., SET's distinctive features needs to be explored and utilized fundamentally. Thus the approach for hybrid CMOS-SET architecture is of higher potential to study.

III. CONTROLLING OPERATION AND 'DECISION MAKING' OF AC MACHINE USING SET- A CASE STUDY

Let us consider the modus operandi of an air conditioning unit which is controlled by four variables; temperature T, humidity H, the time of the day D, and the day of the week W. The ac. machine is considered to be turned on under any of the following circumstances: -

1. The temperature exceeds 78°F and the time of the day is between 8 AM and 5 PM.
2. The humidity exceeds 85%, the temperature exceeds 78°F, and the time of the day is between 8 AM and 5 PM.
3. The humidity exceeds 85%, the temperature exceeds 78°F, and it is a weekend.
4. It is Saturday or Sunday and humidity exceeds 85%.

Thus the air conditioning machine is turned on, if the temperature exceeds 78°F and the time of the day is between 8 AM and 5 PM, or if it is a weekend and the humidity exceeds 85%. The realization of the decision making subsystem is as depicted in the Fig.1in the following.

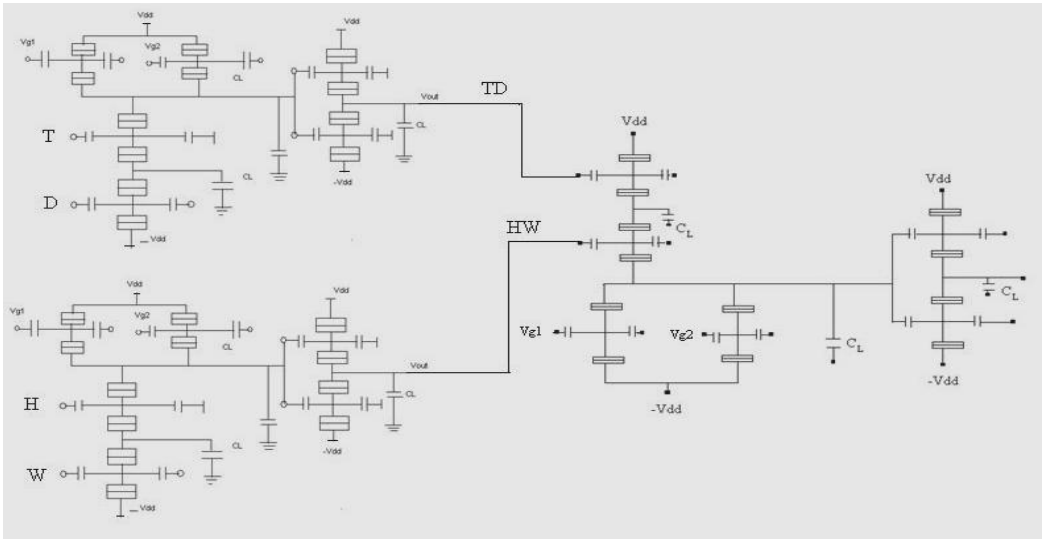

Fig. 1: Realization of the sequences for turning on the machine using SET

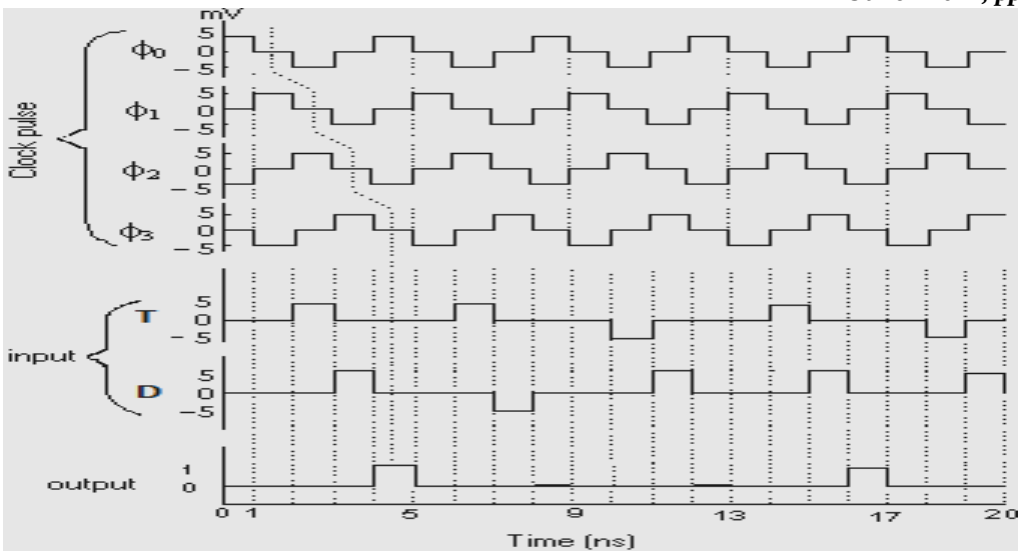

Fig. 2: Waveform of Fig.1

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A. The Inherent Merits Revealed Using SIMON

The model has been tested using SIMON, which is Monte-Carlo based simulation software. The results are partially depicted in Fig.2. It demonstrates the positional aspects and changes at different timing intervals. The graph shows better significance compared to its CMOS counterfeit.

Among other distinctive merits of SET include – (i) the e^- transmission in SETs are performed in one by one step; while many e^- all together participate in conduction of CMOS. (ii) it tenders greater scaling potential than CMOS as the device structure is quite simple. (iii) SET renders greater potential to realize circuits that can operate without consuming high energy than any other existing CMOS circuits. (iv) current advancement in silicon based fabrication technology enlightens the possibilities to realize SET circuits so that to operate in room temperature and (v) moreover, the tunnel junctions which are the basic circuit element of SETs reveals the potential to be fabricated in simplistic ways [12-16].

But, among several merits, SETs posses high output impedance and are sensitive to random background charges. This makes it improbable that SETs will someday replace CMOS-FETs in mass production based applications where large voltage gain or low output impedance is necessary. Other outstanding issues that prevent the exercise of SETs in most applications are the (i) low gain, (ii) the high output impedance and (iii) the background charges and (iv) room temperature operations [17-20].

Beside this, considering the merits of existing and highly proficient as well as much matured CMOS-FETs are – (i) high gain and current drive, (ii) invariably high speed, (iii) well established e-beam lithography based fabrication technology and (iv) huge research studies with empirical results are available; apparently the same studies revealed its sub-10-nm physical limits and power density like intrinsic limitations of it [21-23]. Thus the second approach of hybridizing CMOS with SET is being considered, although very few research attempts have been reported so far. Consequently, ample study is focused where a complete replacement of CMOS by SET is undoubtedly time consuming and more particularly it is not in proximity in very near future. On the other hand it is ardent fact that by combining SET and CMOS, i.e., by hybridizing CMOS-SET next level scientists and engineers can bring out new functionalities, which are not represented in pure CMOS technology as well as in SET technology. Such a 'co-integration' based structural approach also glides the sudden transformation of technology from CMOS to SET [24, 25]. Here the authors have motivated themselves to take this co-integration little apart by incorporating this technology in developing 'decision-making' sub-systems as the concept of hybrid CMOS-SET architectures has already captivated higher attention both in industry and academics. In this context we refer to Toshiba's successful demonstration of the performance of a hybrid MOS-SET inverter on a SOI wafer [26, 27] with improved gain at transition levels although the current drive remains low.

B. Modelling of Hybrid CMOS-SET Architecture of the Proposed Decision Making Sub-system

Recent developments reported in last few years reveal that researchers at Delft University in Netherlands recommended a SPICE simulation package for SET circuit [28-30] by incorporating the Orthodox theory of SET. The authors here adhere to the same SET-MOS quaternary transmission gate which are several times highly accredited and mostly cited in reputed journals. The co-integration model of the above cited case study were cautiously modelled and further simulated using SPICE soft-computing layout which allows maximum place sharing of SETs with the conventional MOS devices in one particular die area as explained in Fig. 3. More expediently, the logic operations of the projected circuit were periodically tested using T-Spice simulation software. Thereafter, the MIB compact model for SET device simulation and design was set and lastly the BSIM4.6.1 model for CMOS was incorporated for obtaining comprehensive empirical results which are briefly included in this presentation. Most interesting part of this model is that it has two basic differences, i.e., (i) the 'Pull Up' transistor is an SET and (ii) the V_{DD} is defined by the SET device parameters. The waveforms of Fig.3 are depicted in Fig.4 and Fig.5 respectively where final control is shown.

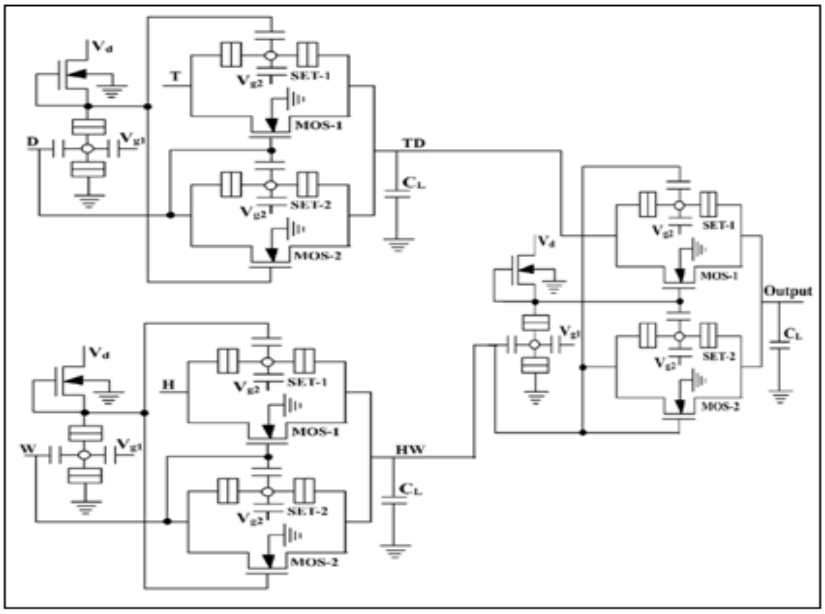

Fig. 3: Hybrid CMOS-SET model of proposed circuit

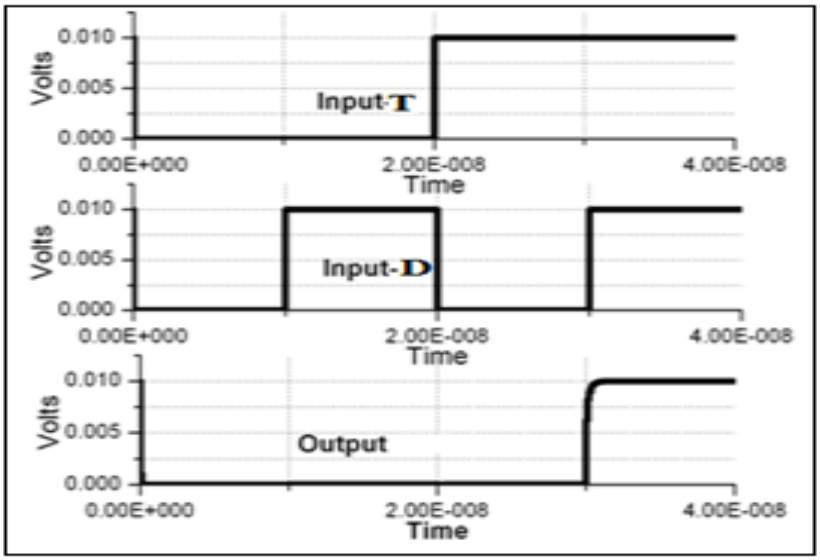

Fig. 4: Output of T and D

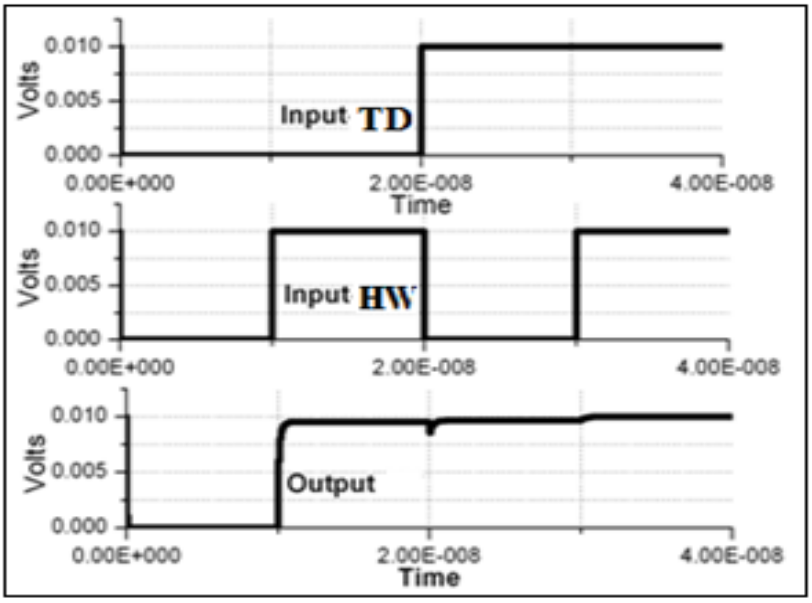

Fig. 5: Final output

C. Comparative Study

This novel model explored the best implementation of hybrid CMOS-SET logic synthesis in one of the most complex decision making design; certainly the presented model of can be included in next generation electronics. The proposed model was tested in all possible situations to explore all possible conditions but it showed no errors in performing the logic operations, rather two distinctive drawbacks of SET circuit was neutralized. Additionally, the power consumptions & propagation delays when evaluated to existing CMOS technology were quite less in hybrid CMOS-SET technology. Table-I below resembles all the estimated values of power consumption of the logic gates employed in these two circuits. The output voltage gain which is utmost critical from design perspective is approximated about 4.8 as obtained from the slope of the transitional region. If a uniform interval clock pulse is applied the model delivers uninterrupted potentiality and is proficient enough to conduct a predetermined sequence of states. The projected conception of hybrid CMOS-SET decision making system shows satisfaction in trade-off between CMOS and SET.

TABLE I
COMPARATIVE TABLE FOR HYBRID CMOS-SET

Circuit type	Power Supply	No. of CMOS	No. of SET	Power Consumption
TD / HW	0.01V	3	3	1.02E-09 W
TD + HW	0.01V	3	3	1.02E-09 W

IV. CONCLUSIONS

The design and simulation of hybrid CMOS-SET decision making sub system is modeled categorically and the results are acquired emphatically to render the underlying potential of perfect co-integration of CMOS-SET. One incredible feature is that the SET and CMOS are positioned in series and in this manner if the hybridization is achieved the result shows improved gain of the models and simultaneously the propagation delay decreases to some extent. The model was designed and implemented using sophisticated simulation software to explore maximum flexibility. The T-Spice simulation results of the proposed decision making sub system are not only agreeable but also the viability of using the proposed hybrid circuit in future low power ultra-dense VLSI/ULSI electronics is justified. Besides, co-integration using hybrid CMOS-SET showed explicit benefit in the room temperature operation, thus the limitations of SETs are controlled and further the model can exhibits its full functionalities. Beside other outstanding consequences of the proposed design, the operating temperature is set near to sub ambient regime of the switching speed, mobility and power dissipation which shows enhanced performance.

ACKNOWLEDGMENT

The first and second authors hereby acknowledge the technological and financial aid provided by the Camellia School of Engineering and Technology (CSET) of Camellia Group.

Abhishek Bar acknowledges the technological and financial aid provided by the ECE dept. of University Institute of Technology, The University of Burdwan.

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