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Low Leakage Power SRAM Design Using Lector Technique In Various CMOS Technology

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Abstract— The major portion of total power consumption in the integrated device is leakage power dissipation and is expected to grow exponentially in the next decade as per the International Technology Roadmap For Semiconductor(ITRS).In CMOS circuit, reduction of threshold voltage due to voltage scaling leads to increase in subthreshold leakage current and hence static power dissipation. Some leakage current reduction technique like Sleep Approach, Stack Approach, Lekage Feedback Approach, ZigZag Approach, Sleeper Keeper technique, Force Stack Technique and here we use proposed novel technique called LECTOR for designing CMOS gates which significantly cuts down the leakage current without increasing the dynamic power dissipation. The main advantage as compared to other techniques which involves the sleep transistor is that LECTOR technique does not require any additional control and monitoring circuitry, thereby limits the area increase and also the power dissipation in active state. Along with this, the other advantage with LECTOR technique is that it does not affect the dynamic power which is the major limitation with the other leakage reduction techniques. . In this paper we design 1 bit SRAM cell by using the LECTOR power reduction techniques. The proposed circuit technique were design in different CMOS/VLSI technology with in Microwind tool and measure power consumption design approach LECTOR achieves up to 35%-50% leakage reduction over the conventional circuit without affecting the dynamic power.

Keywords:Low Power, Leakage Reduction, Subthresholdleakage current, transistor stacking , Deep submicron, LECTOR(Leakage Control Transistor).

I. INTRODUCTION

Aggressive scaling of CMOS devices in the last four decades has enabled the semiconductor industry to meet its ever-increasing demand for higher performance and higher integration densities. In the growing market of mobile hand-held devices used all over the world today, the battery-powered electronic system forms the backbone. To maximize the battery life, the tremendous computational capacity of portable devices such as notebook computers, personal communication devices (mobile phones, pocket PCs, PDAs), hearing aids and implantable pacemakers has to be realized with very low power requirements. With miniaturization and the growing trend towards wireless communication, power dissipation has become a very critical design metric. The longer the battery lasts, the better is the device. The rapid progresses in semiconductor technology have leaded the feature sizes to be shrunk through the use of deep-submicron processes; thereby the extremely complex functionality is enabled to be integrated on a single chip.. High power consumption is one of the major challenges of integrated circuit design in nano-scale technologies . For high-performance applications, large power dissipations within a small die area are resulting in alarming temperatures, posing serious reliability concerns. For battery operated devices, on the other hand, increased power consumption is drastically limiting the battery lifetime. High power consumption leads to reduction in the battery life in the case of battery- powered applications and affects reliability, packaging, and cooling costs. The main sources for power dissipation are: 1) capacitive power dissipation due to the charging and discharging of the load capacitance; 2) short-circuit currents due to the existence of a conducting path between the voltage supply and ground for the brief period during which a logic gate makes a transition; and 3) leakage current. The leakage current consists of reverse-bias diode currents and sub-threshold currents. Scaling down of threshold voltage results in exponential increase of the sub-threshold leakage. Reduction in threshold voltage causes an exponential increase in sub-threshold leakage current, thereby static power. As one continues to scale down supply voltage and threshold voltage, the increased leakage power can dominate the dynamic switching power. In 22nm technology, the static power dissipated is 70-72% of the total power dissipated, where the supply voltage is 0.8V. In this paper LECTOR technique is implemented on memory circuit i.e., Static RAM for 1-bit

II . RELATED WORK

There are numerous methods proposed to control leakage power dissipation.

Power Gating: Power gating is one of the techniques proposed for leakage reduction, which turns off the device by cutting OFF the supply voltage. In this technique bulky NMOS and/or PMOS device called sleep transistor is used in a path between

supply voltage and ground. This is done to create virtual power and ground rails in the circuit. This technique creates a negative effect on the circuit switching speed when the circuit is operating in active mode. The identification of the idle regions of the circuit and the generation of the sleep signal need additional hardware capable of predicting the circuit states accurately. This additional hardware consumes power throughout the circuit operation even when the circuit is in an idle state to continuously monitor the circuit state and control the sleep transistors. A technique makes use of the dependence of the leakage current on the input vector to the gate. With additional control logic, the circuit is put into a low-leakage standby state when it is idle and restored to the original state when reactivated. Reactivation state forces the need to remember the original state information before going to low-leakage standby state. This requires special latches, thereby increasing the area of the circuit by about five times in the worst case. Also, the amount of time for which the unit remains in idle state should be long enough so that the dynamic power consumed in forcing the circuit to low- leakage state and the leakage power dissipated in the standby state together is less than the leakage power without the technique.

MTCMOS: The use of multiple threshold voltage CMOS (MTCMOS) technology for leakage control is another technique. The transistors of the gates are at low threshold voltage and the ground is connected to the gate through a high-threshold voltage NMOS gating transistor. The logical function of a gating transistor is similar to that of a sleep transistor. The existence of reverse conduction paths tend to reduce the noise margin or in the worst case may result in complete failure of the gate. Moreover, there is a performance penalty since high-threshold transistors appear in series with all the switching current paths. A variation of MTCMOS technique is the Dual VT technique, which uses transistors with two different threshold voltages. Low-threshold transistors are used for the gates on the critical path and high-threshold transistors are used for those not in the critical path. In both MTCMOS and Dual VT methods, additional mask layers for each value of threshold voltage. are required for fabricating the transistors selectively according to their assigned threshold voltage values. This makes the fabrication process complex. The techniques discussed above suffer from turning-on latency, that is, when the idle subsections of the circuit are reactivated, they cannot be used immediately because some time is needed before the sub-circuit returns to its normal operating condition. The latency for power gating is typically a few cycles, and for Dual VT technology, is much higher. Also, these techniques are not effective in controlling the leakage power when the circuit is in active state

Force Stacking: Forced stacking introduces an additional transistor for every input of the gate in both N- and P-networks. This ensures that two transistors are OFF instead of one for every OFF-input of the gate and hence makes a significant savings on the leakage current. However, the loading requirement for each input introduced by the forced stacking reduces the drive current of the gate significantly. This results in a detrimental impact on the speed of the circuit.

Sleepy Stack Technique : The sleepy stack technique has a structure merging the forced stack technique and the sleep transistor technique. When applying the sleepy stack technique, each existing transistor is replaced with two half sized transistors and add one extra sleep transistor. The leakage reduction of the sleepy stack structure occurs in two ways. First, leakage power is suppressed by high-Vth transistors, which are applied to the sleep transistors and the transistors parallel to the sleep transistors. Second, two stacked and turned off transistors induce the stack effect, which also suppresses leakage power consumption. By combining these two effects, the sleepy stack structure achieves ultra-low leakage power consumption during sleep mode while retaining exact logic state. The price for this, however, is drastically increased area. And the major disadvantage of having controlling circuitry for sleep transistors is also carried here. As the sleep transistors are bulky, hence increases the dynamic power.

Sleepy Keeper : Sleepy Keeper is a better leakage reduction technique compared to sleepy stack. It gives an excellent alternate for sleepy stack in terms of reducing the area overhead since it doesn't need three transistors to be replaced to one transistor. Sleep transistors are connected to the circuit along with NMOS connected to Vdd and PMOS connected to Gnd. The sleep transistor is turned on when the circuit is active and turned off when the circuit is in idle state with the help of sleep signal. This creates virtual power and ground rails in the circuit. Hence, there is a significant detrimental effect on the switching speed when the circuit is active. The identification of the idle regions of the circuit and the generation of the sleep signal needs an additional hardware capable of predicting the circuit states accurately, thereby increasing the area requirement of the circuit. This technique creates a negative effect when the circuit is operating in active mode in terms of the circuit performance. This additional hardware consumes power throughout the circuit operation even when the circuit is in an idle state to continuously monitor the circuit state and control the sleep transistors.In this work, a new technique for leakage control in CMOS circuits is developed. The proposed technique avoids the problems associated with all the above discussed techniques.

III. PROPOSED TECHNIQUE MODIFIED LECTOR TECHNIQUE

The effective stacking of transistors in the path from supply voltage to ground is the basic idea behind the LECTOR technique for the leakage power reduction. LECTOR approach for reduction of leakage power is based on the effective stacking of transistors in the path from supply voltage to ground. The basic idea behind LECTOR is based on the concept that "a state with more than one transistor OFF in a path from supply voltage to ground is far less leaky than a state with only one transistor OFF in any supply to ground path."The topology of a LECTOR CMOS gate is shown in Figure 1. Two LCTs are introduced between nodes N1 and N2. The gate terminal of each LCT is controlled by the source of the other, hence termed as self-controlled stacked transistors. As LCTs are self-controlled, no external circuit is needed; thereby the limitation with the sleep transistor. technique has been overcome. The introduction of LCTs increases the resistance of the path from Vdd to Gnd, thus reducing the leakage current.In this method, two leakage control transistors (LCTs) were introduced in each CMOS gate, a PMOS (LCT1)

added to the pull-up network and a NMOS (LCT2) added to the pull-down network and the gate terminal of one LCT is controlled by the source terminal of the other, such that one of the LCTs is always near its cutoff region of operation for any input(s) given to the CMOS gate, thus providing additional resistance in the path from supply to ground, decreasing the sub-threshold leakage current, thereby the static power. This section illustrates Leakage Control Transistor (LECTOR) technique with the case of memory circuits and other CMOS logic circuits.

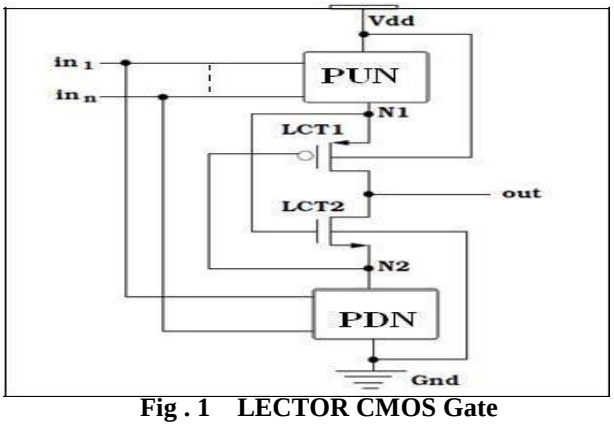


Fig . 1 LECTOR CMOS Gate

A CMOS NAND gate with the addition of two leakage control transistors which is known as LECTOR NAND is shown in Fig. 1. Two leakage control transistors LCT1 (PMOS) and LCT2 (NMOS) are introduced between the nodes N1and N2 of the pull-up and pull-down logic of the NAND gate. The drain nodes of the transistors LCT1 and LCT2 are connected together to form the output node of the NAND gate. The source nodes of the transistors are connected to nodes N1 and N2 of pull-up and pull-down logic, respectively. The switching of transistors LCT1 and LCT2 are controlled by the voltage potentials at nodes N2and N1 respectively. This wiring configuration ensures that one of the LCTs is always *near its cutoff region*.

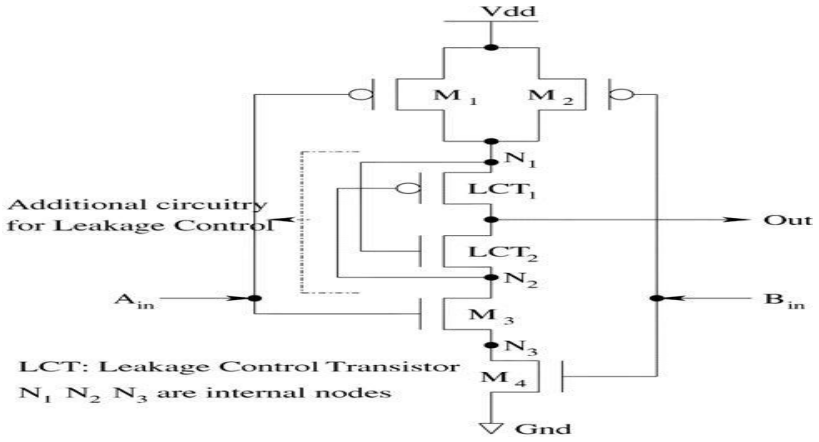


Fig**. 2LECTOR based NAND Gate**

IV. STATIC RANDOM ACCESS MEMORY

The 1-bit Static RAM design using 6 transistors is shown in the Fig. 3. Static RAM is a power-hungry circuit, since it should be in active mode continuously.

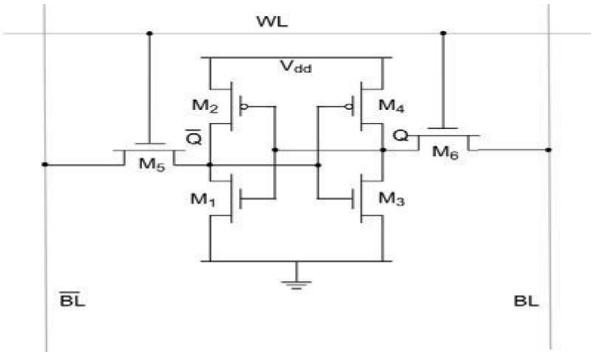


Fig.3 One Bit SRAM Cell

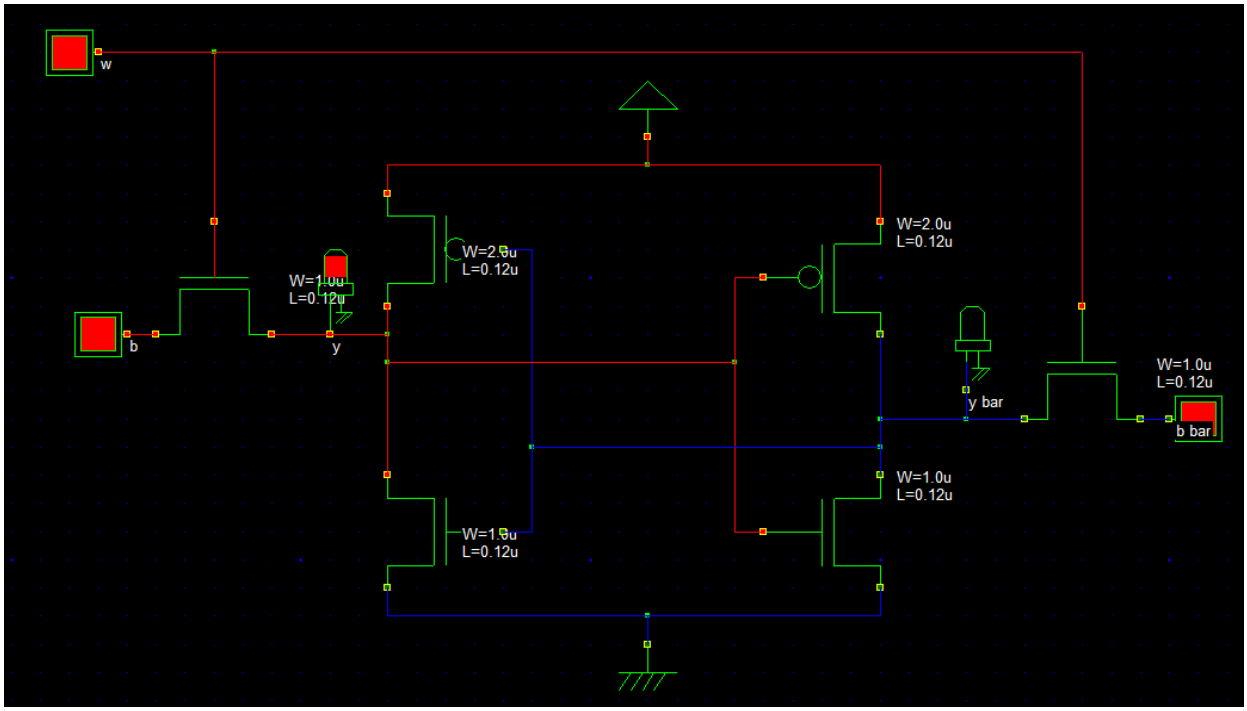
Random access means that locations in the memory can be written to or read from in any order, regardless of the memory location that was last accessed.Each bit in an SRAM is stored on four transistors that form two cross-coupled inverters. This storage cell has two stable states which are used to denote 0 and 1. Two additional access transistors serve to control the access to a storage cell

during read and write operations. Access to the cell is enabled by the word line (WL in figure 3) which controls IV the two access transistors, in turn, control whether the cell should be connected to the bit lines: BL and BL". They are used to transfer data for both read and write operations.

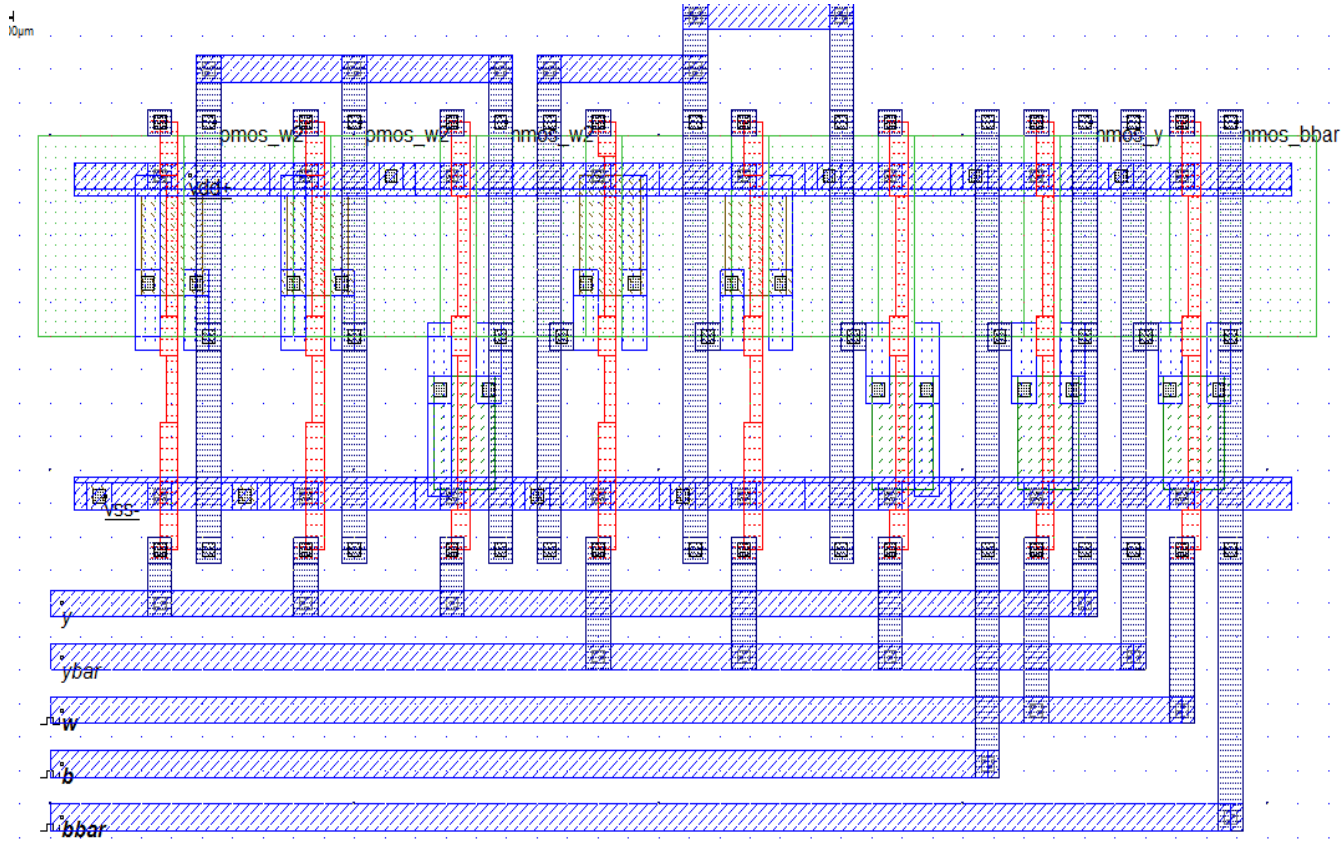
While it's not strictly necessary to have two bit lines, both the signal and its inverse are typically provided since it improves noise margins.Hence in nanoscaletechnology, the leakage power in Static RAM will be comparatively very high than other CMOS circuits. Using other peripheral circuitry like sense amplifiers, precharge circuit and row decoders, the LECTOR technique is applied to higher capacity SRAM

V. DESIGN IMPLEMENTATION

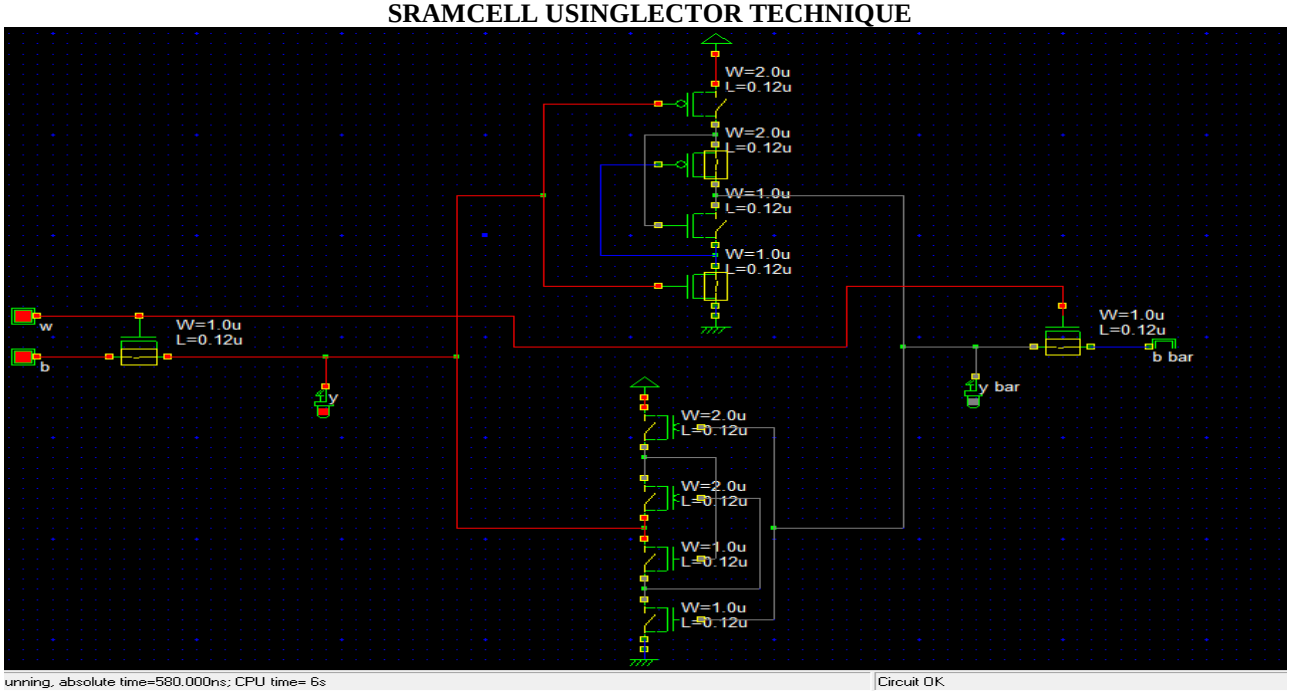
CONVENTIONAL 6T SRAM CELL



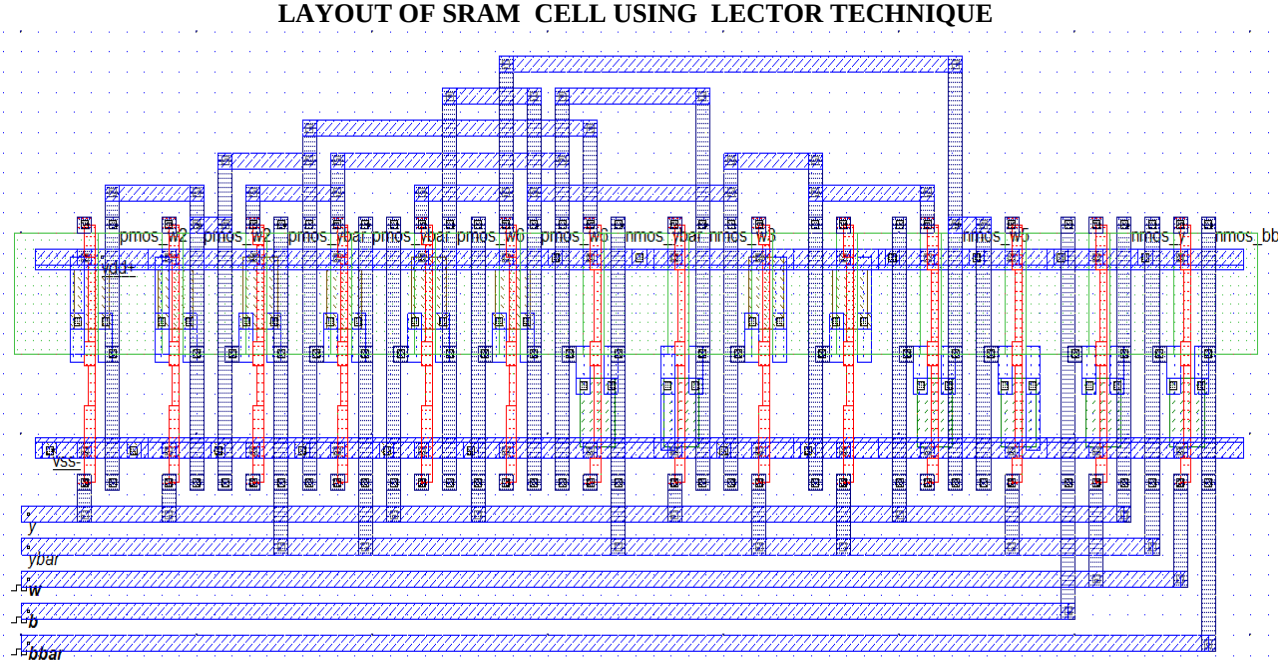
LAYOUT FOR CONVENTIONAL 6T SRAM



SRAMCELL USINGLECTOR TECHNIQUE



LAYOUT OF SRAM CELL USING LECTOR TECHNIQUE



VI. EXPERIMENTAL RESULTS

The MicroWind tool is used to measure the leakage power.Table I shows the results obtained through the technique for the Static RAM for 1 bit and static RAM for 1 bit Based on LECTOR technique.Also these results are compared with that of respective conventional case.

VII. CONCLUSION

The scaling down of device dimensions, supply voltage, and threshold voltage for achieving high performance and low dynamic power dissipation has largely contributed to the increase in leakage power dissipation. With deep-submicron and nanometer technologies, the leakage current becomes more critical in portable systems where battery life is of primary concern.

In nanometer scale CMOS technology, sub-threshold leakage power is compatible to dynamic power consumption, and thus handling leakage power is a great challenge. This paper presents "LECTOR" to tackle the leakage problem. LECTOR uses two additional self-controlled transistors. Like other leakage reduction techniques, such as sleepy stack, sleepy keeper, etc, LECTOR also achieves leakage power reduction but with the advantage of not affecting the dynamic power as this technique does not require any additional control and monitoring circuitry like in and also maintains exact logic state.

LECTOR technique can retain logic state, so it can be used for both generic logic circuits as well as memories, i.e., SRAM.

TABLE . I
RESULTS FOR STATIC RAM USING VARIOUS TECHNOLOGY

SRAM	TECHNOLOGY	LEAKAGE POWER(W)		%AGE Decreases in power dissipation
		Conventional	LECTOR	
1 bit	180nm	3.92 E-03	1.838E-03	53.11
	120 nm	9.72E-04	4.836E-04	50.04
	100nm	5.09E-04	3.25E-04	36.1
	70 nm	5.45E-04	3.96E-04	27.3
	50 nm	9.45.0E-05	6.85E-05	27.6

When applied to Static RAM, the LECTOR technique achieves up to 30-50% leakage reduction over the conventional circuit without affecting the dynamic power.

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