



## Design of High Speed Data Transceiver Serial Front Panel Data Port Protocol

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**ABSTRACT:** This paper presents a high speed data transceiver Serial Front Panel Data Port (SFPDP) protocol which finds applications in most modern day communication systems. The design can be programmed to work at different speeds as required by different systems and thus can be used in variety of systems involving high-speed data transfers. The efficient use of customized IP cores and resources of FPGA delivers high level of performance and area efficient.

**Keywords:**

### I. INTRODUCTION

Serial front panel data port (SFPDP) is a serial communication protocol that is designed to have a low latency and a high transfer rate. It's application is in high-speed real-time applications. It is currently defined to be used with 1.0625 Giga band, 2,125 Giga band 2.5Giga band data rates. The use of fiber optic cables allows SFPDP to operate over long distances.

This design has been mainly done for data transceiver in radar systems but can be programmed and used for variety of applications involving high-speed data transfer. The design follows a systematic approach with design of SFPDP protocol and implementation on FPGA and explains all these stages of design in detail.

FPGA stands for field programmable gate arrays that can be configured by the customer or designer after manufacturing. FPGAs are programmed using a logic circuit diagram or a source code in a hardware description language (HDL) to specify how the chip will work. FPGAs contain programmable logic components called "logic blocks" and a hierarchy of reconfigurable interconnects that allow the blocks to be "wired together". The programmable logic blocks are called configurable logic blocks and reconfigurable interconnects are called switch boxes. Logic blocks (CLBs) can be configured to perform complex combinational functions, or merely simple logic gates like AND and XOR. In most FPGAs, the logic blocks also include memory elements, which may be simple flip-flops or more complete blocks of memory.

### II. ARCHITECTURE

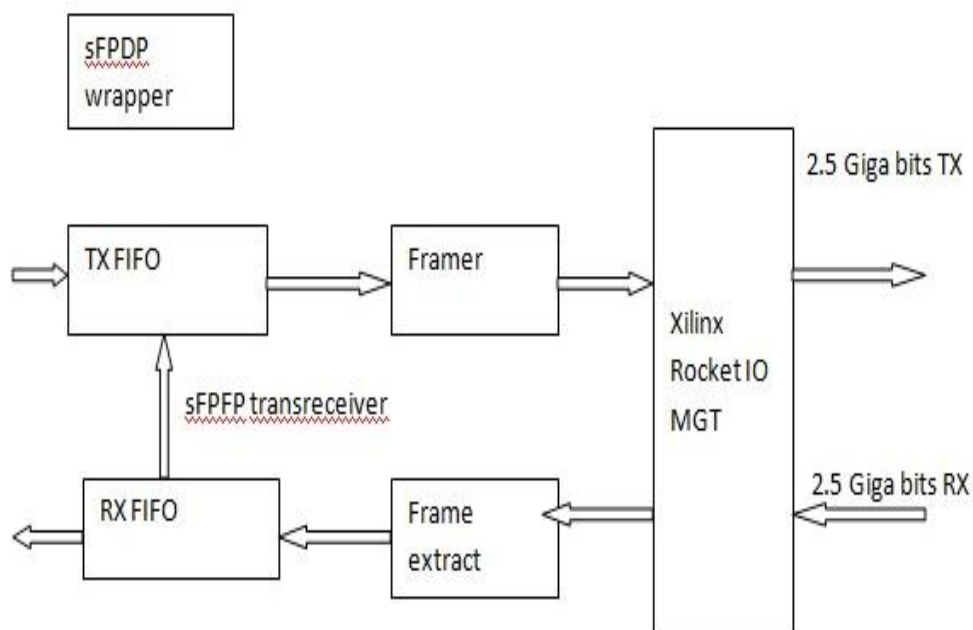


FIG 1. SFPDP wrapper top level diagram

### III. THE PROPOSED TRANSCEIVER- SFPDP

The heart of the SFPFP core is the SFPDP transceiver module. This module takes care of encoding and decoding the SFPDP packets. The encoded data is available on the following:

1. signals.
2. SFPDP\_txcharisk
3. SFPDP\_txdata

This port can connect directly to the transmit input of a Xilinx MGT or GTP. In case of a vertex 4 device the SFPDP\_tx data port will be 32 bits wide and the SFPDP\_txcharisk port is 4 bits wide. In case the core will be used in a vertex 5 the sfpdp\_tx data port will be 16 bits wide and the SFPDP\_txcharisk port is 2 bits wide. Likewise the decoded data has to be made available on the following signals:

1. SFPDP\_RXCHARISK
2. SFPDP\_RX DATA

This port can connect directly to the receiver output of a Xilinx MGT or GTP. In case of a virtex 4 device the SFPDP\_rx data port will be 32 bits wide and the SFPDP\_rxcharisk port is 4 bits wide. In case the core will be used in a virtex 5 the sfpdp\_rxdata\_port will be 16 bits wide and the SFPDP\_rxcharisk port is 2 bits wide. High-speed data transfer finds application in most modern day communication systems. This design has been mainly done for data transfer in radar systems but can be programmed and used for variety of applications involving high speed data transfer. The design follows a systematic approach with design of SFPDP protocol and implementation on FPGA and explains all these stages of design in detail. The design can be programmed to work at different speeds as required by different systems and thus can be used in variety of systems involving high-speed data transfers. The efficient use of customized IP cores and resources of FPGA delivers high level of performance and area efficiency.

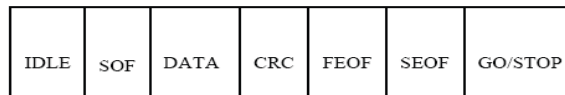


Fig2: Normal Data Fiber Frame

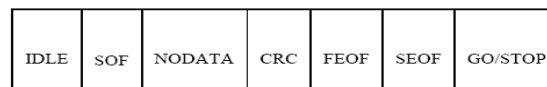


Fig3: Sync without Data Fiber Frame

### IV. Transmitted Data

SFPDP is developed & simulated in ISE simulator. The transmitted data is received at the receiver end with the speed of 10 Giga bps which shows the effectiveness of the proposed designed `timescale 1ns / 1ps`timescale 1ns / 1ps model. The transmitted data is of the form as shown in figure.

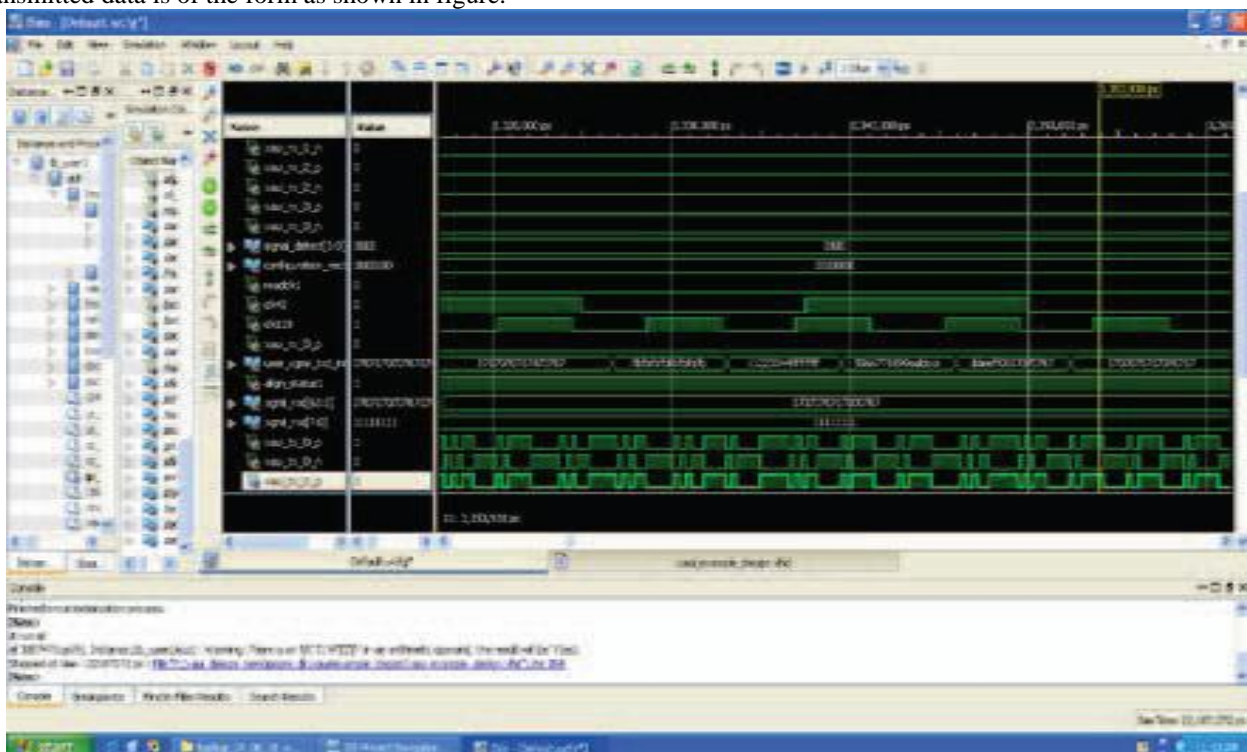


Fig4

### V. Data Stored In The Buffer

The below figure shows the data stored in the buffer. The 32 bit SFPDP frame data transmitted through XAUI core will be stored in the buffer of size 32 bit along with the idle and start bit of XAUI.

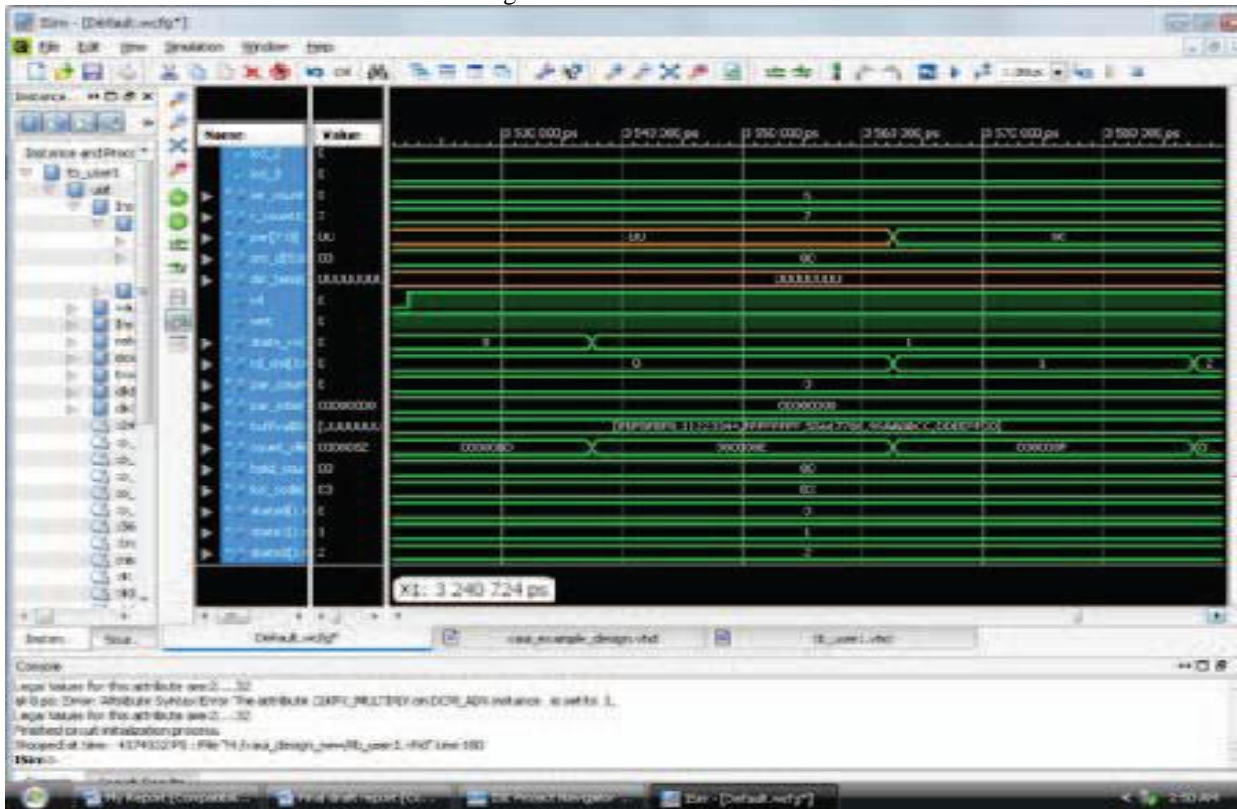


Fig5

### VI. Received Data

The main objective of this work is to transmit the data through SFPDP protocol. The transmitted data is stored in buffer & then received at the receiver. The output at the receiver is of the form as shown in figure 6 which meets the requirement of the designed model. The above results are excellent & justify the designed SFPDP protocol for high speed data transfer. The received data is as same as the transmitted data with the same values.

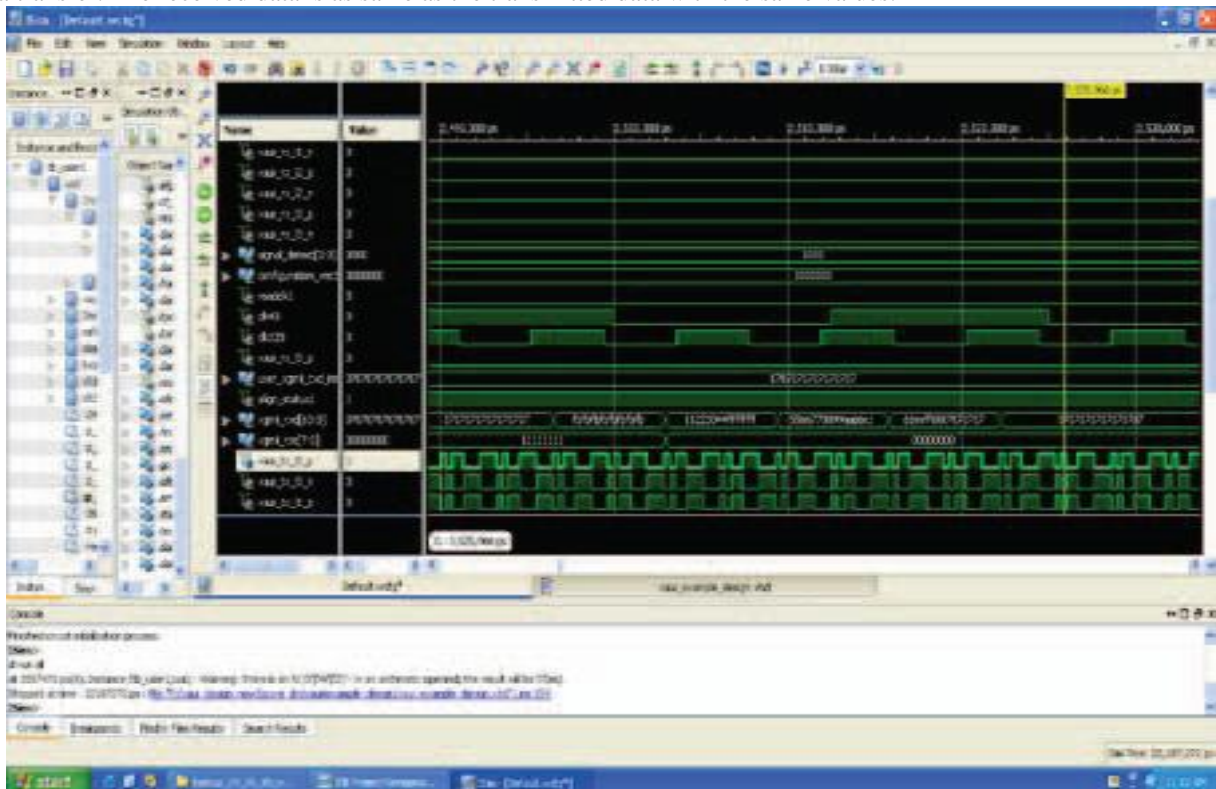


Fig6

## VII. CONCLUSION

This work explains the implementation of reliable technique of high-speed data transfer through optical link by using SFPDP protocol implemented in FPGAs. In this work, XAUI (Extended Attachment Unit Interface), the serial interface core is used. XAUI supports data rate of up to 10 Giga bps, thus the SFPDP frame data is sent through the interface to achieve maximum data transfer rate. The data/SFPDP frame in the system is looped back using fiber optic cable. This module enables the long distance communication with high data rate through optical link. The design can be programmed to work at different speeds as required by different systems and thus can be used in variety of systems involving high speed data transfers.

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