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Stability Analysis of 6t and Schmitt Trigger Based SRAM Cell

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***Abstract** - Due to wide-spread use of electronic devices, embedded memories play a significant role in modern era. Due to fast and random access, SRAM is mainly used as a cache memory. But in low power VLSI, Stability degrades due to technology scaling and fluctuations in process parameters that is oxide thickness, diffusion depth and density of impurity concentration etc Thus to measure stability, static noise margin is the main performance parameter in SRAM cell. In this paper, we present two SRAM topologies, conventional 6t and Schmitt Trigger based SRAM bit cell. These two topologies are characterized and compared on the basis of their Read and Write SNM with dynamic power supply. The tool used for simulation purpose is IC station by Mentor Graphics using TSMC 180nm CMOS technology.*

***Keywords:** Read SNM, Write SNM, Dynamic Supply Voltages, 6T SRAM CELL, LOW POWER SCHMITT TRIGGER SRAM CELL.*

I. INTRODUCTION

In modern era, the need of electronics, portable and multimedia devices is rapidly increasing day by day. So in consumer electronic market, there is a big competition among electronic industries for low power consumption, stability and high speed of devices. With the continuous shrinking of channel length and device scaling, the device loses its speed and stability. Memories are embedded in most of the digital devices. According to International Technology Roadmap for Semiconductors (ITRS), Memory is expected to occupy about 90% of the chip area in 2013 [1]. So any failure in memory will affect the whole performance of the system. Therefore stability is the major concern in order to improve the system performance, stability and efficiency. Static Noise Margin (SNM) is useful performance parameter to measure the stability of a system. Today's everyone wants low power, stable and fast accessible device. Though, the high speed devices use SRAM as a cache memory. Mostly SRAM is used in low power and high speed applications because of its fast and random access. The main and biggest role of low power SRAM in most of the digital devices is due to their battery life and good stability of portable devices. For proper, stable and reliable operation in a SRAM cell, appropriate sizing is done according to the cell ratio [2] and pull ratio up ratio [3] of the transistor. The internal node of SRAM which stores '0' will be pulled up through the access transistor and the drive transistor. This increase in voltage severely degrades the SNM mainly during read operation. In this paper, Schmitt Trigger based SRAM Topology is compared with the conventional 6T SRAM Cell which has better Read and Write static noise margin.

II. THE CONVENTIONAL 6T SRAM CELL

The Schematic diagram of 6T SRAM Cell is shown in Fig1.
The conventional 6T SRAM cell comprises of two cross coupled inverter. The output of one inverter is connected to input of other and vice-versa. The complementary output of these two inverters is connected to the two access transistors (M5 and M6) which connect the bit and bit-bar lines to the cell. These two access transistors are accessed through word line. The word line and bit lines are selected by the row and column address respectively. The combination of these addresses selects a particular cell in a memory array.
A SRAM Cell mainly performs three operations: Hold operation, Read and Write operation.
During Hold Operation, the word line is not asserted and the cell is disconnected to the bit lines. In this state, the two cross coupled inverters retain the stored value till the power supply is going on.
During Read Operation, the bit lines are precharged to an intermediate value (between VDD/2 and VDD) before the starting of the read operation. Suppose the cell is storing logic '1'. In this case, Q is at VDD and QB is at '0'.When the word line is asserted then pull up (M3) and access transistor (M5) will turned on. And current will flow from VDD through M3 to M5. This current will charge the capacitance of bit line. At the same time, the bit bar line is discharged to ground. In this case, the voltage across bit line rises and voltage across bit-bar line falls. Thus, a voltage difference is developed between bit and bit bar line. This voltage difference is very small so a sense amplifier is connected to the bit and bit bar line to detect the presence of '1' in the cell during readout. One should keep in mind that during read '1', the node voltage where logic'0' is stored must not be more than the switching threshold of driver transistor of other inverter otherwise the stored content will destroy. To keep this condition, the cell ratio must be appropriately selected [2].

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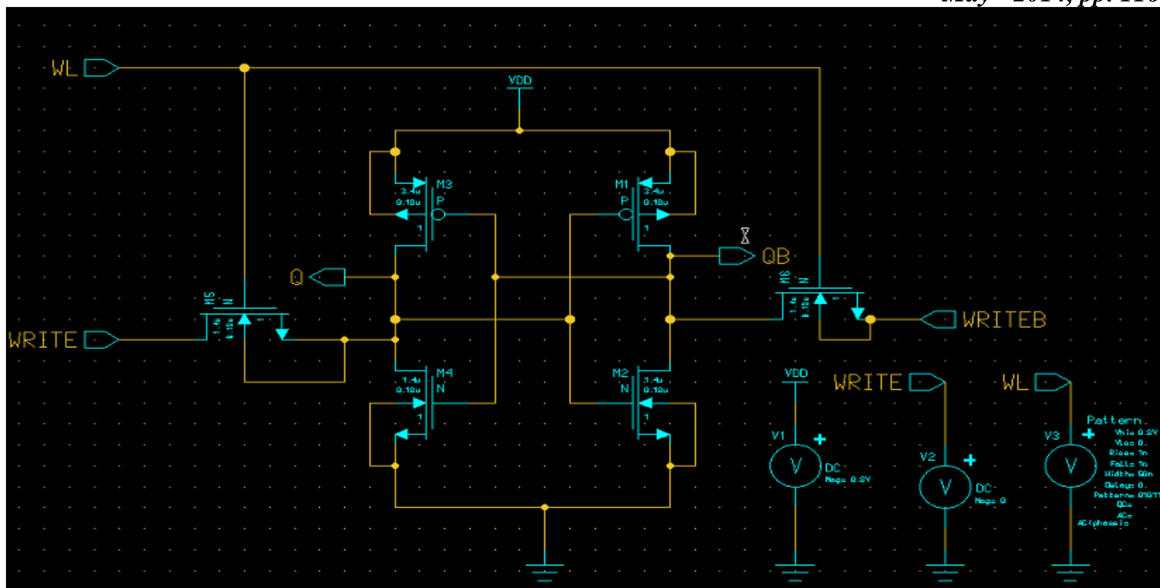

Fig 1: 6T SRAM CELL

The cell ratio (CR) during read operation is defined as:

$$CR= (W/L)_{\text{Pull down}} / (W/L)_{\text{Access Transistor}}$$

During write operation, the precharged logic is kept at low. Suppose we want to store logic'1'. Bit line is charged to VDD and bit bar line is discharged to ground. When the word line is activated, the data on bit and bit bar lines are written into the output nodes of the cell. During updating of content, one should remember that the voltage where logic'1' is stored must be less than the threshold voltage of the driver transistor of other inverter. To keep this condition, the pull up ratio must be appropriately selected [2]. The pull up ratio (PR) is defined as:

$$PR = (W/L)_{\text{Pull up Transistor}} / (W/L)_{\text{Access Transistor}}$$

III. SCHMITT TRIGGER BASED SRAM CELL

In order to find a solution for the conflicting read versus write operation design requirement in the 6T SRAM Cell, Schmitt Trigger principle is applied for the cross coupled inverter pair. A Schmitt trigger increases or decreases the switching threshold of an inverter depending on the direction of the input transition [7]. In this, a feedback mechanism in pull down path is used as shown in Fig.2.

During a read Operation (Q ='0' and QB ='1'), the voltage on Q rises due to voltage divider action between access transistor and pull down transistor. If this voltage becomes higher than the switching threshold of the other inverter, the content of the cell can destroy. This result read failure event [8].

In order to avoid read failure event, this topology is used. In this topology, transistor M4 and N3 raises the switching threshold of source voltage of transistor M3. Thus the feedback transistor tries to preserve the logic'1' at the output of cell [9].

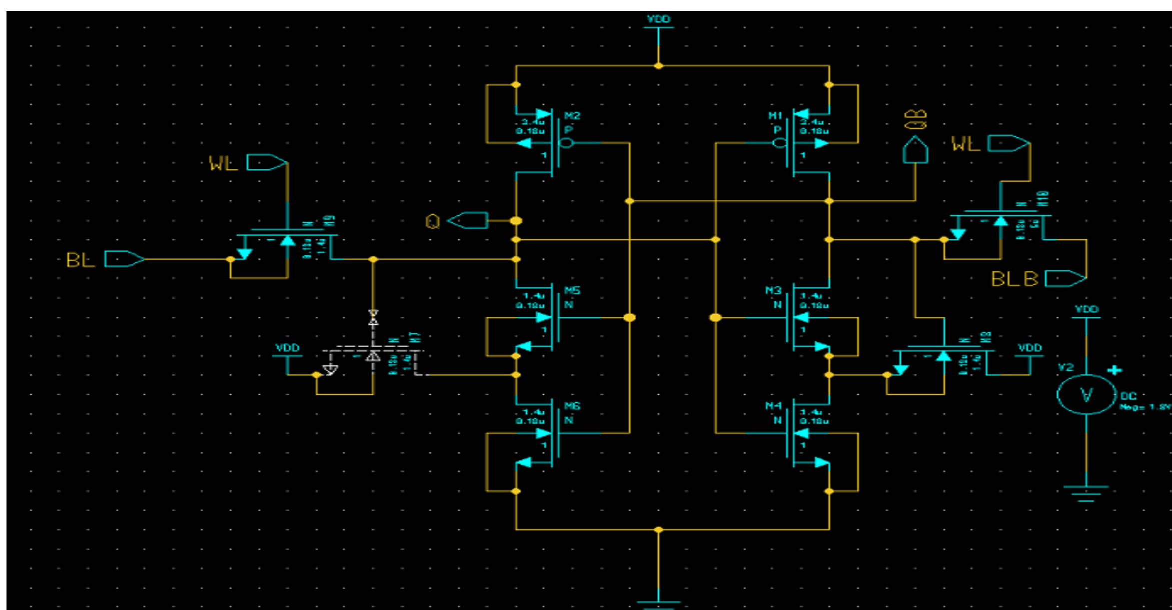

Fig 2: ST BASED SRAM CELL

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IV. EXPERIMENTAL ENVIRONMENT AND SIMULATION RESULTS

All the simulation has been done using IC Design Architect by Mentor Graphics using 180nm CMOS technology with supply voltage ranging. Graph shows stability analysis of the circuits stated at 180nm technology.

V. SNM DETERMINATION

A. Read Static Noise Margin

To find RSNM, Cell Ratio (CR) must be appropriately selected [2] as mentioned earlier. For Read Static Noise Margin, the word line and bit line is kept at high. Then the feedback between these two inverters is broken. By DC analysis, the voltage transfer characteristic (VTC) of the half cell is plotted between input and output voltage. This results butterfly curve by superimposing the VTC of one inverter to the inverse VTC of the other inverter of SRAM Cell [5] [6]. The SNM is the side of largest square fitted in the butterfly curve as shown in fig.

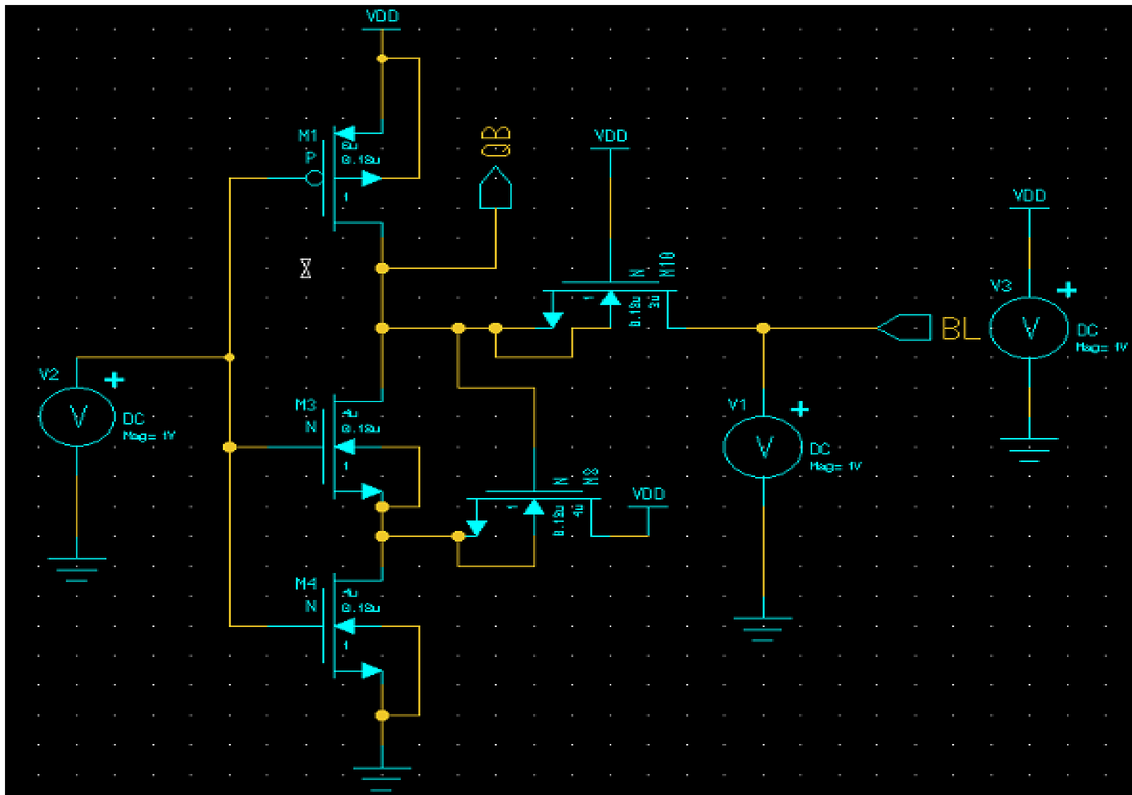

Fig 3: ST READ SNM SCHEMATIC

The Read SNM Curves of ST based SRAM cell for CR= 1.33 on dynamic supply voltages are

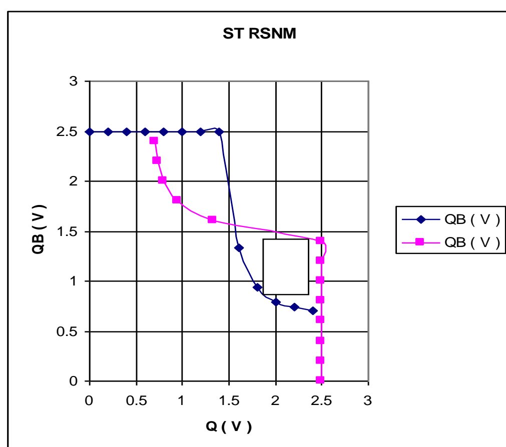

Fig 3(a): Read Static Noise Margin (RSNM) of ST SRAM cell for 2.5V

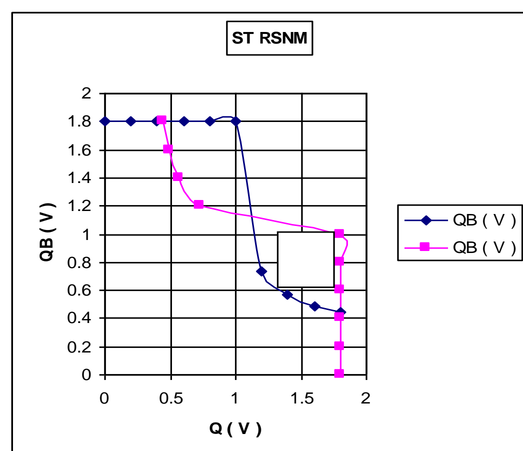

Fig 3(b): Read Static Noise Margin (RSNM) of ST SRAM cell for 1.8V

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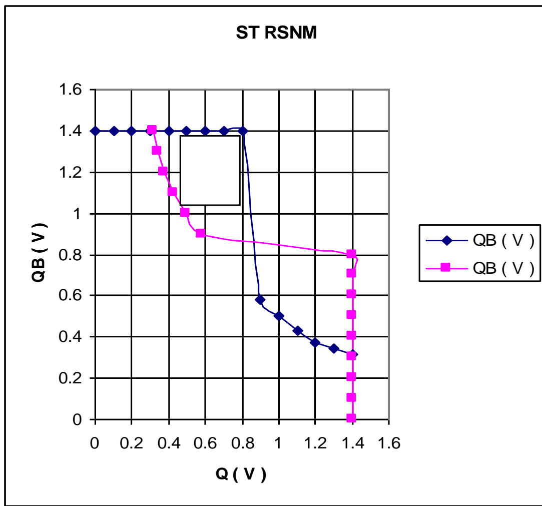

Fig 3(c): Read Static Noise Margin (RSNM) of ST SRAM cell for 1.4V

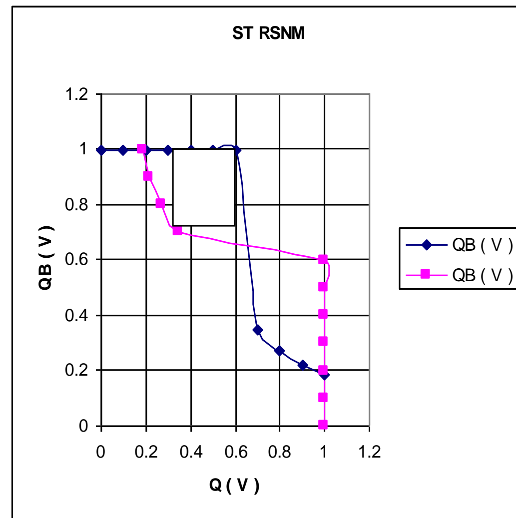

Fig 3(d): Read Static Noise Margin (RSNM) of ST SRAM cell for 1V

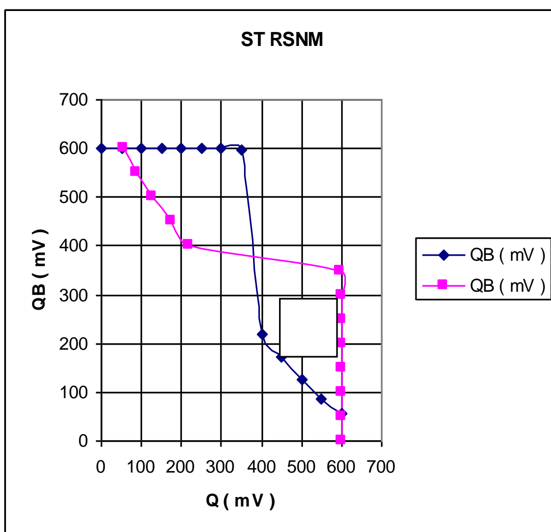

Fig 3(e): Read Static Noise Margin (RSNM) of ST SRAM cell for 0.6V

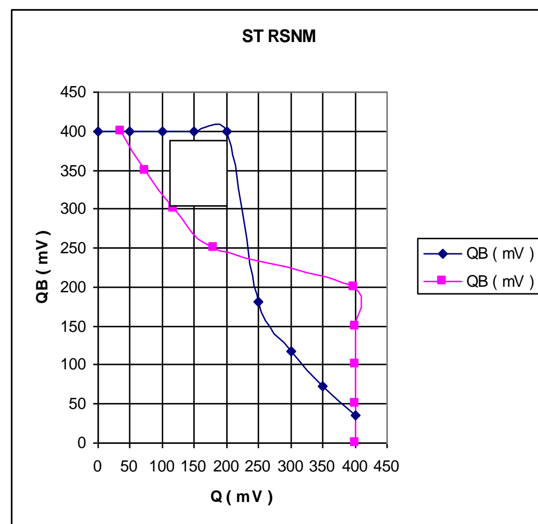

Fig 3(f): Read Static Noise Margin (RSNM) of ST SRAM cell for 0.4V

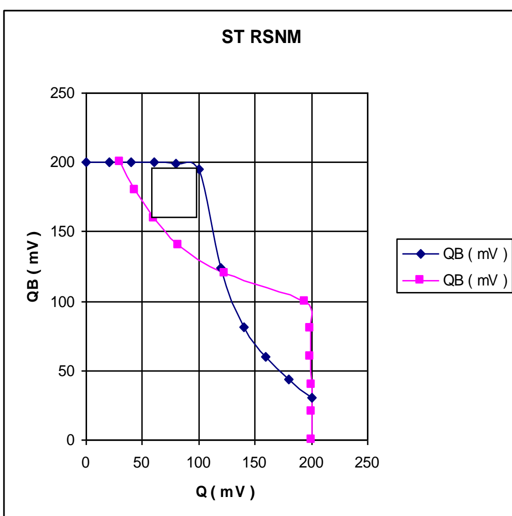

Fig 3(g): Read Static Noise Margin (RSNM) of ST SRAM cell for 0.2V

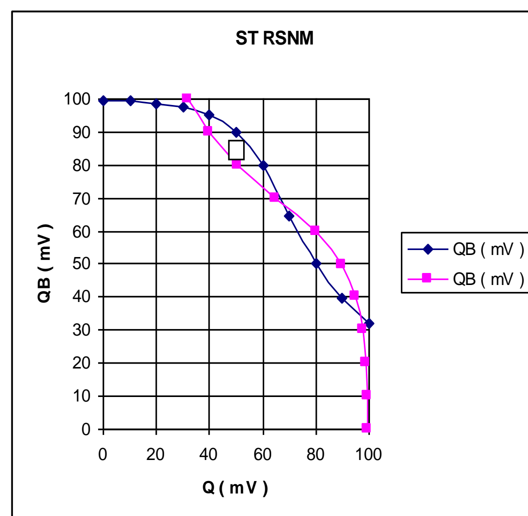

Fig 3(h): Read Static Noise Margin (RSNM) of ST SRAM cell for 0.1V

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TABLE 1: Supply Voltages VS RSNMs

VDD (V)	RSNM (mV) (6T SRAM Cell)	RSNM (mV) (ST SRAM Cell)
2.5	400	500
1.8	210	400
1.4	190	300
1	150	220
0.6	80	160
0.4	55	75
0.2	10	40
0.1	0 (READ FAILURE)	6

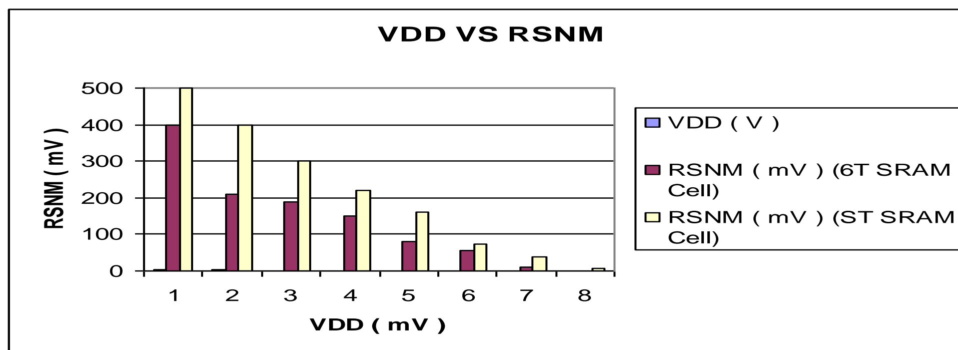

Fig 4: Comparison between Read SNMs of Conventional 6T SRAM cell and ST SRAM cell

Table 1 compares Read SNMs of Conventional 6T SRAM cell and Schmitt Trigger based SRAM cell. Fig 4 shows graphical view of comparison. When butterfly curve is not valid then the read operation fails. Simulation results show that the 6T SRAM cell fails in read operation below 100mV as shown in Table 1.

B. Write Static Noise Margin

To find WSNM, the Pull up Ratio (PR) must be appropriately selected [3]. For WSNM, the word line is kept at logic'1'. The data is loaded on the bit and bit-bar line. Then the feedback from cross-coupled inverter is broken. By DC analysis, a butterfly curve is plotted between input and output of both half cell inverters [5] [6]. The side of largest square fitted in the two VTC of half cell inverters is called Write Static Noise Margin.

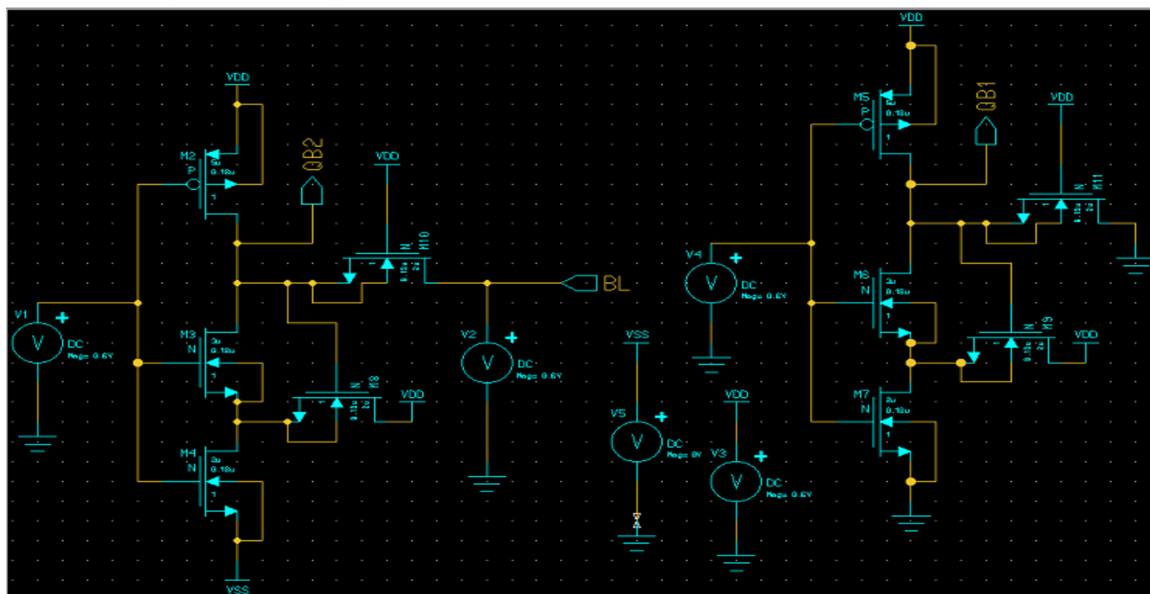

Fig4. ST WSNM SCHEMATIC

The Write SNM Curves of ST based SRAM cell for PR= 2.5 on dynamic supply voltages are

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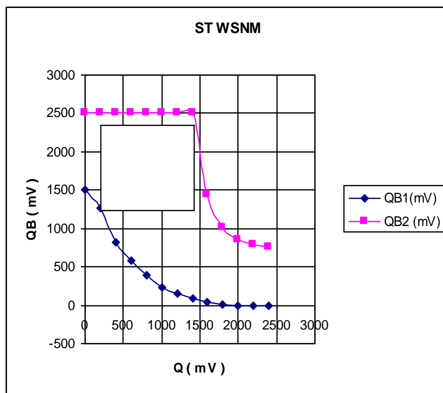

Fig 4(a): Write Static Noise Margin (WSNM) of ST SRAM cell for 2.5V

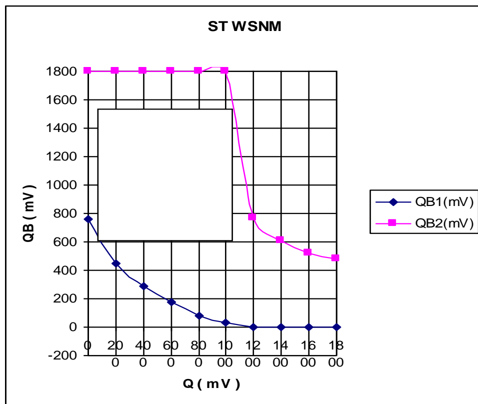

Fig 4(b): Write Static Noise Margin (WSNM) of ST SRAM cell for 1.8V

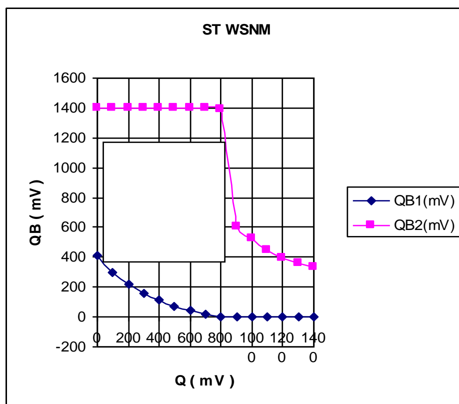

Fig 4(c): Write Static Noise Margin (WSNM) of ST SRAM cell for 1.4V

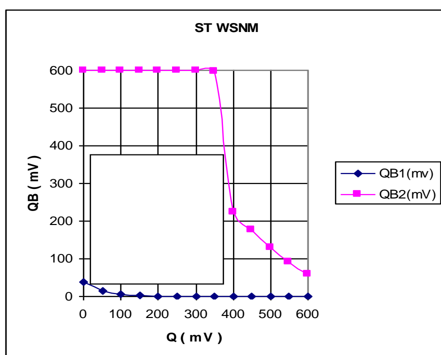

Fig 4(e): Write Static Noise Margin (WSNM) of ST SRAM cell for 0.6V

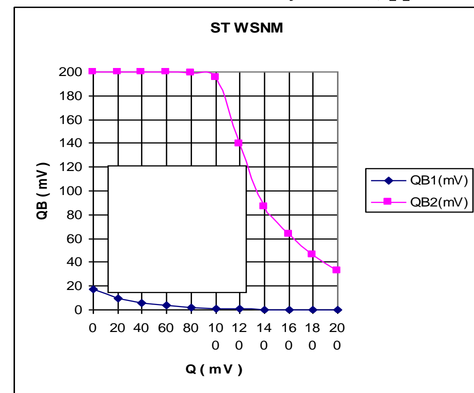

Fig 4(g): Write Static Noise Margin (WSNM) of ST SRAM cell for 0.2V

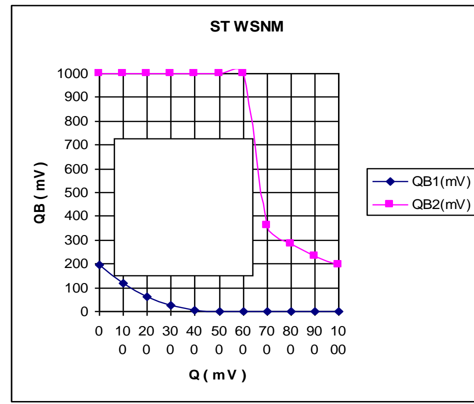

Fig 4(d): Write Static Noise Margin (WSNM) of ST SRAM cell for 1V

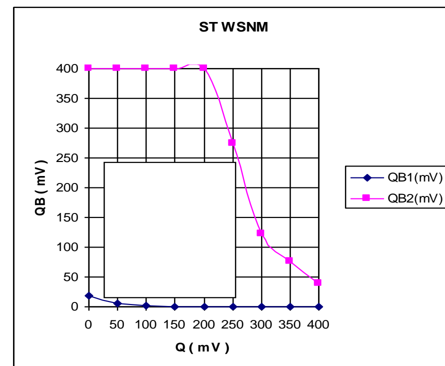

Fig 4(f): Write Static Noise Margin (WSNM) of ST SRAM cell for 0.4V

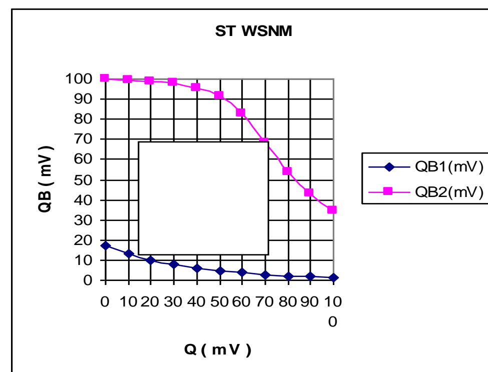

Fig 4(h): Write Static Noise Margin (WSNM) of ST SRAM cell for 0.1V

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TABLE 2: Supply Voltages Vs WSNMs

VDD (V)	WSNM (mV) (6T SRAM Cell)	WSNM (mV) (ST SRAM Cell
2.5	880	1100
1.8	710	900
1.4	650	800
1	500	570
0.6	280	360
0.4	200	230
0.2	95	110
0.1	45	56

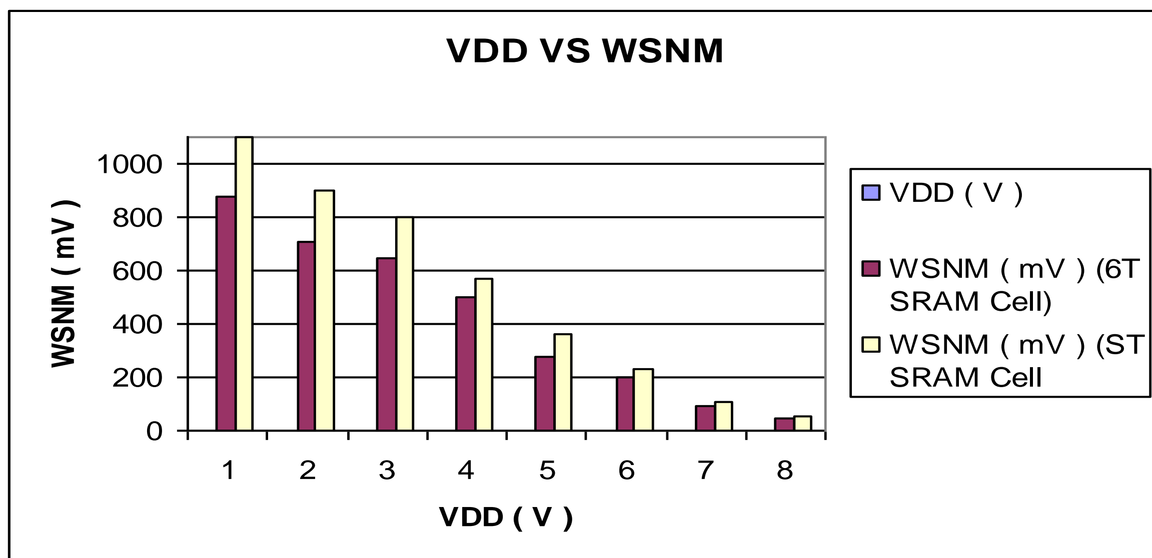

Fig 5: Comparison between Write SNMs of Conventional 6T SRAM cell and ST SRAM cell

Table 2 compares Write SNMs of Conventional 6T SRAM cell and Schmitt Trigger based SRAM cell. Fig 5 shows graphical view of comparison. Simulation results show that the ST SRAM cell is more robust and stable than 6T Conventional SRAM cell as shown in Table 2.

VI. CONCLUSION

Nano scaled technologies for ultra low power and high speed application degrades the stability. Stability is measured by Static Noise Margin and defines the robustness of the cell. From the above analysis, it can be concluded that as supply voltage decreases gradually then at a point, the RSNM of conventional 6T cell becomes zero at VDD=0.1V due to process variations but the ST based SRAM Cell is still stable at this voltage. Also at same CR and PR, the RSNM and WSNM is more than the conventional 6T SRAM Cell at dynamic supply voltages. It means that the ST SRAM cell can work efficiently in sub threshold region.

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