



Empirical Review of Low Power Column by Pass Multiplier

Er. Neha Gupta
M.Tech (ECE), SRMIET.

Dr. B.K Sharma
Director, SRMIET.

ABSTRACT: *Designing high-speed multipliers with low power and regular in layout have substantial research interest. The analysis is done on the basis of certain performance parameters i.e. Area, Speed and Power consumption and dissipation. Multipliers are considered to be an important component in DSP applications like filters. Therefore, the low power multiplier is a necessity for the design and implementation.*

To scale back the facility consumption of multiplier factor booth coding methodology is being employed to rearrange the input bits. The operation of the booth decoder is to rearrange the given booth equivalent. Booth decoder can increase the range of zeros in variety. Hence the switching activity are going to be reduced that further reduces the power consumption of the design. The input bit constant determines the switching activity part that's once the input constant is zero corresponding rows or column of the multiplier ought to be deactivated. When multiplicand contains more number of zeros the higher power reduction can takes place. So in modified booth multiplier high power reductions will be achieved. In this paper a modified structure with reduced switching activity is presented through optimization of design. Many low power designs have been found. Power reduction can be improved using structure modification.

Keywords: *Column bypassing multiplier, Modified booth algorithm, Spartan-3AN.*

I. INTRODUCTION

Multiplication is a basic arithmetic operation which is present in many part of the digital computer especially in signal processing systems such as graphics and computation system. It requires more hardware resources and processing time than addition and subtraction requires. There is a continuous development in VLSI technologies and, the needs to develop process independent chip design tools are growing [1], [2], [3].

Low power consumption, and short design cycle, have Become increasingly popular over the past few years. Many Multimedia and DSP applications are highly multiplication intensive so that the performance and power consumption of these systems are dominated by multipliers. The computation of the multipliers manipulates two input data to generate many partial products for subsequent addition operations, which in the CMOS circuit design requires many switching activities. Thus, switching activity within the functional unit requires for majority of power consumption and also increases delay. Therefore, minimizing the switching activities can effectively reduce power dissipation and increase the speed of operation without impacting the circuit's operational performance.

There are different multiplier structures which can be classified as Serial Multipliers, Parallel multipliers, Array multipliers, Tree multipliers and so on [4],[5]. Multipliers are categorized in relative to their architecture, applications, and the way of producing partial products and summing up of partial products to produce the final result.

In parallel multipliers numbers of partial products to be added is the main parameter that determines the performance of multiplier. In an array multiplier, futile computations occur on those columns or rows of adder corresponding to zero bits in the input operands. To save the power, we must first disable the futile computation and second bypass results from the previous stage [6], [7]. The computation can be disabled by either freezing its inputs or gating the logic evaluation. The former approach requires either input gating or multiplexing circuits while the latter approach needs extra gating logic along the evaluation path. The output signal bypassing must be realized by a multiplexer.

II. LITERATURE SURVEY

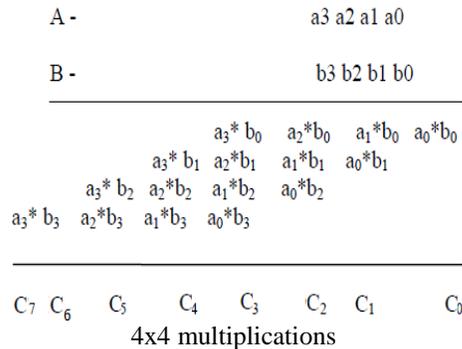
A. ARRAY MULTIPLIER

Array multiplier is an efficient layout of a combinational multiplier. Multiplication of two binary number can be obtained with one micro-operation by using a combinational circuit that forms the product bit all at once thus making it a fast way of multiplying two numbers since only delay is the time for the signals to propagate through the gates that forms the multiplication array. With its good structure, this multiplier is based on the standard add and shift operations. Each partial product is generated by taking into account the multiplicand and one bit of multiplier each time. The impending addition is carried out by high-speed carry-save algorithm and the final product is obtained employing any fast adder – the number of partial products depends upon the number of multiplier bits.

Consider the multiplication of two unsigned n-bit numbers, where $A = a_{n-1}, a_{n-2}, \dots, a_0$ is the multiplicand and $B = b_{n-1}, b_{n-2}, \dots, b_0$ is the multiplier. The product $C = c_{2n-1}, c_{2n-2}, \dots, c_0$, can be written as follows:

$$C = \sum_{i=0}^{n-1} \sum_{j=0}^{n-1} (a_i * b_j) 2^{i+j}$$

The additions are shown in the corresponding row is shown as



Conclusion: Array Multiplier gives more power consumption as well as optimum number of components required, but delay for this multiplier is larger. It also requires larger number of gates because of which area is also increased; due to this array multiplier is less economical [8] [9]. Thus, it is a fast multiplier but hardware complexity is high.

B. WALLACE TREE MULTIPLIER

For real-time signal processing, a high speed and throughput Multipliers-Accumulator (MAC) is always a key to achieve high performance in the digital signal processing system. The main consideration of MAC design is to enhance its speeds. That high speed is achieved through this well-known Wallace tree multiplier. Wallace introduced parallel multiplier architecture [10], [11] to achieve high speed. Wallace Tree algorithm can be used to reduce the number of sequential adding stages. Using this method, a three step process is used to multiply two numbers; the bit products are formed, the bit product matrix is reduced to a two row matrix where sum of the row equals the sum of bit products, and the two resulting rows are summed with a fast adder to produce a final product. In this architecture, all the bits of all partial products in each column are added together to a set of counters in parallel without propagating the carries. Another set of counters reduces this new matrix until a two row matrix is generated.

Generally the Wallace tree construction has many ways to implement. One way among them is considering all bits in a column and producing two bits as output for that column. Another way is to consider first four bits of a column and producing two bits which uses 4:2 compressors. And the other is considering first three bits in a column which uses 3:2 compressors. The Wallace Tree multiplier has an irregular structure [12]. Many different adder tree structures have been used to reduce the computation time of the multipliers. The computation time of the Wallace tree has achieved the lower bound of $O(\log_{3/2} N)$. For n-bit Wallace tree multiplier, the number of steps needed is $(\log_{3/2}(n/2) + 1)$. Wallace tree multipliers have significant complexity and timing advantages over traditional matrix multipliers.

Conclusion: In the Wallace tree method, the circuit layout is not easy although the speed of the operation is high since the circuit is quite irregular [13]. Wallace tree styles are generally avoided for low power applications, since excess of wiring is likely to consume extra power.



Fig.1 Wallace tree multiplier

C. BAUGH WOOLEY MULTIPLIER

Baugh-Wooley Two's complement Signed multipliers is the best known algorithm for signed multiplication because it maximizes the regularity of the multiplier and allow all the partial products to have positive sign bits. Baugh-Wooley technique was developed to design direct multipliers for Two's complement numbers [14]. When multiplying two's

complement numbers directly, each of the partial products to be added is a signed numbers. Thus each partial product has to be sign extended to the width of the final product in order to form a correct sum by the Carry Save Adder (CSA) tree.

Conclusion: According to the Baugh wooley approach, an efficient method of adding extra entries to the matrix is suggested to avoid negatively bits in the partial product matrix which results in extra circuitry and increase in power consumption.

D. BRAUN MULTIPLIER

Braun multiplier is well known due to its regular structure. It is a simple parallel multiplier that is commonly known as carry save array multiplier. This multiplier is restricted to performing multiplication of two unsigned numbers. It consists of array of AND gates and adders arranged in iterative structure that does not require logic registers. This is also known as the non-additive multiplier since it does not add an additional operand to result of multiplication.

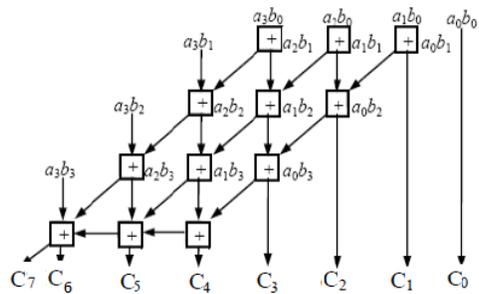


Figure 2: 4x4 Braun multiplier

An array implementation, known as the Braun multiplier is shown in Figure 2. In the 4x4 Braun multiplier, the multiplier array consists of rows of carry-saveadders (CSAs), in which each row contains 3 full adders (FAs). Each FA has three inputs and two outputs: the sum bit and the carry bit. 3 FAs in the first CSA row that have only two valid inputs can be replaced by 3 half adders (HAs) and 3 FAs in the last row can be constructed as a 3-bit ripple-carry adder.

Conclusion: One of the major disadvantages of the Braun's multiplier is that the number of components required increases quadratically with the number of bits which will make the multiplier to be inefficient. It cannot stop the switching activity even if the bit coefficient is zero that ultimately results in unnecessary power dissipation.

E. BOOTH MULTIPLIER

The Booth recoding multiplier is one such multiplier; it scans the three bits at a time to reduce the number of partial products [15]. These three bits are: the two bit from the present pair; and a third bit from the high order bit of an adjacent lower order pair. After examining each triplet of bits, the triplets are converted by Booth logic into a set of five control signals used by the adder cells in the array to control the operations performed by the adder cells. The method of Booth recording reduces the numbers of adders and hence the delay required to produce the partial sums by examining three bits at a time. To speed up the multiplication Booth encoding performs several steps of multiplication at once. Booth's algorithm takes advantage of the fact that an adder subtracted is nearly as fast and small as a simple adder.

Conclusion: The drawbacks of Booth multiplier are number of add subtract operations and the number of shift operation becomes variable and becomes inconvenient in designing parallel multipliers. The algorithm becomes inefficient when there are isolated 1's, which results in more power consumption due to large number of adders. Summing the partially redundant partial products requires as much hardware as representing them in the fully redundant form.

III. PROPOSED WORK

MODIFIED BOOTH ALGORITHM

Booth encoding is a method of reducing the number of partial products required to produce the multiplication result. To achieve high-speed multiplication, algorithms using parallel counters like modified Booth algorithm has been proposed and used. This type of fast multiplier operates much faster than an array multiplier for longer operands because it's time to compute is proportional to the logarithm of the word length of operands. By recoding the numbers that are to be multiplied, Modified Booth multiplier allows for smaller, faster multiplication circuits. The number of partial products is reduced to half, by using the technique of Booth recoding [16], [17]. Reduction in the number of partial products depends upon how many bits are recoded and on the grouping of bits.

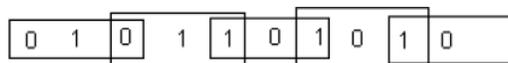


Fig.3 Grouping of bits from the multiplier term

Thus grouped multiplier will result in the production of bits between these five bits as follows as -2,-1, 0, +1, and +2. The advantage of this method is making the number of partial products into half of the multiplier term size by grouping.

The advantage of this method is making the number of partial products into half of the multiplier term size by grouping. The main disadvantage of the modified booth multiplier is its complexity of the circuit to produce partial product.

| Block | Re - coded digit | Operation |
|-------|------------------|-----------|
| 000 | 0 | 0 |
| 001 | +1 | +1 |
| 010 | +1 | +1 |
| 011 | +2 | +2 |
| 100 | -2 | -2 |
| 101 | -1 | -1 |
| 110 | -1 | -1 |
| 111 | 0 | 0 |

An example of modified booth algorithm is given as:

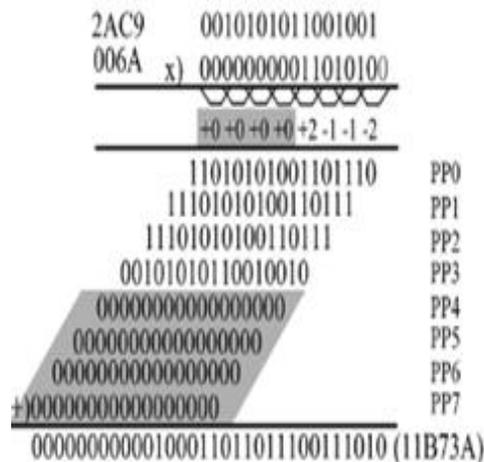


Fig.4 Example of Modified Booth Multiplier

This Booth Algorithm, is called the Modified Booth Algorithm or simply the Booth Algorithm, can be generalized to any radix. However, a 3-bit recoding would require the following set of digits to be multiplied by the multiplicand: 0, ±1, ±2, ±3, ±4. The difficulty lies in the fact that ±3Y is computed by summing (or subtracting) Y to ±2Y, which means that a carry propagation occurs. The delay caused by the carry propagation renders this scheme to be slower than a conventional one.

Consequently, only the 2 bit (radix 4) Booth recoding is used. So Modified Booth recoding is performed within two steps: encoding and selection. The purpose of the encoding is to scan the triplet of bits of the multiplier and define the operation to be performed on the multiplicand, as:

After scanning all the input three bits we will come to a conclusion that outcome of three input bits is the input bit other than the same two input bits, so we can bypass that multiplier through column bypassing technique which will help us to further reduce our delay.

IV. POWER CONSUMPTION

Power is the most important parameter in digital circuits to fabricate chips and portable devices. CMOS technology is used in digital circuits due to its less power consumption. Power consumption in CMOS circuits can be divided into dynamic and static power consumption.

$$P_s = a f_{clk} V_{dd}^2 C_l + I_{cc} V_{dd} + I_{leak} V_{dd}$$

Where a is the switching activity, f_{clk} is the clock frequency, C_l is the output capacitance, V_{dd} is the supply voltage, and I_{leak} is the leakage current.

V. BYPASSING TECHNIQUE

Dynamic power consumption can be reduced by bypassing method when the multiplier has more zeros in input data. To perform isolation, transmission gates can be used, as ideal switches with small power consumption, propagation delay similar to the inverter and small area. To study the proposed design we have consider column bypassing multiplier in which columns of adders are bypassed. In this multiplier, the operations in a column can be disabled if the corresponding bit in the multiplicand is 0. The advantage of this multiplier is it eliminates the extra correcting circuit.

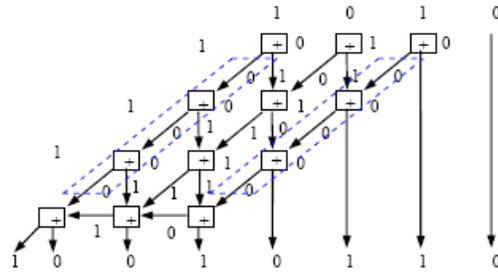


Fig. An example of Column Bypassing

VI. CONCLUSION

Considering all facts of the multipliers above, combinations of multiplier can give good result for operands which have greater number of bits. Its dynamic power saving is a main advantage in Low power VLSI design world with great battery backup. In this paper we have concluded reduced delay using modified booth algorithm with implemented on Spartan 3-AN family [19]. Optimization has been achieved using VERILOG instead of VHDL. This technique achieves higher delay reduction with lower hardware overhead and power is further reduced by switching off the unused circuit elements. This work can be further extended with the analysis of power and area when considered for ASIC implementation.

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