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# Comparative Analysis of CMOS Comparator in various Topologies for ADC Applications

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***Abstract — Watt Characterization of various CMOS comparators is presented. Topologies described are Two stage OPAMP, clock driven preamplifier-latch and high speed differential clocked comparator. These topologies are simulated in various technologies such as 0.18, 0.25, 0.35µm using Mentor Graphics. Watt Characteristics are analyzed at different temperatures for a range of power supply voltages. Simulation results are then reported and graphs are shown.***

***Keyword — CMOS Comparator, OP-Amp, Supply Voltage, ADC, Power Dissipation***

## I. INTRODUCTION

Analog-to-Digital Converters are most commonly used electronic devices to act as an interface between the real world and digital systems of these devices. The comparator circuit is one of its basic building block. The comparator is a circuit that compares an analog signal with another analog signal or reference and outputs a binary signal based on comparison. If the + input of comparator is at a greater potential than the –input , the output of the comparator is at logic 1, where as if the +input is at a potential less than the –input, the output of the comparator is at logic 0.

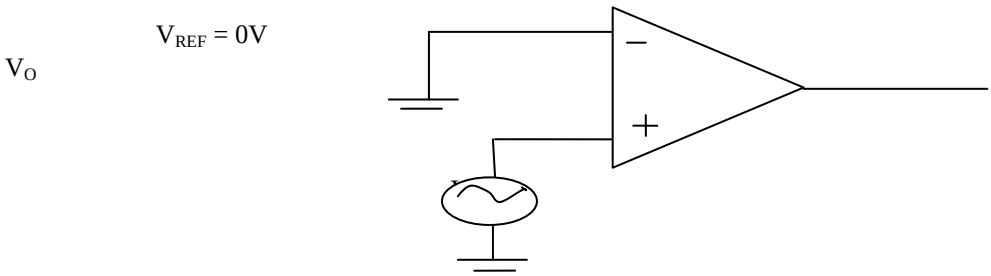


Fig 1: Symbol of comparator

This paper is organized into 5 sections. Mathematical analysis is described in section 2. CMOS comparator architectures are described in section 3. Simulation results and graphs are presented in section 4. Finally, conclusions are drawn in section 5.

## II. MATHEMATICAL ANALYSIS

### *A.Power Dissipation*

Power dissipation is one of the most important parameter that affects the performance of comparator. The power consumption of a CMOS comparator can be divided into three different components: dynamic, static (or leakage) and short circuit power consumption. Switching power, which includes both dynamic power and short-circuit power, is consumed when signals through CMOS circuits change their logic state, resulting in the charging and discharging of load capacitors. Leakage power is due to the sub-threshold currents and reverse biased diodes in a CMOS transistor. Thus,

$$P_{total} = P_{dynamic} + P_{leakage} + P\text{short-circuit}.$$

Dynamic switching power is the major component of overall power dissipation. When signals change their logic state in a CMOS transistor, energy is drawn from the power supply to charge up the load capacitance from 0 to V*dd*. For an inverter the power drawn from the power supply is dissipated as heat in PMOS transistor during the charging process. Energy is needed whenever charge is moved
against some potential. When the output of the inverter makes a transition from logic level 0 to 1, the load capacitance is charged. The energy drawn from the supply during the charging process is given by,

$$dEP = d(VQ) = V_{dd}.dQ \ldots.(i)$$

 

since the power supply provides power at a constant voltage V*dd*. Now, since Q =C.V. we have:

$$dQ = C.dV. \text{ Therefore,}$$
$$dEP = V_{dd}.C.dV \ldots.(ii)$$

Integrating above equation (ii), results in

$$E_P = \int_0^{Vdd} C.Vdd.dV \ldots.(iii)$$
$$= V_{dd}.C \int_0^{Vdd} dV \ldots.(iv)$$
$$= C.Vdd^2.$$

Thus a total of $C.Vdd^2$ energy is drawn from the power source. The energy $E_L$ stored in the capacitor at the end of transition can be computed as follows:

$$dE_L = d(VQ) = V.dQ \ldots.(v)$$

where V is the instantaneous voltage across the load capacitance, and Q is the instantaneous charge of the load capacitance during the loading process. Therefore,

$$dE_L = V.C.dV \ldots.(vi)$$

Integrating above equation (vi), results in

$$E_L = \int_0^{Vdd} C.V.dV \ldots.(vii)$$
$$= C_L.Vdd^2/2.$$

Half of the energy drawn from the power supply is stored in the load capacitance; the rest is dissipated as heat. The energy stored in the output capacitance is released during the discharging of the load capacitance, which occurs when the output of the inverter makes a transition from logic level 1 to 0. The load capacitance of the CMOS logic gate consists of the node capacitance of output of the logic gate, the effective interconnect capacitance, and the input node capacitance of the driven gate. The low power design methodology concentrates on minimizing this major component given by the expression:

$$P=C.Vdd^2.F \ldots.(viii)$$

Where,

F is output frequency, Vdd is the supply voltage, and C is the output load capacitance.

## III. CMOS COMPARATOR ARCHITECTURES

The schematics of three comparators are shown. Power analysis begins with study of Two stage OPAMP based comparator which is beneficial in low power applications such as in many biomedical applications, then proceeds with Clock driven preamplifier-latch comparator that is suitable for sigma-delta Analog-to-Digital converter and ends at high speed differential clocked comparator.

### *A. Two Stage OPAMP based CMOS comparator*

First stage of this comparator is composite cascode differential amplifier consisting of N-channel input devices (MN2-MN3) in series with combination of cascade active PMOS based current mirror load such as (MP1-MP4) that compares the two inputs providing smaller gain. Second stage is common source amplifier (MP5 and MN8) provide larger swing and greater gain [11]. This comparator does not require stability criteria so it eliminated need for compensation capacitor.

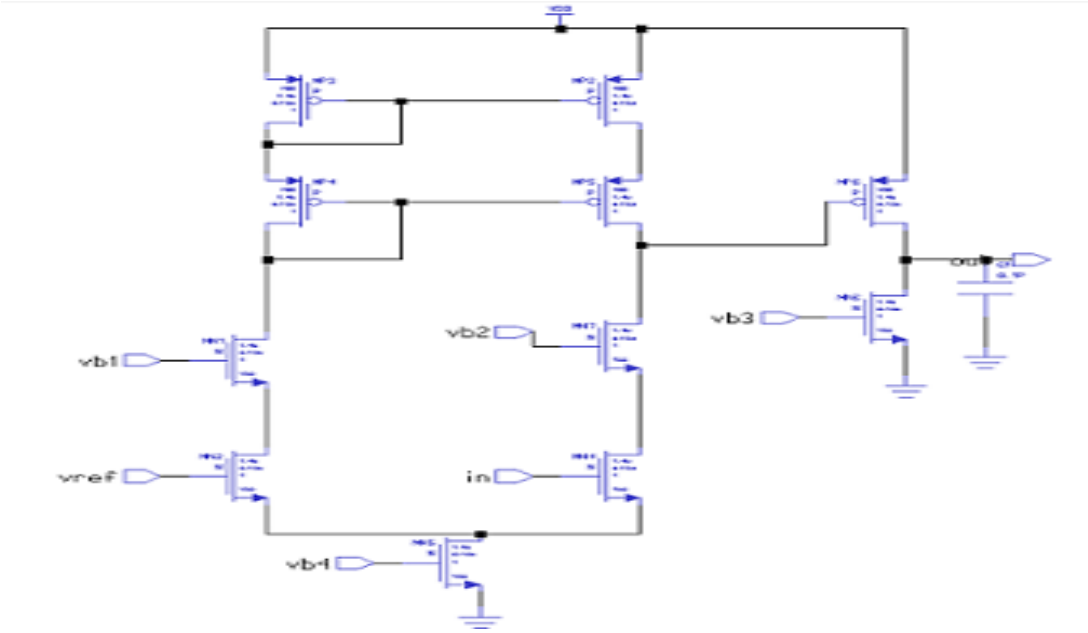


Fig 2: Two stage OPAMP based comparator (comparator1)

 

*B. Clock Driven Preamplifier-Latch Comparator*

Two most important component of this comparator are preamplifier and latch circuits. Preamplifier stage consists of transistor (N1-N5). And latch circuit is realized by cross coupled inverters that forms a differential comparator. Latch part consists of transistors (N6-N14) which includes two back to back connected inverter pair (N10-N11) & (N12-N13) and the charge imbalance circuitry (N6-N9). An NMOS transistor N14 is connected between two differential nodes of latch. The latch operates in two phases; reset and regeneration. In the reset phase, the charge imbalance is created on the differential nodes of latch that is proportional to the variations in the input signal. In regeneration phase, the imbalance in voltage on the nodes is sampled to the rail to rail digital levels by the NMOS and PMOS regeneration loops [12]. During the regeneration process, comparator uses the positive feedback mechanism to scale the digital level. The variations in voltage at the regeneration nodes are coupled to the inputs and disturb the input voltages. This disturbance is called the kickback noise. N7-N8 transistors are used to reduce kickback noise.

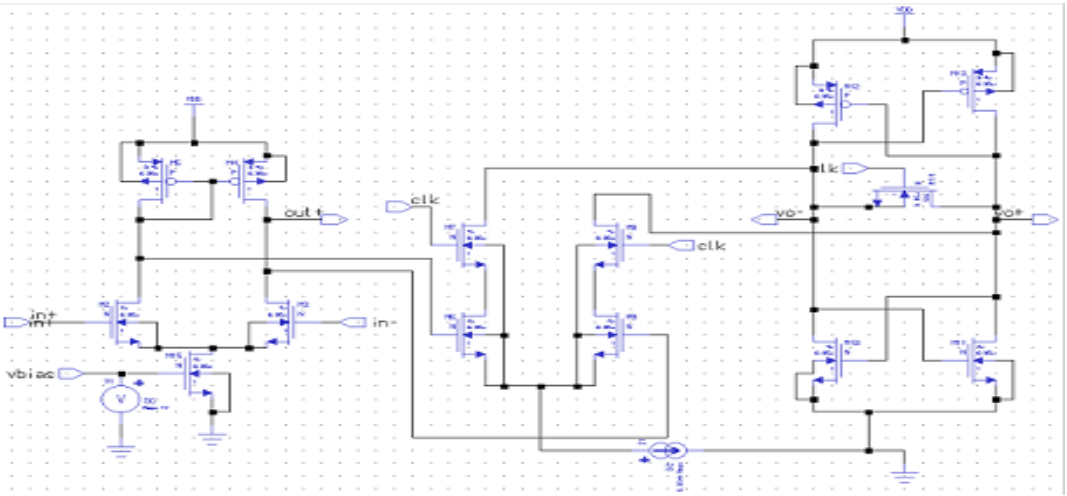


Fig 3: Clock driven preamplifier-latch comparator (comparator2)

*C. High Speed Differential Clocked Comparator*

This comparator has three basic components: a preamplifier, a latch, and an output sampler. The preamplifier has PMOS transistors as differential input pairs. The output current of the preamplifier are mirrored into the latch stage. The latch consists of the cross coupled inverters connected to the ground through the clock enabled transistor [7]. The latch operates in two phases, reset and evaluation, respectively. During reset phase, the latch output voltage is at the midpoint of the power supply rail voltages, which give a smaller regeneration time. During the evaluation phase, the latch is activated and outputs are sampled. The last part, the output sampler, consists of a transmission gate and inverters as buffers. Latch is sampled by the transmission gate during the evaluation phase and then the samples are amplified and the outputs are buffered by inverters. Sampling signals, "samp" and "sampB" are generated using two delay lines and three inverters constitutes a delay line.

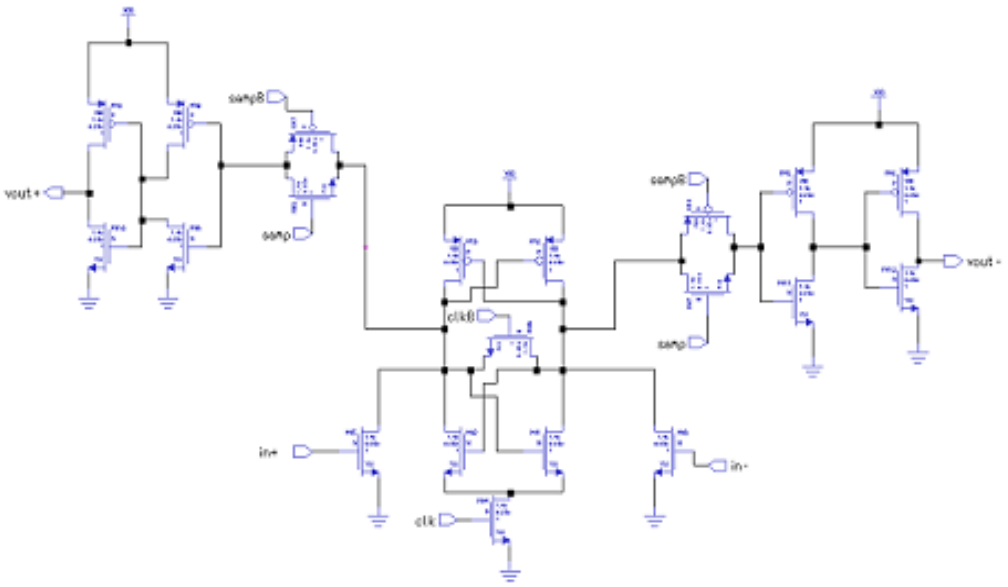


Fig 4: High Speed Differential Clocked Comparator.(comparator 3)

 

## IV. SIMULATION RESULTS AND DISCUSSIONS

Simulation of the comparators is done using Mentor Graphics to analyze the thermal behavior. These designs are simulated in 0.18, 0.25 and 0.35µm technologies at different temperatures. Power dissipation are measured for various ranges of power supply voltages. Fig 5 represent the simulated transient curve of comparator 1. Fig 6 represent the simulated transient curve of comparator 2. Fig 7 represent the simulated transient curve of comparator 3.

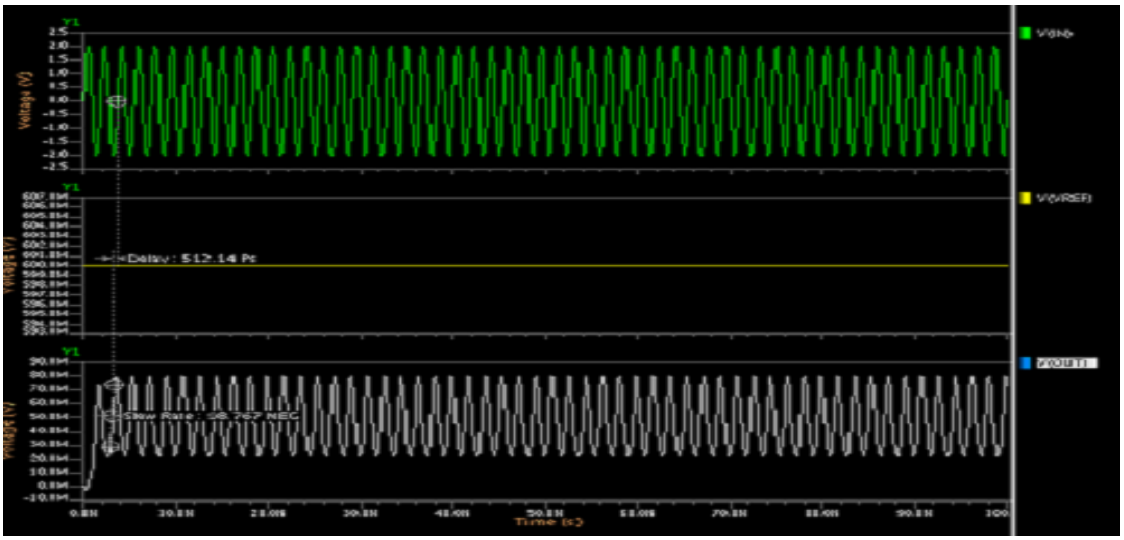


Fig 5: Transient response of comparator1

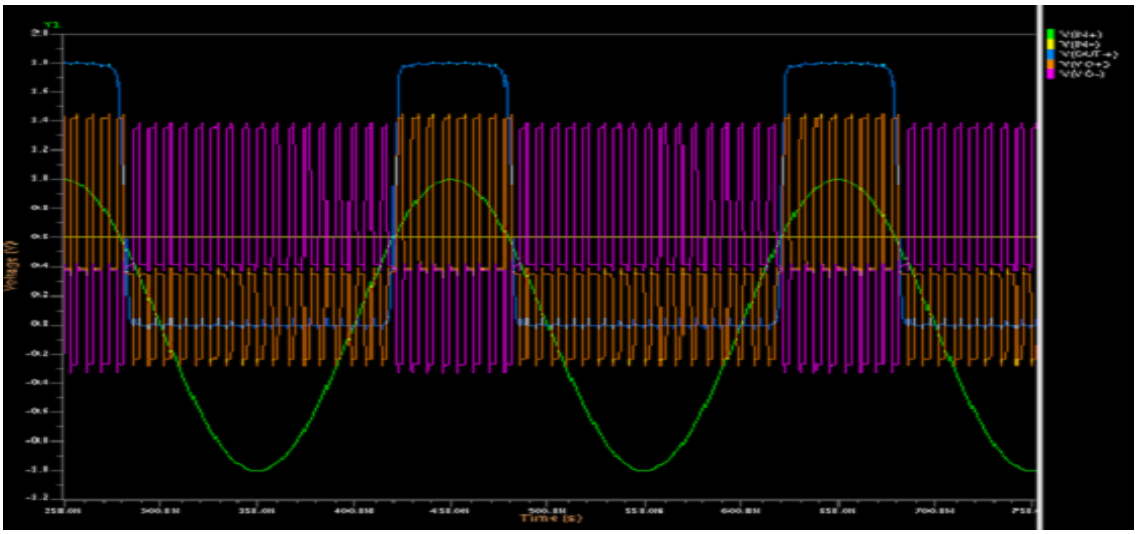


Fig 6: Transient response of comparator2

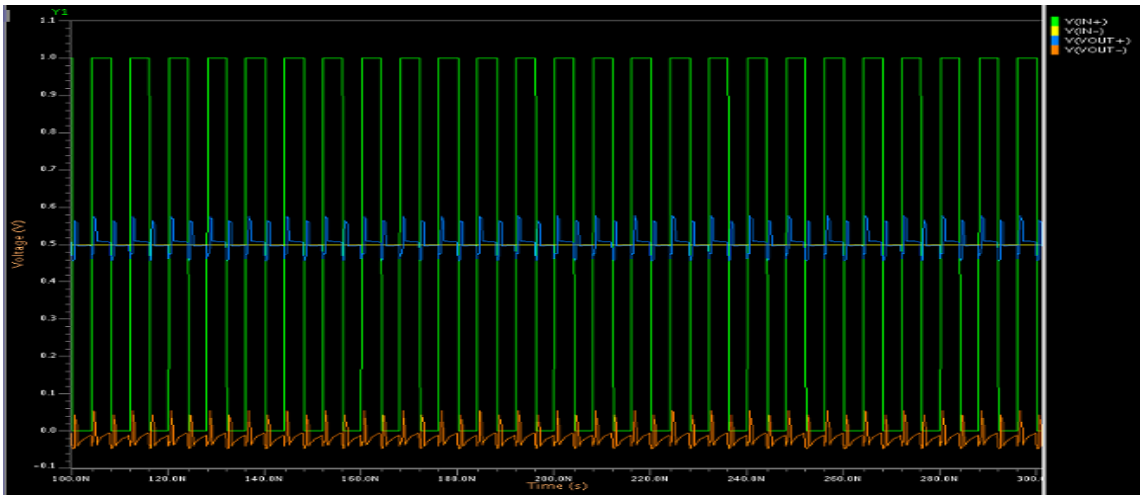


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Fig 7: Transient response of comparator3

*POWER ANALYSIS*

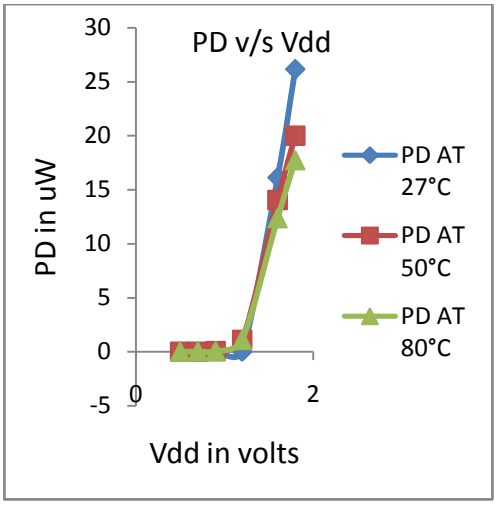
Power dissipation of above three comparators are measured at different temperatures using different technologies in mentor graphics. We have plotted the graphs between supply voltage and power dissipation at 27°C, 50°C and at 80°C showing watt characterization of these comparators.

A. *0.18µm Technology :*

This technology employs the channel length = 0.18µm of Metal oxide semiconductor field effect transistor.

TABLE 1. POWER DISSIPATION OF COMPARATOR 1

| Vdd | AT 27°C | AT 50°C | AT 80°C |
|---|---|---|---|
| 0.5V | 0.073941 | 0.1252 | 0.53511 |
| 0.7V | 0.142446 | 0.218908 | 1.1424 |
| 0.9V | 0.24647 | 0.35675 | 1.1774 |
| 1.2V | 0.52356 | 0.687019 | 1.8113 |
| 1.6V | 1.384 | 1.6227 | 2.9887 |
| 1.8V | 2.2632 | 2.529 | 3.7741 |

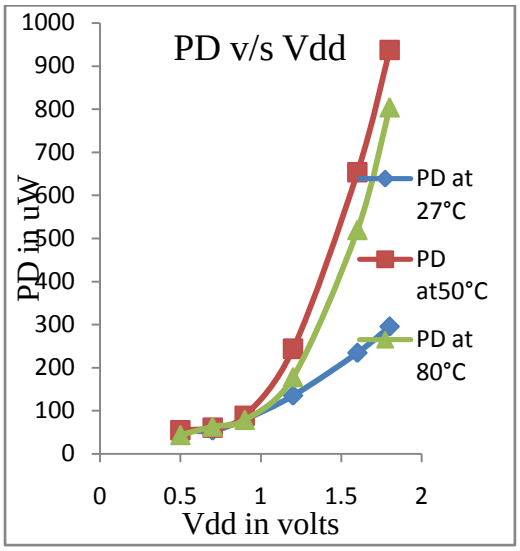



Graph 1: Shows the variation of Pow wrt Vdd for Comparator 1.

TABLE 2. POWER DISSIPATION OF COMPARATOR 2

| Vdd | AT 27°C | AT 50°C | AT 80°C |
|---|---|---|---|
| 0.5V | 0.000233 | 0.00041621 | 0.000847 |
| 0.7V | 0.003146 | 0.0047136 | 0.007435 |
| 0.9V | 0.037619 | 0.0475066 | 0.061439 |
| 1.2V | 0.00107 | 1.084 | 1.0979 |
| 1.6V | 16.14 | 14.055 | 12.381 |
| 1.8V | 26.181 | 20.011 | 17.7625 |

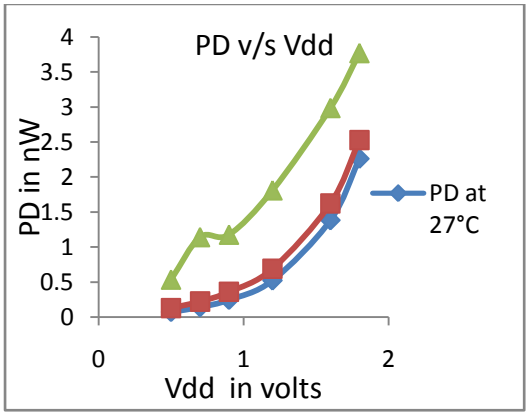
 




Graph 2: Shows the variation of Pow wrt Vdd for comparator 2

TABLE 3. POWER DISSIPATION OF COMPARATOR 3

| Vdd | AT 27°C | AT 50°C | AT 80°C |
|---|---|---|---|
| 0.5V | 54.381 | 54.661 | 43.6401 |
| 0.7V | 54.0336 | 60.2957 | 63.287 |
| 0.9V | 80.135 | 88.022 | 78.7887 |
| 1.2V | 135.286 | 243.77 | 178.095 |
| 1.6V | 234.619 | 653.53 | 519.666 |
| 1.8V | 295.65 | 937.43 | 804.37 |




Graph 3: Shows the variation of Pow wrt Vdd for Comparator 3.

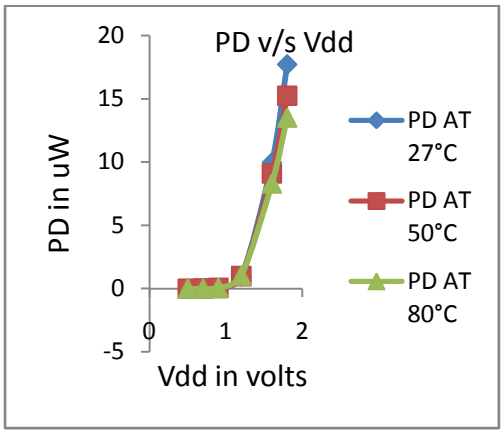
 

*B. 0.25µm Technology:*

This technology employs the channel length = 0.25µm of Metal oxide semiconductor field effect transistor.

TABLE 4. POWER DISSIPATION OF COMPARATOR 1

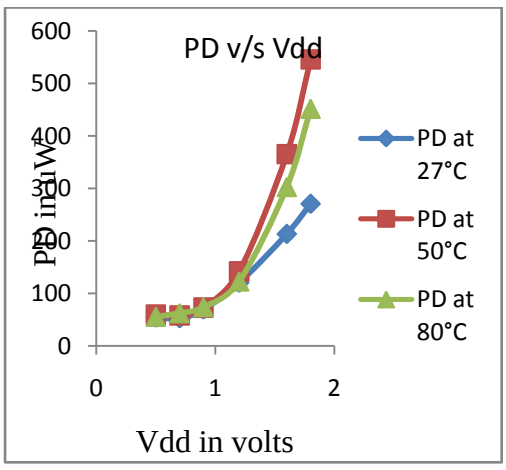
| Vdd | AT 27°C | AT 50°C | AT 80°C |
|---|---|---|---|
| 0.5V | 0.0002334 | 0.000397 | 0.000804 |
| 0.7V | 0.003585 | 0.0052776 | 0.008154 |
| 0.9V | 0.04399 | 0.055051 | 0.070476 |
| 1.2V | 0.94114 | 0.989898 | 1.0379 |
| 1.6V | 9.9533 | 9.08689 | 8.314 |
| 1.8V | 17.7085 | 15.221 | 13.512 |




Graph 4: Shows the variation of Pow wrt Vdd for Comparator 1.

TABLE 5. POWER DISSIPATION OF COMPARATOR 2

| Vdd | AT 27°C | AT 50°C | AT 80°C |
|---|---|---|---|
| 0.5V | 53.976 | 59.9207 | 55.7214 |
| 0.7V | 52.66 | 58.4797 | 62.54 |
| 0.9V | 69.509 | 73.1972 | 73.977 |
| 1.2V | 120.3466 | 142.009 | 123.046 |
| 1.6V | 213.2349 | 365.222 | 303.017 |
| 1.8V | 270.6052 | 545.497 | 452.06 |

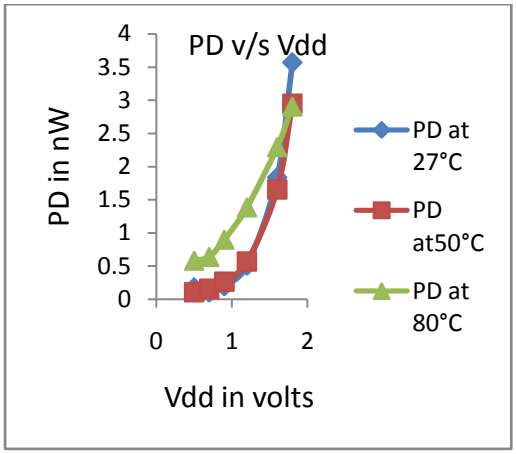



Graph 5: Shows the variation of Pow wrt Vdd for Comparator 2.

TABLE 6 . POWER DISSIPATION OF COMPARATOR 3

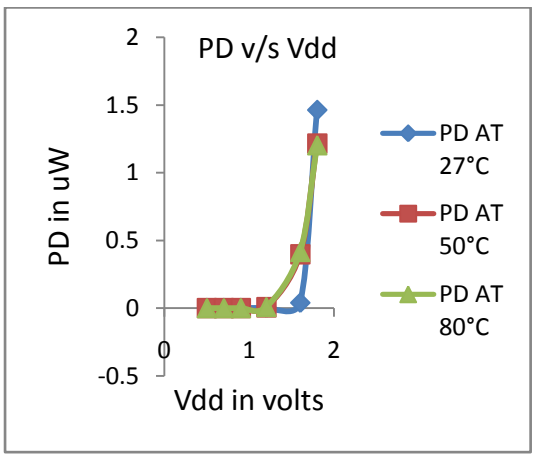
| Vdd | AT 27°C | AT 50°C | AT 80°C |
|---|---|---|---|
| 0.5V | 0.17785 | 0.105216 | 0.58144 |
| 0.7V | 0.10228 | 0.154609 | 0.63749 |
| 0.9V | 0.197174 | 0.26348 | 0.897863 |
| 1.2V | 0.506187 | 0.56662 | 1.3851 |
| 1.6V | 1.8368 | 1.6538 | 2.2925 |
| 1.8V | 3.5656 | 2.9473 | 2.9055 |




Graph 6: Shows the variation of Pow wrt Vdd for Comparator3. *0.35µm Technology:*
This technology employs the channel length = 0.35µm of Metal oxide semiconductor field effect transistor.

TABLE 7. POWER DISSIPATION OF COMPARATOR 1

| Vdd | AT 27°C | AT 50°C | AT 80°C |
|---|---|---|---|
| 0.5V | 0.0000014 | 0.0000033 | 0.000113 |
| 0.7V | 0.00000658 | 0.000013 | 0.000102 |
| 0.9V | 0.0000674 | 0.000126 | 0.000343 |
| 1.2V | 0.003796 | 0.005407 | 0.008088 |
| 1.6V | 0.0389 | 0.3965 | 0.414822 |
| 1.8V | 1.4622 | 1.215 | 1.2029 |

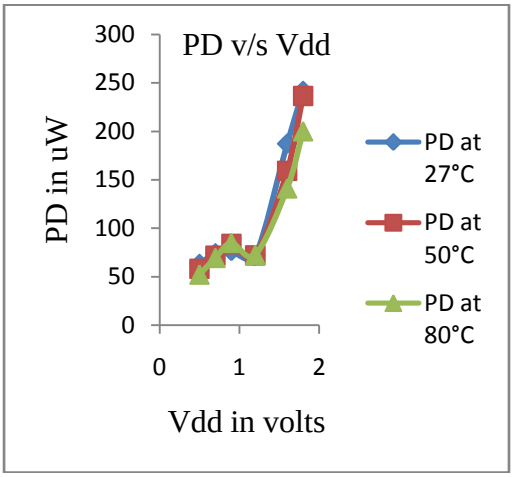



Graph 7: Shows the variation of Pow wrt Vdd for Comparator 1.

TABLE 8. POWER DISSIPATION OF COMPARATOR 2

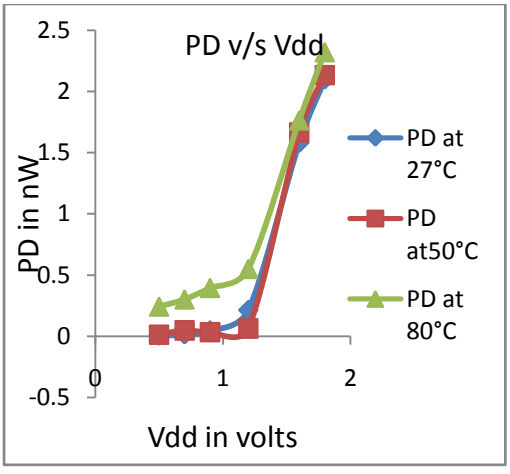
| Vdd | AT 27°C | AT 50°C | AT 80°C |
|---|---|---|---|
| 0.5V | 63.1953 | 58.131 | 52.316 |
| 0.7V | 74.144 | 71.558 | 69.503 |
| 0.9V | 76.6433 | 83.726 | 84.913 |
| 1.2V | 71.6433 | 72.0568 | 72.678 |
| 1.6V | 187.323 | 159.158 | 141.244 |
| 1.8V | 241.83 | 236.449 | 200.204 |




Graph 8: Shows the variation of Pow wrt Vdd for Comparator 2.

TABLE 9. POWER DISSIPATION OF COMPARATOR 3

| Vdd | AT 27°C | AT 50°C | AT 80°C |
|---|---|---|---|
| 0.5V | 0.006416 | 0.013552 | 0.24434 |
| 0.7V | 0.016488 | 0.04849 | 0.302769 |
| 0.9V | 0.048388 | 0.033291 | 0.39677 |
| 1.2V | 0.21492 | 0.06447 | 0.55182 |
| 1.6V | 1.5808 | 1.6654 | 1.7655 |
| 1.8V | 2.0987 | 2.1322 | 2.3222 |




Graph 9: Shows the variation of Pow wrt Vdd for Comparator 3.

## V. CONCLUSION

This paper explains about the Comparator and its design in three different topologies. The three topologies of CMOS based Comparators have been implemented in 0.18, 0.25 & 0.35 μm technologies and power analysis between them is made by analyzing pre-layout simulation results. The basic parameter need to be considered in any design is Power Dissipation. Tables show that different circuits have different advantages and disadvantages. Still, the selection of any topology is based on the application and the requirements.

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