Volume 4, Issue 5, May 2014 ISSN: 2277 128X
International Journal of Advanced Research in Computer Science and Software Engineering
Research Paper
Available online at: www.ijarcsse.com

A Novel Design of Low-Power Two Stage Cas Code Op-Amp

B.Krishna, D. Arunkumar
KITE Womens College of Professional Engineering Sciences-SHABAD

Abstract-This paper presents, A Novel design of Low power two stage operational amplifiers with low power, high speed, high gain, high slew rate. The design is carried out using LTSPICE tool in 180 nm technology.
Index Terms-Gain, Slew rate, Bandwidth,LT spice

Keyword-

I. INTRODUCTION

The design shown below is a two-stage op amp with an n-channel input pair. The Op amp uses a dual-polarity power supply (Vdd and Vss) so the AC signals can swing above and below ground and also be centered at ground.The power supply here is constrained within +1.65V and -1.65V. Based on the design parameters of 180 nm technology,the topology was determined to achieve the specifications listed below through the Op Amp design procedure provided in the section 6.3 of CMOS Analog Circuit Design by Phillip Allen.

A. Specifications

Parameter	Value
Technology	180 nm
Phase Margin	>60 degrees
Slew Rate (SR):	10 V/µs
Power Supply	±1.65 V
DC Gain	>70 dB
Unity Gain Frequency (UGF)	15 MHz

Table 1. Two stage op-amp Specifications

B. Circuit diagram

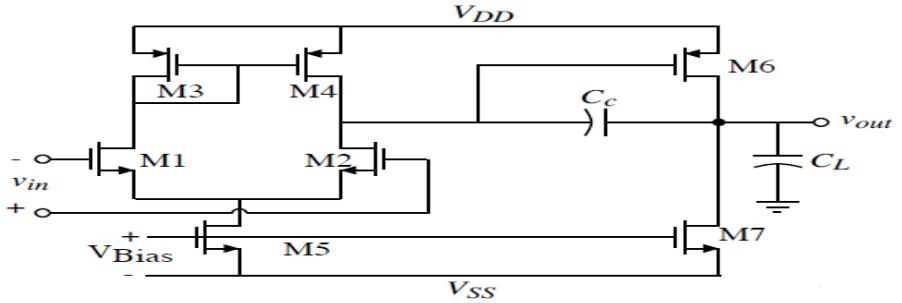


Fig 1.Circuit diagram of two stage op-amp

II. DESIGN CALCULATIONS

First we have to calculate I_{bias} which can be calculated from the below equation. Considercoupling capacitor Cc=3 pF.

$I_{bias}= SR*C_c = 30\mu A$ (1)

Now, We have to calculate Trans-conducatace g_m using below equation

$g_m= 2\pi (UGF)C_c = 91.2\mu S$ (2)

Now calculate aspect ratios of M_1 and M_2 using the below equation

$(W/L)_1=(W/L)_2 =g_m^2/(K_nI_{bias})$ (3)

$M_1=M_2=1.5\mu/540n$

In order to calculate other transistors aspect ratio use MOSFET current equation,

$Id= \frac{\mu Cox}{2}.\frac{W}{L}.(Vgs-Vth)^2$ (4)

Calculated aspect ratios of all MOS transistors are as shown below

$M_3=M_4=15\ \mu/540n$

M_5=M_6=14.7µ/540n
M_7=85 µ/540n
M_8=42.9 µ/540n

III. SIMULATION RESULTS

A. *Circuit Diagram*

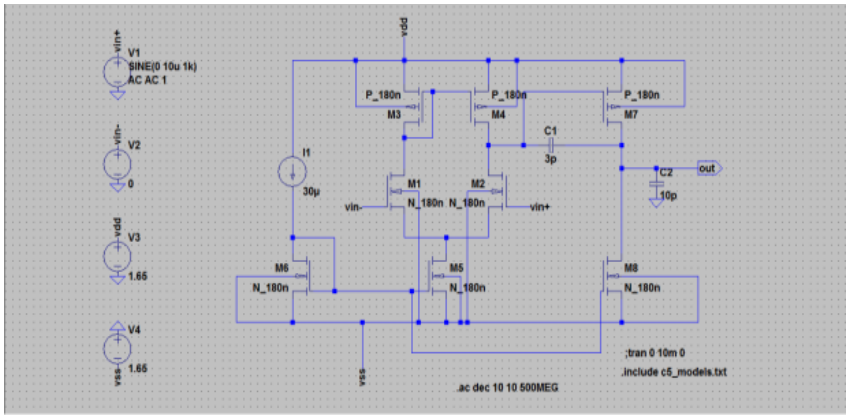


Fig 2. Two stage op-amp

B. *Symbol of two stage op-amp*

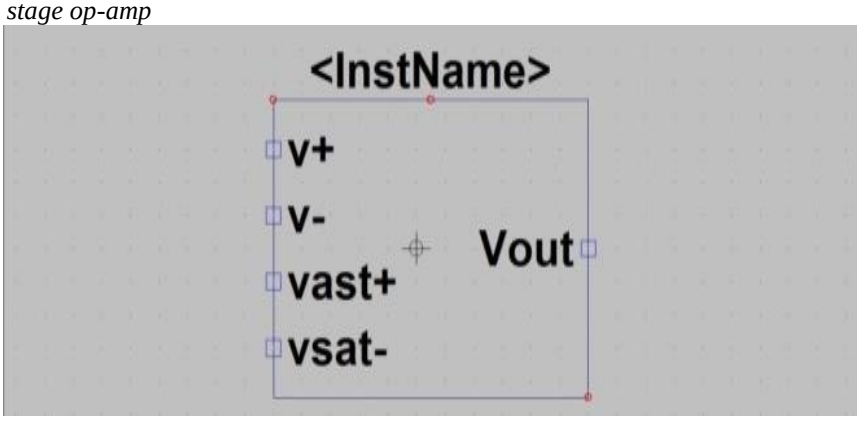


Fig 3. Symbol of Two stage op-amp

C. *Offset of two stage op-amp*

Two stage op-amp offset is obtained by giving both differential inputs as zero volts and by doing a transient analysis. Below result shows the offset of the two stage op-amp.From simulation Results it can be seen that offset is 142µV.

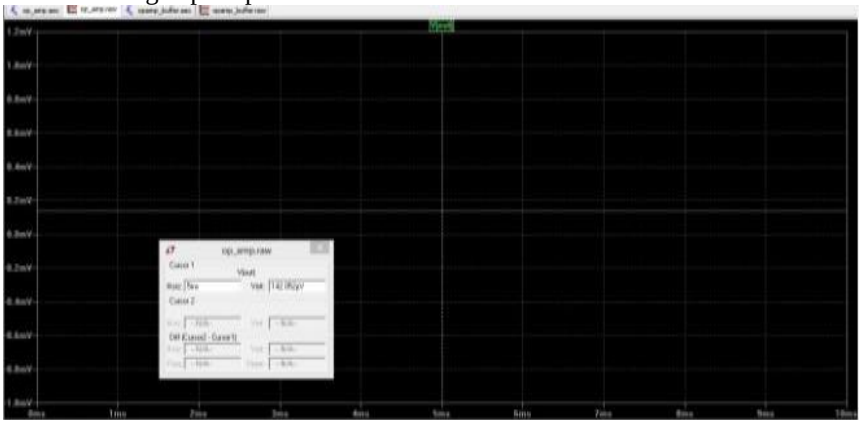


Fig 4. Offset of two stage op-amp

D. *AC analysis of two stage op-amp*

AC analysis is done by giving a AC signal(sinusoidal signal) and by doing AC analysis we can calculate Gain, Unity Gain frequency(UGF) and Phase Margin.The frequency at which gain becomes 0 dB is called UGF.From Phase Margin we can comment on stability. From the simulation results it can be seen that Gain=68 dB, Phase Margin=65 degrees and UGF=14MHz.

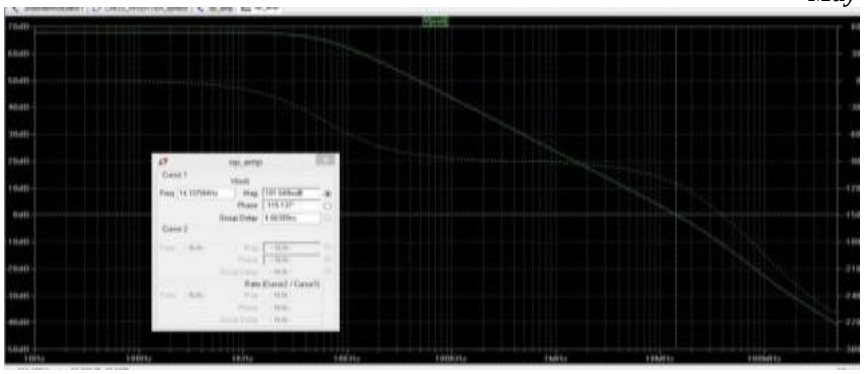


Fig 5. AC analysis of two stage op-amp

E. Slew rate

Slew rate of an Op amp is defined as the maximum rate of change of output for the small change in input

$$SR = \left[\frac{dVo}{dt}\right]_{max}$$

Generally SR is determined from the slope of output waveform during rise or fall of the output when the input is applied. So, we have a positive SR and a negative SR. From Simulation Results we can say that it has a positive slew rate of 10.8 v/µs and negative slew rate of 9.32 V/µs.

Circuit to calculate Slew rate

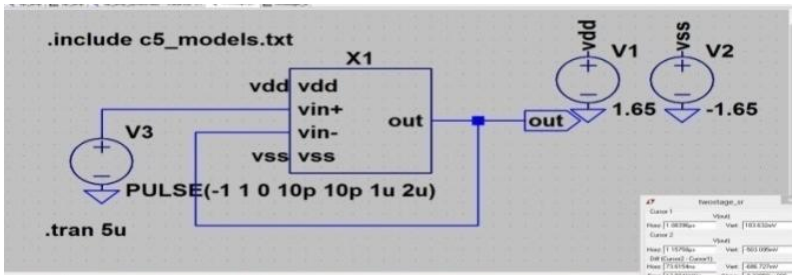


Fig 6. Slew rate of two stage op-amp

Positive slew rateof two stage op-amp

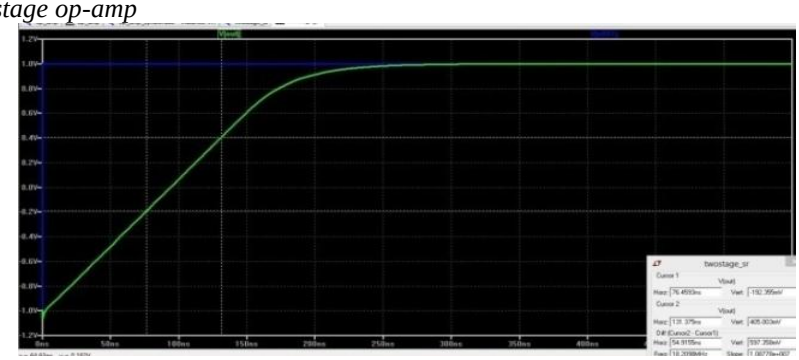
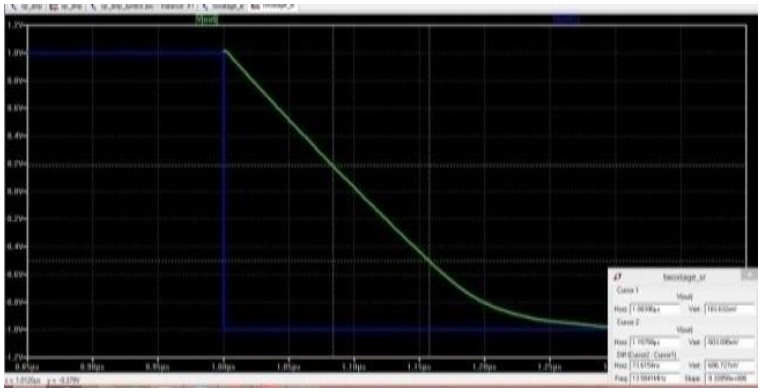


Fig 7. Positive slew rate of two stage op-amp



Negative slew rate of two stage op-amp

Fig 8. Negative slew rate of two stage op-amp

Power dissipation

From simulation results it can be seen that the power dissipation is 2.1mW.

Fig 9.Power dissipation of two-stage op-amp

Summary table of simulation results

Parameter	**Simulation Values**
Phase Margin	65 degrees
Slew Rate (SR):	10.8 V/µs,-9.32 V/µs
Offset voltage	142 µV
DC Gain	>70 dB
Unity Gain Frequency	14 MHz
Power Dissipation	2.1mW

IV. CONCLUSION

In this thesis, a Low power high speed two stage cascode op-amp capable of providing high gain(68dB) and High speed with more stable(Phase margin=65) is designed in LTSPICE with 180nm CMOS technology. Simulation results are observed that circuit dissipates very low power.

REFERENCES

[1] P. Phillip E Allen and Douglas R. Holdberg, "CMOS analog circuit design" Oxford series.

ABOUT AUTHORS

Mr.B.Krishna completed **B.Tech** in ECE From Dr.Paul-Raj Engineering College Bhadrachalam(JNTUH) in 2005 and ,**M.Tech**(VLSI-SD) From SITAMS-Chittoor(JNTUH) in 2008. Presently he is working in **KITE Womens College of Professional Engineering Sciences as a Asst. Professor**

Mr. D.Arunkumar-Graduated(**B.Tech**) from Vaagdevi College Of Engineering in Electronics and Communication Engineering and **Master in Engineering** from Vasavi college of Engineering in Embedded Systems and VLSI Design. Presently he is working in **KITE Womens College of Professional Engineering Sciences as a Asst. Professor**

